DATA SHEET

NEC

TFT COLOR LCD MODULE
NL128102AC23-02

39 cm (15.4 inches), 1280 × 1024 pixels, Full-color, Wide viewing angle Multi-scan Function

DESCRIPTION

NL128102AC23-02 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL128102AC23-02 has a built-in backlight with an inverter.

The 39 cm (15.4 inches) diagonal display area contains 1280 × 1024 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has multi-scan function.

FEATURES

- Wide viewing angle (with retardation film)
- High luminance and low reflection
- Multi-scan function: e.g., SXGA, XGA, SVGA, VGA, VGA-TEXT, MAC
- Incorporated edge type backlight with an inverter (Four lamps into two lamp holders)
- Lamp holder replaceable

APPLICATIONS

- Desk-top type of PC
- Engineering work station
- Display terminals for control system

On Screen Display

Regarding the use of OSD, please note that there is possibility of conflicts with a patent in Europe and the U.S. Thus, if such conflict might happen when you use OSD, we shall not be responsible for any trouble.

The information in this document is subject to change without notice.
Please confirm with the delivery specification before starting to design the system.

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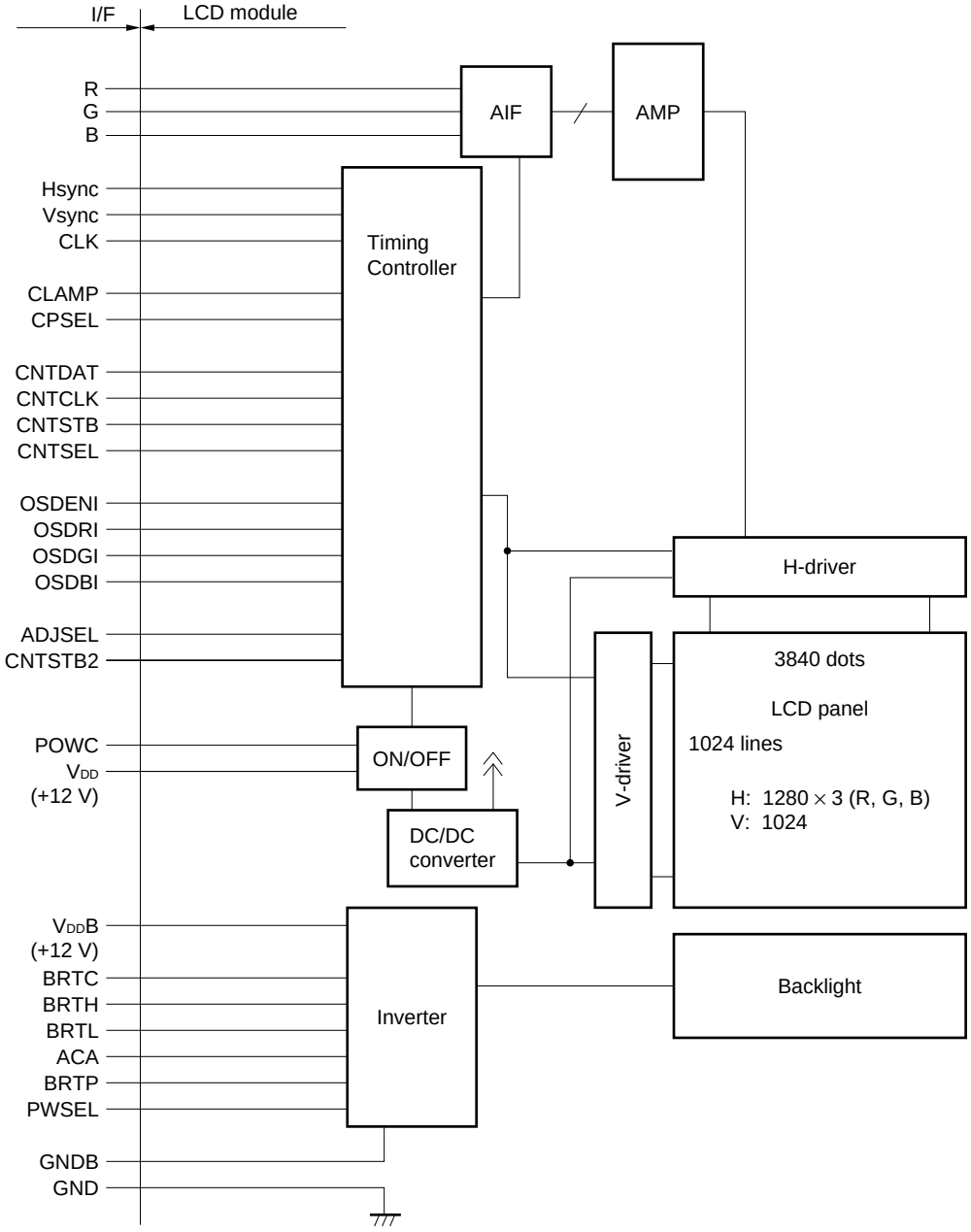
STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

BLOCK DIAGRAM



Note Neither GND nor GNDB is connected to Frame.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	305.28 (H) × 244.224 (V) mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1280 × 1024 pixels
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.2385 (H) × 0.2385 (V) mm
Module size	350.0 (H) × 284.8 (V) × 21.0 (typ.) (D) mm
Weight	1560 g (typ.)
Contrast ratio	200 : 1 (typ.)
Viewing angle (more than the contrast ratio of 10 : 1)	
	Horizontal : 60° (typ., left side, right side)
	Vertical : 50° (typ., up side), 45° (typ., down side)
Color gamut	59% (typ., at center, to NTSC)
Response time	7 ms (typ.), white 100% to black 100%
Luminance	200 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals (Hsync and Vsync), Dot clock (CLK)
Supply voltages	12 V (Logic/LCD driving), 12 V (Backlight)
Backlight	Edge light type: Four cold cathode fluorescent lamps with an inverter • Lamp holder: type No. 154LHS02 • Inverter: type No. 154PW021
Power consumption	26.4 W (typ.)

GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	350.0 ± 0.6 (H) × 284.8 ± 0.6 (V) × 21.5 (MAX.) (D)	mm
Display area	305.28 (H) × 244.224 (V)	mm
Number of dots	1280 × 3 (H) × 1024 (V)	dot
Number of pixels	1280 (H) × 1024 (V)	pixel
Dot pitch	0.0795 (H) × 0.2385 (V)	mm
Pixel pitch	0.2385 (H) × 0.2385 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	full color	color
Weight	1620 (max.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks	
Supply voltage	V_{DD}	–0.3 to +14	V	T_a = 25°C	
	$V_{DD}B$	–0.3 to +14	V		
Logic input voltage	V_{in1}	–0.3 to +5.5	V	T_a = 25°C V_{DD} = 12 V	
R,G,B input voltage	V_{in2}	–6.0 to +6.0	V		
CLK input voltage	V_{in3}	–7.0 to +7.0	V		
BRTL input voltage	V_{in4}	–0.3 to + 1.5	V		
Storage temp.	T_{ST}	–20 to + 60	°C	–	
Operating temp.	T_{OP}	0 to +50	°C	Module surface	**Note 1**
Humidity	≤ 95% relative humidity			T_a ≤ 40°C	No condensation
	≤ 85% relative humidity			40 < T_a ≤ 50°C	
	Absolute humidity shall not exceed T_a = 50°C, 85% relative humidity level.			T_a > 50°C	

Note 1: Measured at the LCD panel

ELECTRICAL CHARACTERISTICS

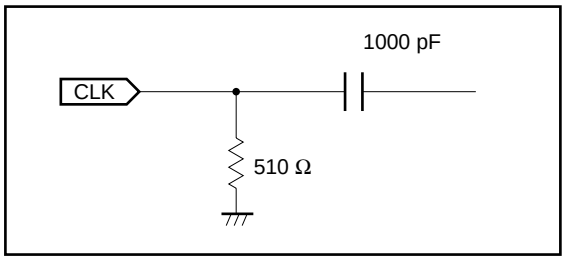
(1) Logic, LCD driving, Backlight

T_a = 25°C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply voltage	V_{DD}	11.4	12.0	12.6	V	for logic and LCD driving
	$V_{DD}B$	11.4	12.0	12.6	V	for backlight
Logic input “L” voltage 1	V_{IL}	0	–	0.8	V	Hsync/Csync, Vsync, SEL, UP, DOWN, EXIT, VOLSEL, DDCDAT, DDCCLK, OSDSEL, WPRT, MENUSEL
Logic input “H” voltage 1	V_{IH}	2.0	–	5.25	V	
Logic input “L” voltage 2	ViL2	0	–	0.8	V	Logic except BRTP
Logic input “H” voltage 2	ViH2	2.0	–	5.25	V	
CLK input voltage	ViCLK	0.6	–	1.0	Vp-p	for CLK
CLK DC input voltage	ViDCCLK	–4.5	–	+4.5	V	
Logic input “L” current 1	I_{iL1}	–1	–	–	μA	Hsync/Csync, Vsync
Logic input “H” current 1	I_{iH1}	–	–	1	μA	
Logic input “L” current 2	I_{iL2}	–	–	1	μA	DDCDAT
Logic input “H” current 2	I_{iH2}	–1	–	–	μA	
Logic input “L” current 3	I_{iL3}	–10	–	–	μA	for CNTDAT, CNTSTB, CNTCLK, CLAMP, OSDENI, OSDRI, OSDGI, OSDBI, ADJSEL, CNTSTB2
Logic input “H” current 3	I_{iH3}	–	–	1400	μA	
Logic input “L” current 4	I_{iL4}	–1.0	–	–	mA	for BRTP
Logic input “H” current 4	I_{iH4}	–	–	10	mA	
Logic input “L” current 5	I_{iL5}	–1.0	–	–	mA	for ACA, BRTC, PWSEL, BRTL
Logic input “H” current 5	I_{iH5}	–	–	0.8	mA	
Supply current **Note 1**	I_{DD}	–	1000	1500	mA	for LCD driving V_{DD} = 12.0 V
	$I_{DD}B$	–	1400	1600	mA	for back light $V_{DD}B$ = 12.0 V (max. luminance)

Note 1: The display is Dot-checkered pattern.

(2) CLK input equivalent circuit

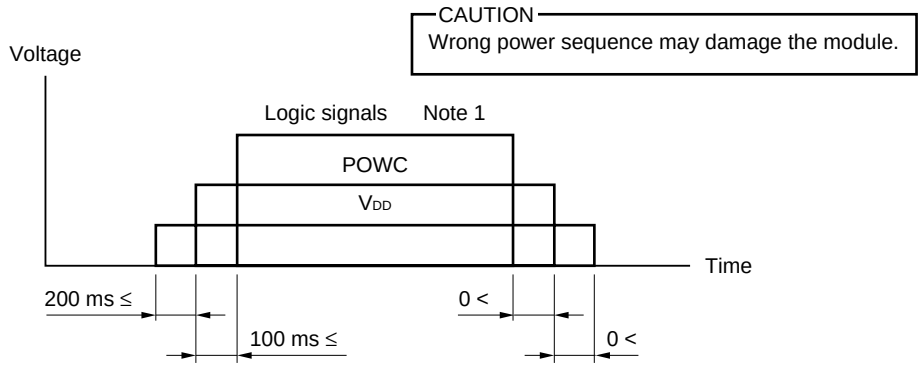


(3) Video signal (R,G,B) input

T_a = 25°C

Item	MIN.	TYP.	MAX.	Unit	Remarks
Maximum amplitude (white - black)	0 (black)	0.7 (white)	0.9	Vp-p	Need to adjust contrast if input more 0.7 Vp-p
DC input level (black)	–3.5	–	+3.5	V	–

POWER SUPPLY SEQUENCE



Note 1: Synchronous signals, Control signals, CLK

(1) Logic signals (synchronous signals and control signals) should be “0” voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.

(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, and Vsync is not input more than 90 ms typically.
As the display data are unstable in this period, the display maybe disordered. But the backlight works correctly even this period. So the backlight should be controlled by BRTC signal.

(3) The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

(4) Keep POWC signal “L” more than 200 ms after the power supply (V_{DD}) is input, if POWC signal is conrolled.

(5) Analog RGB inputs are independent from this power supply sequence.

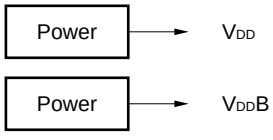
(6) Ripple of supply voltage

	V_{DD} (for logic and LCD driver)	$V_{DD}B$ (for backlight)
Acceptable range	≤ 100 mVp-p	≤ 200 mVp-p

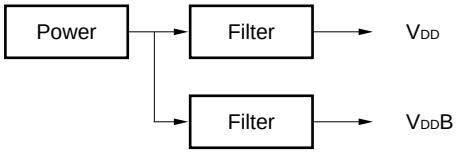
Note 1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

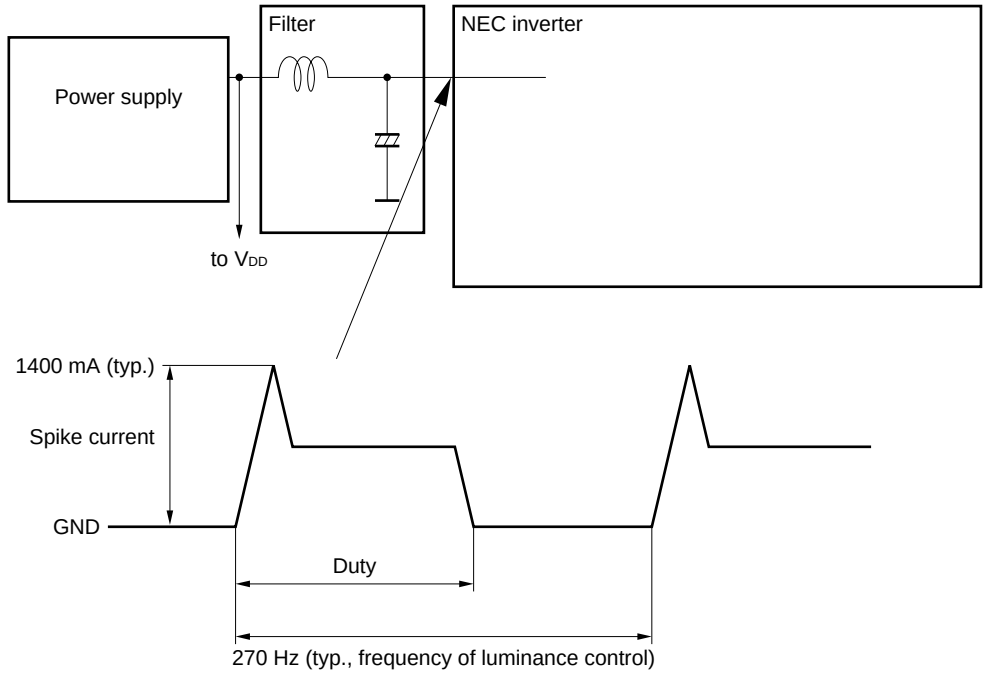
a) Separate the power supply



b) Put the filter



(7) Inverter current wave



In the maximum luminance, the inverter current is DC. However, in the luminance control by BRTP signal, the above duty varies 100% to 20% and the spike current, which causes the noise on the screen, may be observed. In this case, adjust the value of the capacitance in the above filter to eliminate the noise on the screen.

INTERFACE PIN CONNECTION

CN1

Part No. : MRF03-6R-SMT

Adaptable socket : MRF03-6P-1.27 (For cable type) or MRF03-6PR-SMT (For board to board type)

Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

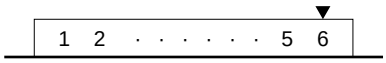
Coaxial cable : UL20537PF75VLAS

Supplier : HITACHI CO., LTD.

Note 1: A coaxial cable shield should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6▼	CLK

Figure from socket view



CN2

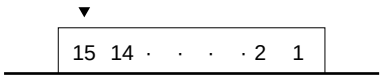
Part No. : IL-Z-15PL-SMTY

Adaptable socket : IL-Z-15S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V_{DD}	9	GND
2	V_{DD}	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15▼	GND
8	CNTSTB		

Figure from socket view



Note 1: N.C. (No connection) must be open.

CN3

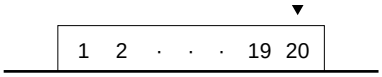
Part No. : DF14A-20P-1.25H

Adaptable socket : DF14-20S-1.25C

Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Pin No.	Symbol	Pin No.	Symbol
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20▼	N.C.

Figure from socket view



CN201

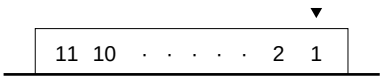
Part No. : IL-Z-11PL-SMTY

Adaptable socket : IL-Z-11S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V_{DD}B	7	ACA
2	V_{DD}B	8	BRTC
3	V_{DD}B	9	BRTH
4	GNDB	10▼	BRTL
5	GNDB	11	N.C.
6	GNDB		

Figure from socket view



Note 1: N.C. (No connection) must be open.

CN202

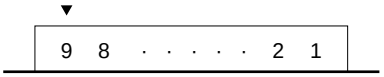
Part No. : IL-Z-9PL1-SMTY

Adaptable socket : IL-Z-9S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

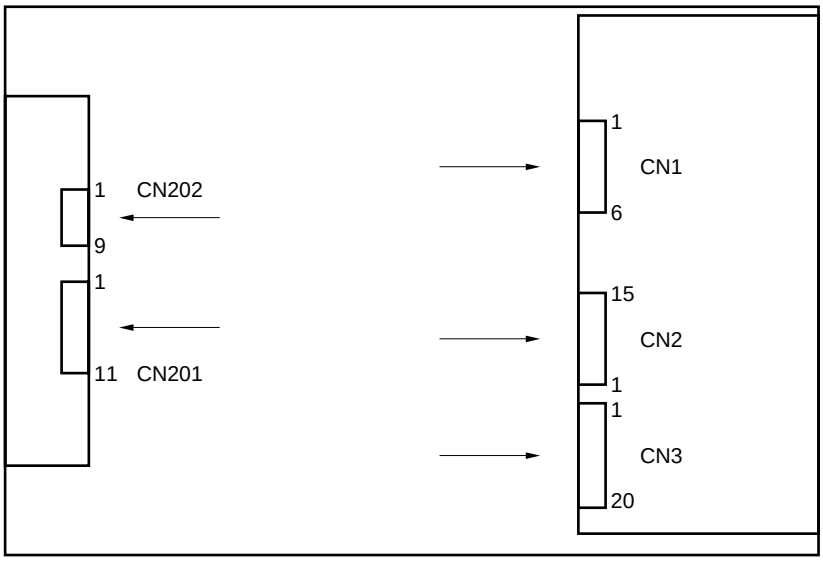
Pin No.	Symbol	Pin No.	Symbol
1	GNDB	6	BRTL
2	GNDB	7▼	BRTP
3	ACA	8	GNDB
4	BRTC	9	PWSEL
5	BRTH		

Figure from socket view



<Connector location>

Rear view



PIN FUNCTIONS

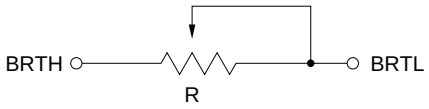
Symbol	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) Timing signal for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	–	Red video signal input (0.7 Vp-p, 75 Ω)
G	Input	–	Green video signal input (0.7 Vp-p, 75 Ω)
B	Input	–	Blue video signal input (0.7 Vp-p, 75 Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "open" : Logic and LCD powers are on. "L" : Logic and LCD powers are off. (Note 1)
CNTSEL	Input	–	Display control signal in case of serial communications. (TTL level) "H" or "Open": Default "L" : External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **FUNCTIONS**.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in **FUNCTIONS**.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in **FUNCTIONS**.
CPSEL	Input	–	Clamp function select signal (TTL level) "H" or "Open": Default "L" : CLAMP signals is possible. (External control)
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L."
ACA	Input	Positive	Luminance control signal (TTL level) "H" or "Open": Normal luminance "L" : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal (TTL level) "H" or "Open": Backlight on "L" : Backlight off
BRTH	Input	–	Backlight luminance control-1 Variable resistor control (Note 2) or voltage control (Note 3) These controls work in BRTP = "Open."
BRTL	Input	–	
BRTP	Input	–	Backlight luminance control-2 (TTL level) BRTP signal control (Note 4)
PWSEL	Input	–	Luminance control select signal (TTL level) "H" or "Open": Variable resistor control or voltage control "L" : BRTP signal control
ADJSEL	Input	Positive	Contrast, brightness control signal (TTL level) "H" or "Open": Default "L" : External control Serial communications are set up by external control.
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTDAT is mentioned in **OSD FUNCTIONS**.
OSDRI	Input	–	OSD Red input (TTL level) Detail of CNTDAT is mentioned in **OSD FUNCTIONS**.
OSDGI	Input	–	OSD Green input (TTL level) Detail of CNTDAT is mentioned in **OSD FUNCTIONS**.

Symbol	I/O	Logic	Description
OSDBI	Input	–	OSD Blue input (TTL level) Detail of CNTDAT is mentioned in **OSD FUNCTIONS**.
OSDENI	Input	Positive	OSD enable signal (TTL level) Detail of CNTDAT is mentioned in **OSD FUNCTIONS**.
V_{DD}	–	–	V_{DD} (+12 V ± 5%) power supply for logic and LCD driving
$V_{DD}B$	–	–	$V_{DD}B$ (+12 V ± 5%) power supply for backlight
GND	–	–	Signal ground for logic/LCD driving (V_{CC}, V_{DD}) (Connect to a system ground.)
GNDB	–	–	Ground for backlight (VDDB) GNDB is not connected the module GND (FG).

Note 1: When POWC is “L”, serial communication data is clear, please set again. When POWC is “L”, logic input signal has to be all “0 V”. If more than “0.3 V” is inputted, inside circuit of the LCD module may be broken.

Note 2: The way of luminance control by a variable resistor

This way works in PWSEL = “H” or “Open” and in BRTP = “Open”. The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor correspond to the minimum of luminance.



Mating variable resistor:
10 kΩ ± 5%, B curve

Maximum luminance (100%): R = 10 kΩ
Minimum luminance (30%; ACA = “H”, 60%; ACA = “L”): R = 0 Ω

Note 3: The way of luminance control by voltage

This way works in PWSEL = “H” or “Open” and in BRTP = “Open”. If luminance is controlled by BRTH/BRTL input voltage, at first BRTH is “0 V”, and BRTL input voltage controls luminance. When BRTL input voltage is “1 V”, the luminance become maximum, and when BRTL input voltage is “0 V”, the luminance become minimum.

Maximum luminance (100%): BRTL = “1 V”
Minimum luminance (30%; ACA = “H”, 60%; ACA = “L”): BRTL = “0 V”

Note 4: The way of luminance control by BRTP signal

Refer to **OUTSIDE CONTROL FOR LUMINANCE**.

FUNCTIONS

This LCD module has following functions by serial data input (table 1):

(1) Expansion mode: See table 2 and **EXPANSION FUNCTIONS**
(2) Control Display position (VERTICAL): See table 3.
(3) Control Display position (HORIZONTAL): See table 6.
(4) Control CLK delay: See table 4.
(5) Change CLK fall/rise synchronous: See table 5.
(6) Contrast control:
(7) Sub-Contrast control:
(8) Sub-Brightness control:

} See table 9, 10 and **COLOR CONTROL FUNCTIONS AND GRAPH IMAGE**

Set up the following items to work the above functions

(A) CLK counts of horizontal period: See table 7.
(B) CLK frequency range: See table 8.

HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is “L”, the above functions ((1) – (5)) are valid. (CNTSEL is “H” or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions ((1) – (5)) are effective.

If ADJSEL is “L”, the above functions ((6) – (8)) are valid. (ADJSEL is “H” or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB2. Once, the data is latched, the above functions ((6) – (8)) are effective.

Please keep CNTSTB/2 to be “L” during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

Table 1. CNTDAT (Serial data) Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DALAY5	CLK delay	
D17	DALAY4	CLK delay	
D18	DALAY3	CLK delay	
D19	DALAY2	CLK delay	
D20	DALAY1	CLK delay	
D21	DALAY0	CLK delay (LSB)	
D22	CKS	CLK signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK counts of horizontal period (MSB)	See table 7
D33	HSE9	CLK counts of horizontal period	
D34	HSE8	CLK counts of horizontal period	
D35	HSE7	CLK counts of horizontal period	
D36	HSE6	CLK counts of horizontal period	
D37	HSE5	CLK counts of horizontal period	
D38	HSE4	CLK counts of horizontal period	
D39	HSE3	CLK counts of horizontal period	

DATA	DATA name	Function	
D40	HSE2	CLK counts of horizontal period	See table 7
D41	HSE1	CLK counts of horizontal period	
D42	HSE0	CLK counts of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	
AD0	DAD0	Color adjust data (LSB)	See table 9
AD1	DAD1	Color adjust data	
AD2	DAD2	Color adjust data	
AD3	DAD3	Color adjust data	
AD4	DAD4	Color adjust data	
AD5	DAD5	Color adjust data	
AD6	DAD6	Color adjust data	
AD7	DAD7	Color adjust data (MSB)	
AD8	DAA3	Color adjust select data (MSB)	See table 10
AD9	DAA2	Color adjust select data	
AD10	DAA1	Color adjust select data	
AD11	DAA0	Color adjust select data (LSB)	

Table 2. Expansion mode (VEX3 to VEX0 : 4 bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	SXGA	Standard Note 1
0	0	0	1	1.25	XGA	See **DISPLAY IMAGES**.
0	0	1	0	1.6	SVGA, MAC	
0	0	1	1	2.0	VGA	
0	1	0	0	2.5	VGA-TEXT	
0	1	0	1	–	Prohibit	
0	1	1	0	–	Prohibit	
0	1	1	1	–	Prohibit	
1	0	0	0	1.1	SUN	
1	0	0	1	–	Prohibit	
1	0	1	0	–	Prohibit	
1	0	1	1	–	Prohibit	
1	1	0	0	–	Prohibit	
1	1	0	1	–	Prohibit	
1	1	1	0	–	Prohibit	
1	1	1	1	–	Prohibit	

Note 1: Display mode is SXGA, when CNTSEL is “H” or “open.”

Table 3. Vertical display position (VD10 to VD0 : 11 bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] **note 1**
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 **note 2**

Note 1: The number of horizontal line between Vsync-fall and RGB data valid.

Note 2: The maximum number is based on horizontal line count of the display mode.

Note 3: Vertical position is fixed at 41 H, when CNTCEL is “H” or “open”.

Table 4. CLK delay (DELAY6 to DELAY0 : 7 bit)

DELAY [6..0]	Delay	Unit	DELAY [6..0]	Delay	Unit	DELAY [6..0]	Delay	Unit
00H	0	ns	28H	12.53	ns	50H	25.16	ns
01H	0.36	ns	29H	12.84	ns	51H	25.47	ns
02H	0.67	ns	2AH	13.15	ns	52H	25.78	ns
03H	0.98	ns	2BH	13.46	ns	53H	26.09	ns
04H	1.32	ns	2CH	13.8	ns	54H	26.43	ns
05H	1.63	ns	2DH	14.11	ns	55H	26.74	ns
06H	1.95	ns	2EH	14.43	ns	56H	27.06	ns
07H	2.27	ns	2FH	14.74	ns	57H	27.37	ns
08H	2.52	ns	30H	15.04	ns	58H	27.63	ns
09H	2.83	ns	31H	15.35	ns	59H	27.94	ns
0AH	3.14	ns	32H	15.66	ns	5AH	28.25	ns
0BH	3.45	ns	33H	15.96	ns	5BH	28.56	ns
0CH	3.79	ns	34H	16.31	ns	5CH	28.9	ns
0DH	4.1	ns	35H	16.61	ns	5DH	29.22	ns
0EH	4.42	ns	36H	16.93	ns	5EH	29.55	ns
0FH	4.73	ns	37H	17.25	ns	5FH	29.87	ns
10H	5	ns	38H	17.52	ns	60H	30.18	ns
11H	5.31	ns	39H	17.83	ns	61H	30.49	ns
12H	5.62	ns	3AH	18.14	ns	62H	30.8	ns
13H	5.93	ns	3BH	18.45	ns	63H	31.11	ns
14H	6.27	ns	3CH	18.79	ns	64H	31.45	ns
15H	6.58	ns	3DH	19.1	ns	65H	31.76	ns
16H	6.9	ns	3EH	19.42	ns	66H	32.08	ns
17H	7.22	ns	3FH	19.74	ns	67H	32.39	ns
18H	7.5	ns	40H	19.97	ns	68H	32.69	ns
19H	7.81	ns	41H	20.29	ns	69H	32.99	ns
1AH	8.12	ns	42H	20.63	ns	6AH	33.3	ns
1BH	8.43	ns	43H	20.94	ns	6BH	33.61	ns
1CH	8.77	ns	44H	21.28	ns	6CH	33.95	ns
1DH	9.08	ns	45H	21.58	ns	6DH	34.26	ns
1EH	9.41	ns	46H	21.91	ns	6EH	34.58	ns
1FH	9.72	ns	47H	22.24	ns	6FH	34.91	ns
20H	10.03	ns	48H	22.58	ns	70H	35.17	ns
21H	10.35	ns	49H	22.91	ns	71H	35.48	ns
22H	10.67	ns	4AH	23.25	ns	72H	35.79	ns
23H	10.99	ns	4BH	23.55	ns	73H	37.06	ns
24H	11.32	ns	4CH	23.9	ns	74H	36.44	ns
25H	11.63	ns	4DH	24.2	ns	75H	36.74	ns
26H	11.95	ns	4EH	24.52	ns	76H	37.06	ns
27H	12.28	ns	4FH	24.87	ns	77H	37.38	ns

DELAY [6..0]	Delay	Unit
78H	37.67	ns
79H	37.98	ns
7AH	38.29	ns
7BH	38.6	ns
7CH	38.94	ns
7DH	39.25	ns
7EH	39.57	ns
7FH	39.86	ns

Note 1: DELAY [6..0] is fixed at 00H, when CNTSEL is “H” or “open”.

Note 2: This delay value is typical value at Ta = 25°C. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

<1> Variation of CLK delay by temperature drift. (only reference) The temperature constant of CLK delay is 0.2%/°C.

Calculated example:

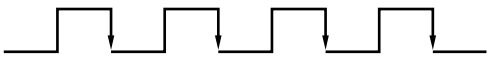
In case of delay time is 20ns at Ta = 25°C;

(a) In case Ta rising to 50°C.
Increase of delay time → (50°C - 25°C) × 0.002 × 20 ns = +1 ns
So, the total delay time is 21 ns at Ta = 50°C.

(b) In case Ta falling to 0°C.
Decrease of delay time → (0°C - 25°C) × 0.002 × 20 ns = –1 ns
So, the total delay time is 19 ns at Ta = 0°C

<2> Variation of CLK delay time against each LCD module. (Only reference)
–10.5% to +14.4%

Table 5. CLK reverse signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK. 
1	DATA is sampled on falling edge of CLK. 

Note 1: CKS is “0”, when CNTSEL is “H” or “open.”

Table 6. Horizontal display position (HD8 to HD0 : 9 bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] **Note 1**
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Note 1: The number of CLK between Hsync-fall and RGB data valid.

Note 2: Horizontal position is set at 360 CLK, when CNTSEL is “H” or “open”.

Table 7. CLK counts of horizontal period (HSE10 to HSE0 : 11bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count **Note 1**
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Note 1: The number of CLK between Hsync signals.

Note 2: CLK number is set 1688 CLK, when CNTSEL is “H” or “open”.

Note 3: If setting value is different from actual input signal, it causes to malfunction.

Table 8. CLK frequency select (MOD1 to MOD0 : 2 bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	90 to 135
0	1	65 to 90
1	0	50 to 65
1	1	20 to 50

Note 1: Set complying with input CLK frequency.

Note 2: CLK frequency is set 90 to 135 MHz, when CNTSEL is “H” or “open”.

Table 9. Color control data (DAD7 to DAD0 : 8 bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	Adjusting value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Note 1: Adjust value for selecting function above table. 10.

Note 2: Different D/A-range depends on function selected.

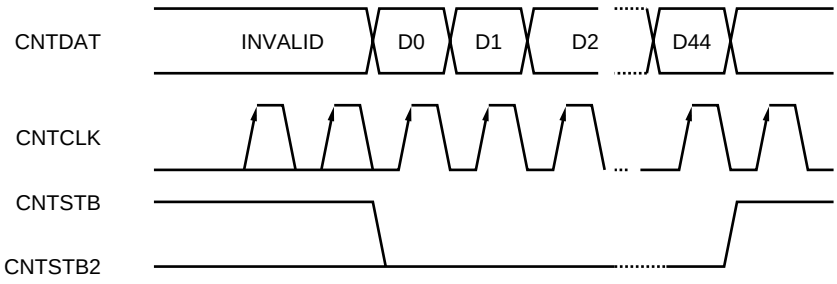
Note 3: See more detail **Color control function and graph image**.

Table 10. Color adjust select data (DAA3 to DAA0 : 4 bit)

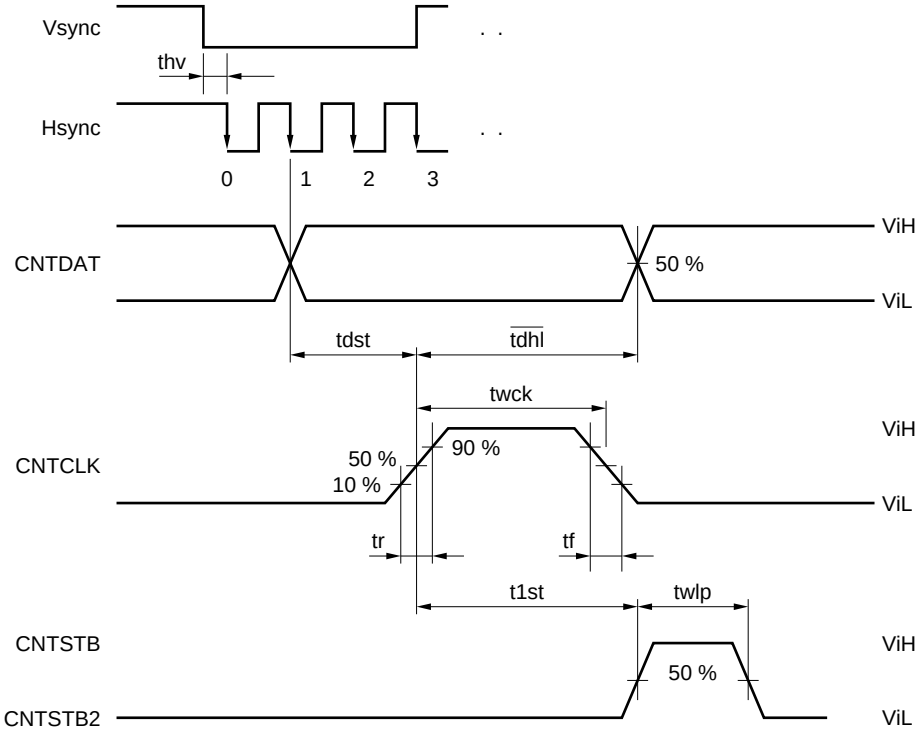
DAA3	DAA2	DAA1	DAD0	Function
0	0	0	0	Prohibit
0	0	0	1	Main contrast
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

Note 1: See more detail **Color control function and graph image**.

SERIAL COMMUNICATION TIMINGS



Parameters	Symbols	Min.	Max.	Unit	Remark
CLK pulse-width	twck	50	–	ns	CNTCLK
CLK frequency	fclk	–	5	MHz	
DATA set-up-time	tdst	50	–	ns	CNTDAT
DATA hold-time	tdhl	50	–	ns	
Latch pulse-width	twlp	50	–	ns	CNTSTB CNTSTB2
Latch set-up-time	t1st	50	–	ns	
Rise/fall time	tr, tf	–	50	ns	CNT xxx



EXPANSION FUNCTION

(1) How to use expansion mode

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 2.0 times vertically and horizontally,VGA screen image can be displayed fully on the screen of SXGA resolution.

This LCD module has the function that expands vertical direction as shown in the following table. And expanding horizontal direction is possible by setting input CLK frequency equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

Please adopt this mode after evaluating display quality, because the appearance in the expansion mode is happened to be relatively bad in some cases.

The followings show the display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal **Note**
SXGA	1280 × 1024	1	1
XGA	1024 × 768	1.25	1.25
SVGA	800 × 600	1.6	1.6
VGA	640 × 480	2.0	2.0
VGA text	720 × 400	2.5	1.7
MAC	832 × 624	1.6	1.5
SUN	1152 × 900	1.1	1.1

Note The horizontal magnification multiples the input clock (CLK).
Input CLK = system CLK × horizontal magnification.

Example In case of SXGA and VGA, CLK frequency can be decided as follows.
SXGA: (system CLK (108.0 MHz)) × 1.0 = 108.0 MHz.
VGA : (system CLK (25.175 MHz)) × 2.0 = 50.35 MHz.

(2) Setting serial data for expansion

Input signal								Module serial-data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count Number [CLK]	DSP [CLK]	Count Number [H]	DSP [H]	Calculation formula		
				(A)	(B)	–	(C)	(A) × Ver.magni	(B) × Hor.magni	= (C)
SXGA (1280 × 1024)	108.0	63.981	60.02	1688	360	1066	41	(A) × 1	(B) × 1	
	117.0	71.691	67.189	1632	336	1067	41			
	125.0	75.120	71.204	1664	352	1055	28			
	130.076	76.968	72.000	1690	378	1069	42			
	135.0	78.125	72.005	1728	384	1085	58			
	135.0	79.976	75.025	1688	392	1066	41			
XGA (1024 × 768)	65*	48.363	60.004	1344	296	806	35	(A) × 1.25	(B) × 1.25	
	75*	56.476	70.069	1328	280	806	35			
	78.75*	60.023	75.029	1312	272	800	31			
MAC (832 × 624)	57.283*	49.725	74.5	1152	288	667	42	(A) × 1.5	(B) × 1.5	
SVGA (800 × 600)	36*	35.156	56.25	1024	200	625	24	(A) × 1.6	(B) × 1.6	= (C)
	40*	37.879	60.317	1056	216	628	27			
	50*	48.077	72.188	1040	184	666	29			
	49.5*	46.875	75	1056	240	666	24			
VGA (640 × 480)	25.175*	31.469	59.94	800	144	525	35	(A) × 2.0	(B) × 2.0	
	31.5*	37.861	72.809	832	168	520	31			
	31.5*	37.5	75	840	184	500	19			
	30.24*	35.0	66.667	864	160	525	42			
VGA text (720 × 400)	28.322*	31.469	70.087	900	153	449	37	(A) × 1.7	(B) × 1.7	
SUN (1152 × 900)	94.500*	61.845	66.003	1528	336	937	35	(A) × 1.1	(A) × 1.1	

*: Standard timings (Please set them up properly for correct expansion).

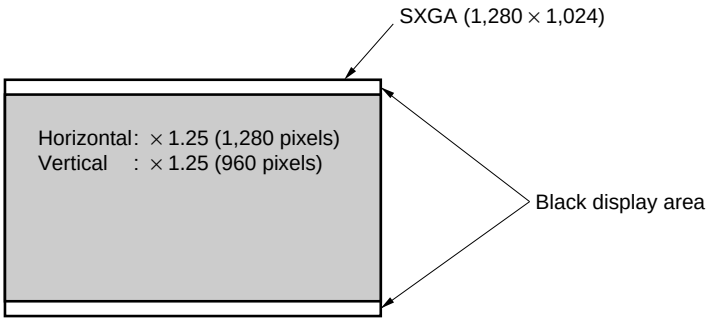
Note 1. DSP = Display Start Period. DSP is total of “pulse-width” and “back-porch”.

2. HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

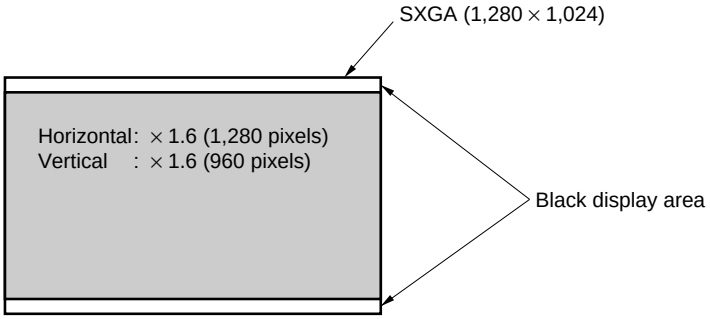
3. The pulse-width of Hsync, Vsync and Back-porch are the same as SXGA-mode (Standard-mode).

(3) Display Image

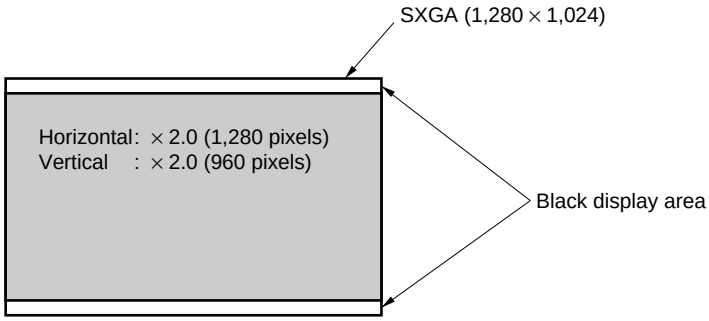
1. XGA mode (1024 × 768)



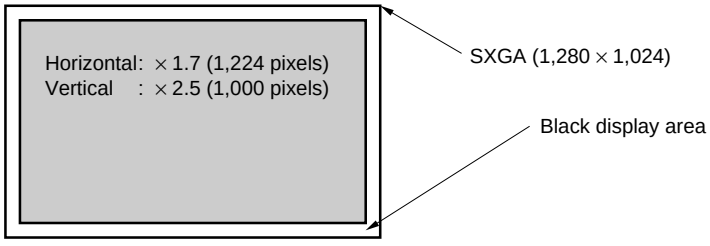
2. SVGA mode (800 × 600)



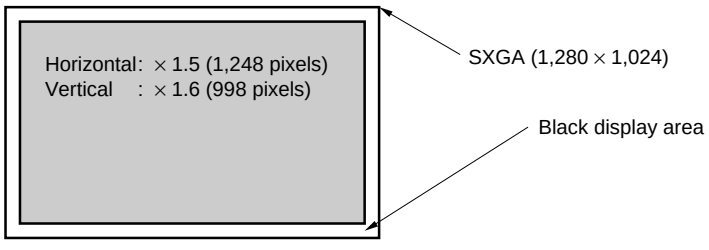
3. VGA mode (640 × 480)



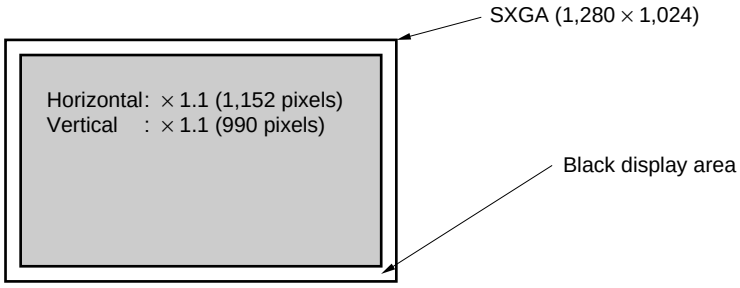
4. VGA text mode (720 × 400)



5. 832 × 624 MAC mode (832 × 624)



6. SUN mode (1152 × 900)



COLOR CONTROL FUNCTION AND GRAPH IMAGE

This LCD module can adjust the following functions by serial data input (table. 1)

(1) Main contrast :
(2) Sub-contrast each R, G, B :
(3) Sub-brightness each R, G, B :

} See table 9, 10 and **COLOR CONTRAOL FUNCTION AND GRAPH IMAGE**

(1) Main contrast

Main contrast is adjusted R/G/B contrast at the same time. Contrast controls the amplitude of input video signal.

Default value: 128, Valid range: 78 to198
Contrast minimum : 198
Contrast maximum : 78
ADJSEL = “H” or “Open”: Maincontrast = 128

(2) Sub-contrast R, G, B

Sub-contrast can adjust each R/G/B, Contrast controls the amplitude of input video signal.

Default value: 128, Valid range: 78 to198
Contrast minimum : 198
Contrast maximum: 78
ADJSEL = “H” or “Open”: Maincontrast = 128

(3) Sub-brightness R, G, B

Sub-brightness can adjust each R/G/B. Brightness adjusts the black level of input video signal.

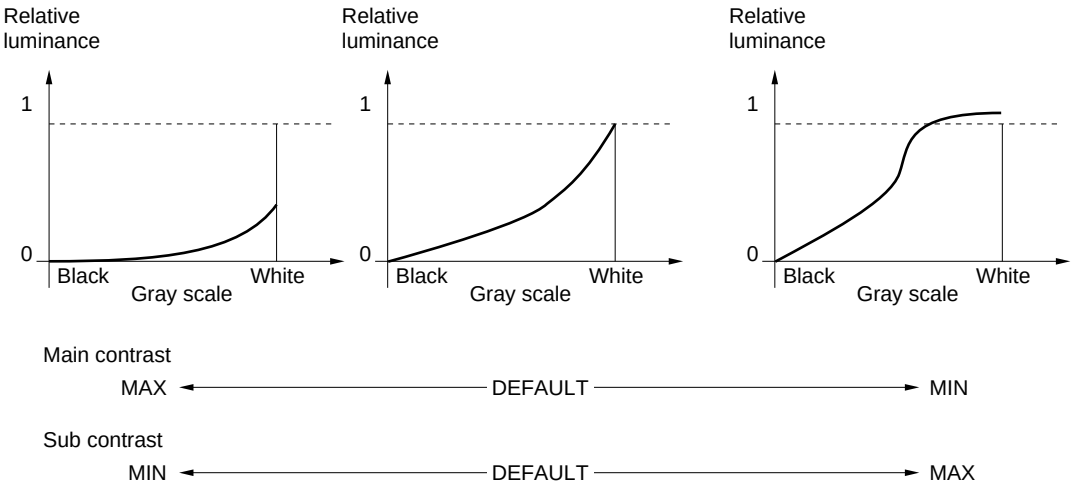
Default value: 128, Valid range: 55 to163
Brightness minimum : 55
Brightness maximum: 163
ADJSEL = “H” or “Open”: Maincontrast = 128

Note 1: If use to go over above valid range, LCD module will not be destroyed. However LCD will be inferiority. Please keep value of valid range.

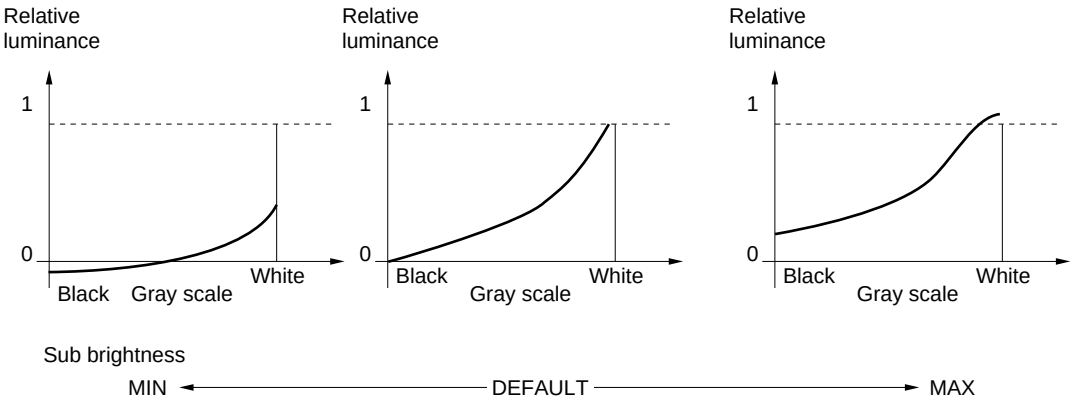
Note 2: Although set up the same value for each LCD, color will be caused the different. And also, will be afraid to deviate values from optical characteristics. Please adopt this functions evaluating display quality.

GRAPH IMAGE

- Main contrast & Sub contrast



- Sub brightness



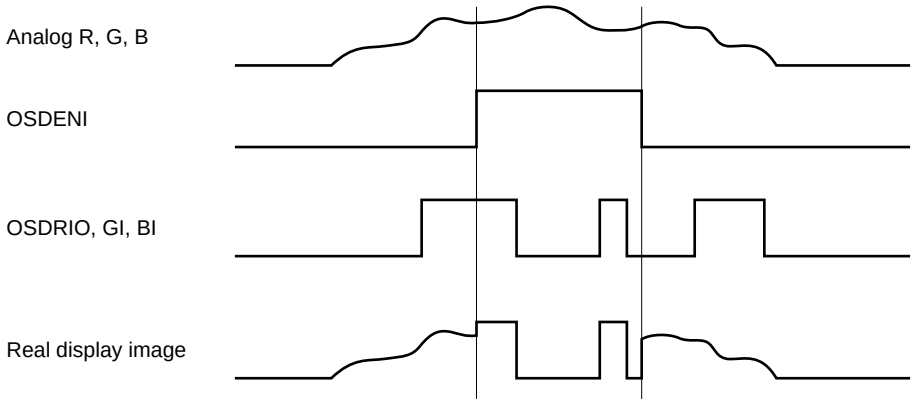
OSD FUNCTION

OSD (On Screen Display) is the function to display the other digital data on the input analog input data.
Possible to display 1 bit data for each R/G/B color (8 colors). OSD valid for the period of OSDENI

OSDRI, OSDGI, OSDBI: digital data for OSD
OSDENI = “H” : OSD signal is valid
OSDENI = “L” : OSD signal is not valid

OSD is the sub-display for function-control and the display quality will be not guaranteed. Please adopt the OSD image evaluating display quality.

OSD image



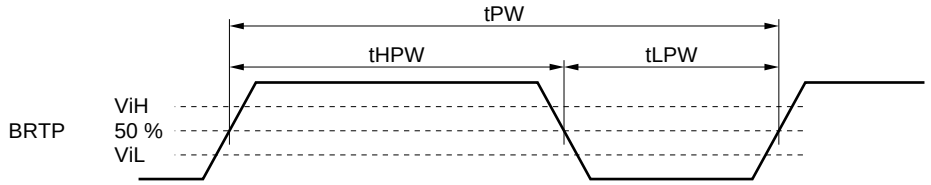
OUTSIDE CONTROL FOR LUMINANCE

Outside control is valid, when PWSEL = “L” and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.

Duty = 100%: luminance is maximum.

Duty = 20% : luminance is minimum.

Timing for BRTP



Parameters	Symbols	Min.	Typ.	Max.	Unit	Remark
Frequency	L/tPW	185	–	340	Hz	–
OFF section	tLPW	–	–	50	Ms	When tLPW is more than 50ms, the lamps are turned off.
Pulse-width	tHPW/tPW	20	–	100	%	At max. luminance (100%)
Input voltage	ViL	0	–	0.6	V	–
	ViH	4.5	–	5.25	V	–

Regarding setup for frequency, please refer to the below method.

Setup frequency = Vsync frequency × (n + 0.25) or (n + 0.75)

Please adopt the frequency evaluating the display quality, because the display will be disturbed depending on the frequency.

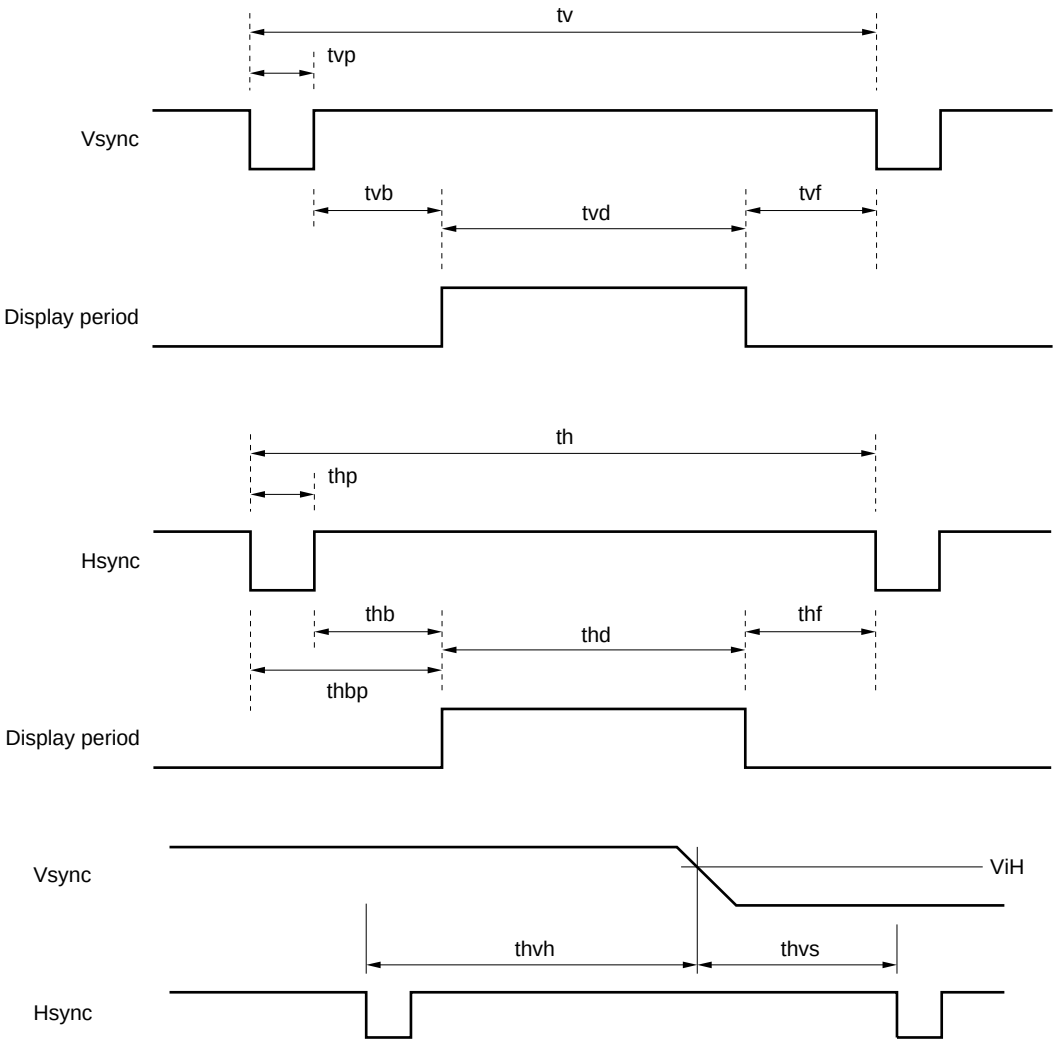
INPUT SIGNAL TIMINGS

(1) SXGA Mode (Standard)

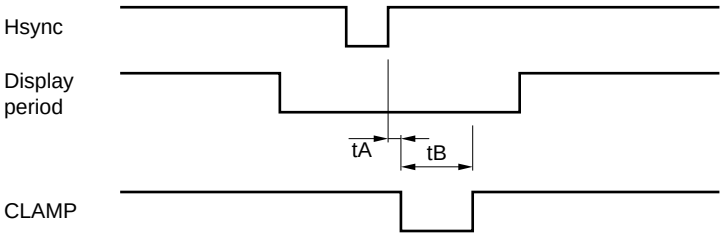
Name		Symbol	Min.	Typ.	Max.	Unit	Remark
CLK	Frequency	1/tc	95.0 –	108.0 9.3	135.0 –	MHz ns	SXGA standard
	Rise/Fall	tcrf	–	–	10	ns	–
	Pulse-width	tc/tcl	0.4	0.5	0.6	–	–
Hsync	Period	th	12.3 –	15.630 1688	17.0 –	μs CLK	63.981 kHz (typ.)
	Display	thd	– –	11.852 1280	– –	μs CLK	–
	Front-porch	thf	– 10	0.444 48	– –	μs CLK	–
	Pulse-width	thp	– 16	1.037 112	– –	μs CLK	–
	Back-porch	thb	1.0 94	2.296 248	– –	μs CLK	**Note 1**
	Pulse-width +Back-porch	thbp	1.8	–	–	μs	–
	V-Hsync timing hold/setup time	thvh	4	–	–	CLK	–
		thvs	1	–	–	CLK	–
	Rise/Fall	thrf	–	–	10	ns	–
Vsync	Period	tv	13.3 –	16.661 1066	18.5 –	ms H	60.020 Hz (typ.)
	Display	tvd	– –	16.005 1024	– –	ms H	–
	Front-porch	tvf	– 1	0.016 1	– –	ms H	–
	Pulse-width	tvp	– 2	0.047 3	– –	ms H	–
	Back-porch	tvb	– 5	0.594 38	– –	ms H	–

Note 1: Minimum value of Back-porch (thb) must be satisfied with both 1.0 μs and 94 CLK.

Note 2: Typical value should be set in default of CNTSEL input.
When CNTSEL is “H” or “Open”, display control mode is default.



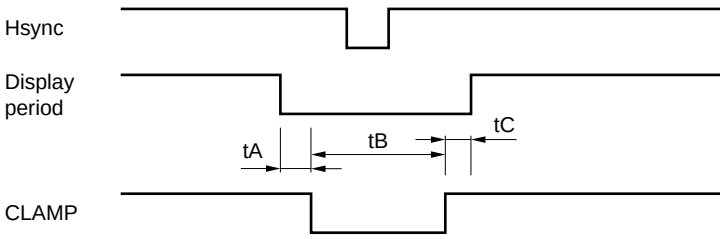
TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB [CLK]
0	0	2	41
0	1		27
1	0		20
1	1		15

Note 1: Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = “L”. If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

TIMING FOR INPUTTING CLAMP SIGNAL FROM OUTSIDE

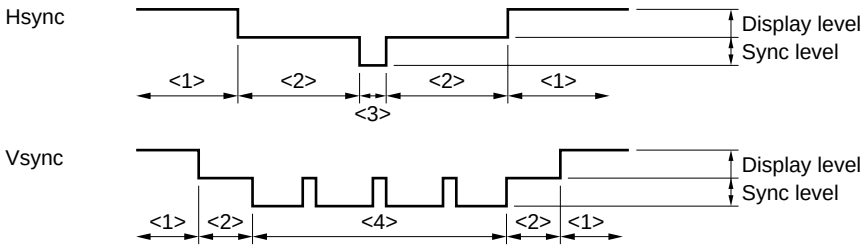


ITEMS	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	–	–	μs	–
tB	0.3	–	–	μs	–
tC	0.2	–	–	μs	–

Note 1: Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = “L”. If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

Note 2: Attention for using Sync On Green signal
Clamp signals must be input during black level period as next page.
If Clamp signals are input during other period, the display becomes un-uniformity.

Sync on Green input signal timings



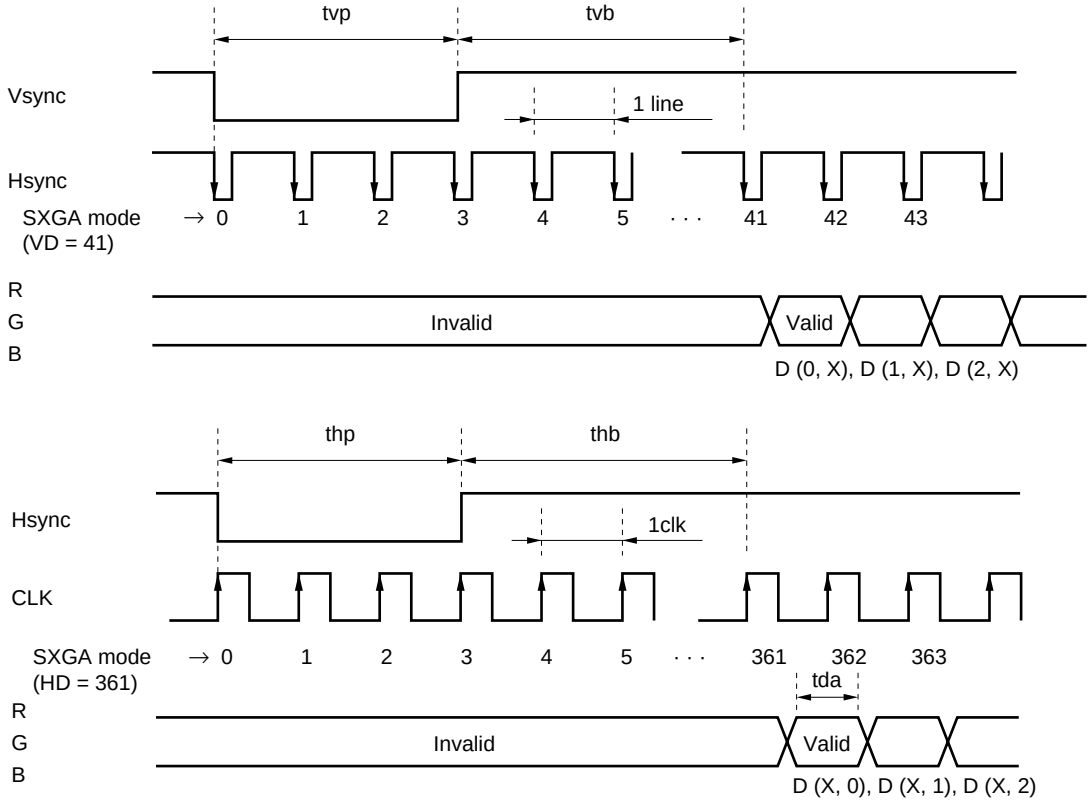
<1>: Display period <2>: Black level period <3>: Hsync period <4>: Vsync period

INPUT SIGNAL AND DISPLAY POSITION

(1) SXGA Standard Timing

Pixels

D (0, 0)	D (0, 1)	D (0, 2)	• • •	• • •	D (0, 1279)
D (1, 0)	D (1, 1)	D (1, 2)	• • •	• • •	D (1, 1279)
D (2, 0)	D (2, 1)	D (2, 2)	• • •	• • •	D (2, 1279)
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
D (1023, 0)	D (1023, 1)	D (1023, 2)	• • •	• • •	D (1023, 1279)



Note 1: The tda should be more than 4 ns.

OPTICAL CHARACTERISTICS

(T_a = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	γ = 2.2 viewing angle θR = 0°, θL = 0°, θD = 0° White/Black, at center	100	200	–	–	**Note 1**
Luminance	Lvmax	White, at center	150	200	–	cd/m^2	**Note 2**
Luminance uniformity	–	White	–	1.20	1.30	–	**Note 3**

Reference data

(T_a = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V)

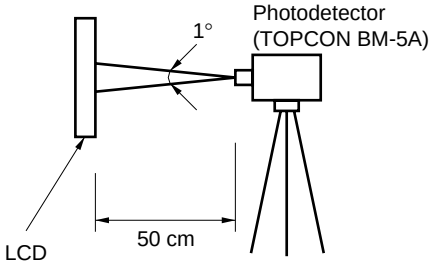
Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Best contrast ratio	CR	θR = 0°, θL = 0°, θU = 0°, θD = 10°		–	250	–	–	–
Viewing angle range	θR	CR > 10, θU = 0°, θD = 0°		50	60	–	deg.	**Note 4**
	θL			50	60	–	deg.	
	θU	CR > 10, θR = 0°, θL = 0°		35	50	–	deg.	
	θD			30	45	–	deg.	
Color gamut	C	θR = 0°, θL = 0°, θU = 0°, θD = 0°, at center, to NTSC		50	59	–	%	–
Response time	Ton	White 100% to Black 10%		–	7	12	ms	**Note 5**
Luminance control range	–	Maximum luminance: 100 %	ACA = H	–	30 to 100	–	%	–
			ACA = L	–	60 to 100	–		

Notes 1. The contrast ratio is calculated by using the following formula.

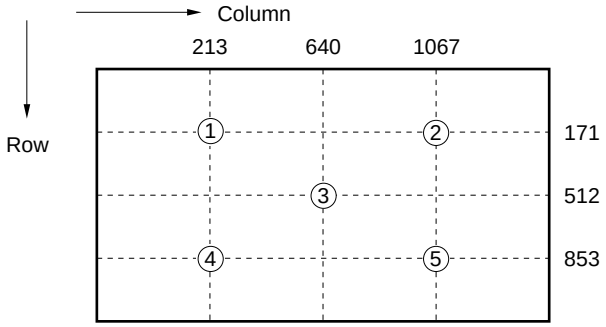
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in “white”}}{\text{Luminance with all pixels in “black”}}$$

The Luminance is measured in darkroom.

2. The luminance is measured after 20 minutes from the module works, with all pixels in white. Typical value is measured after luminance saturation.
Display mode: VESA SXGA - 75 Hz



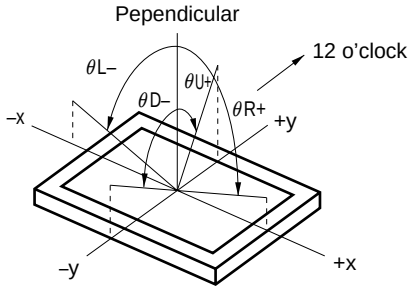
3. The luminance is measured at near the five points shown below.



Luminance uniformity is calculated using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

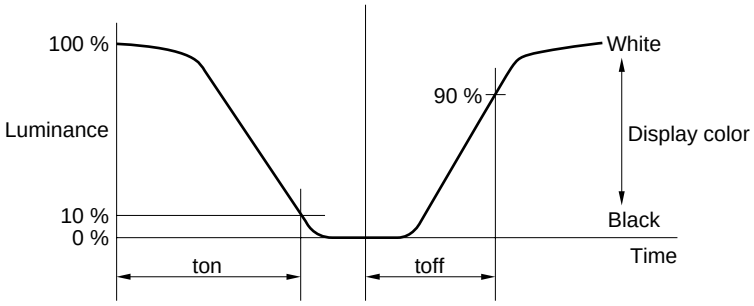
4. Definitions of viewing angle are as follows.



5. Definition of response time is as follows.

Photo-detector output signal is measured when the luminance changes “white” to “black”.

Response times are Ton and Toff of the photo-detector output amplitude. Ton is the time between 100 % and 10 %. Toff is the time between 0 % and 90 %.



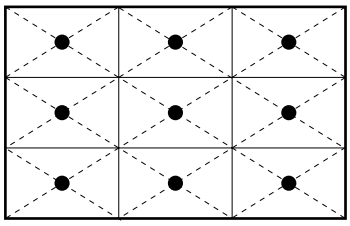
RELIABILITY TEST

Test item		Test condition
High temperature/humidity operation	**Note 1**	50 ± 2°C, 85% relative humidity 240 hours Display data is black.
Heat cycle (operation)	**Note 1**	<1> 0°C ± 3°C ⋯ 1 hour 55°C ± 3°C ⋯ 1 hour <2> 50 cycles, 4 hours/cycle <3> Display data is black.
Thermal shock (non-operation)	**Note 1**	<1> –20°C ± 3°C ⋯ 30 minutes 60°C ± 3°C ⋯ 30 minutes <2> 100 cycles <3> Temperature transition time within 5 minutes
Vibration (non-operation)	**Notes 1, 2**	<1> 5 - 100 Hz, 2G 1 minute/cycle X, Y, Z direction <2> 50 times each direction
Mechanical shock (non-operation)	**Notes 1, 2**	<1> 30 G, 11 ms X, Y, Z direction <2> 3 times each direction
ESD (operation)	**Notes 1, 3**	150 pF, 150 Ω, ±10 kV 9 places on a panel 10 times each place at one-second intervals
Dust (operation)	**Note 1**	15 kinds of dust (JIS Z 8901) Hourly 15 seconds stir, 8 times repeat

Notes 1. Display function is checked by the same condition as LCD module out-going inspection.

2. Physical damage.

3. Discharge points "●" are shown in the figure.



GENERAL CAUTIONS

Next figures and sentence are very important. Please understand these contents as follows.

 CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate

 CAUTION

 Do not touch an inverter, on which is stuck a caution label, while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module

a) Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

a) As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

b)  As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

c) As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

d) Do not pull the interface connectors in or out while the LCD module is operating.

e) Put the module display side down on that horizontal plane.

f) Handle connectors and cables with care.

g) When the module is operating, do not lose CLK, Hsync or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

h) Do not put front side (display surface side) of the module on a desk or a table for a long time, because the display may become un-uniformity.

i) The torque to mounting screw should never exceed 0.392 N·m (4 kgf·cm).

(3) Cautions for the atmosphere

a) Dew drop atmosphere must be avoided.

b) Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

c) This module uses cold cathod fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

d) Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

a) Do not apply fixed pattern data signal for a long time to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

b) This module has the retardation film, which may cause the variation of the color hue in the different viewing angles. The ununiformity may appear on the screen under the high temperature operation.

c) The noise from the inverter circuit may be observed in the luminance control mode. This is neither defects nor malfunctions.

(5) Other cautions

a) Do not disassemble and/or reassemble LCD module.

b) Do not readjust variable resistors or switches, etc.

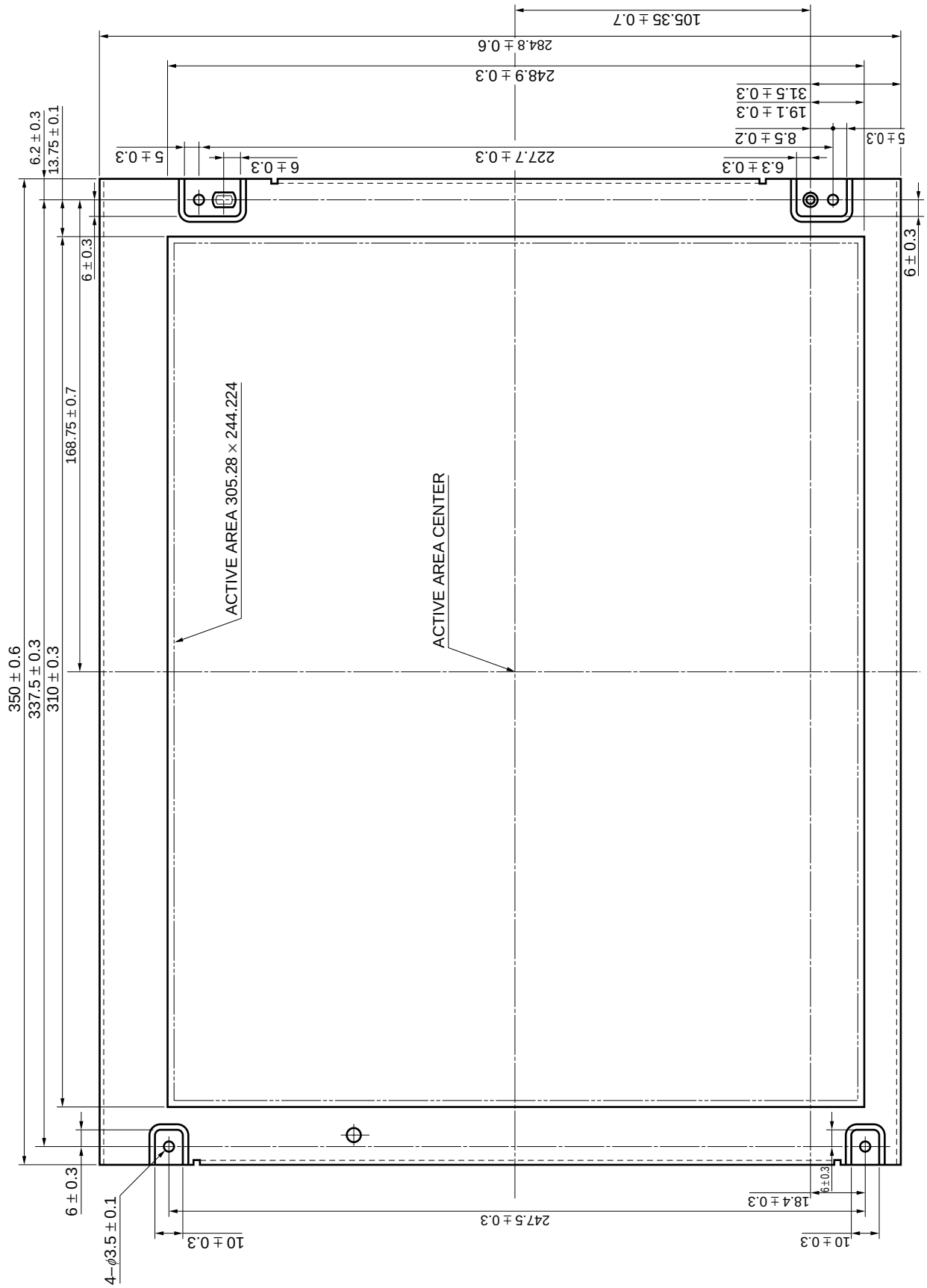
c) When returning the module for repair or etc, please pack the module not to be broken. We recommend the original shipping packages.

d) In case that the scan converter is used to convert VGA signal to NTSC, it is recommended using the frame-memory type, not the line-memory.

Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

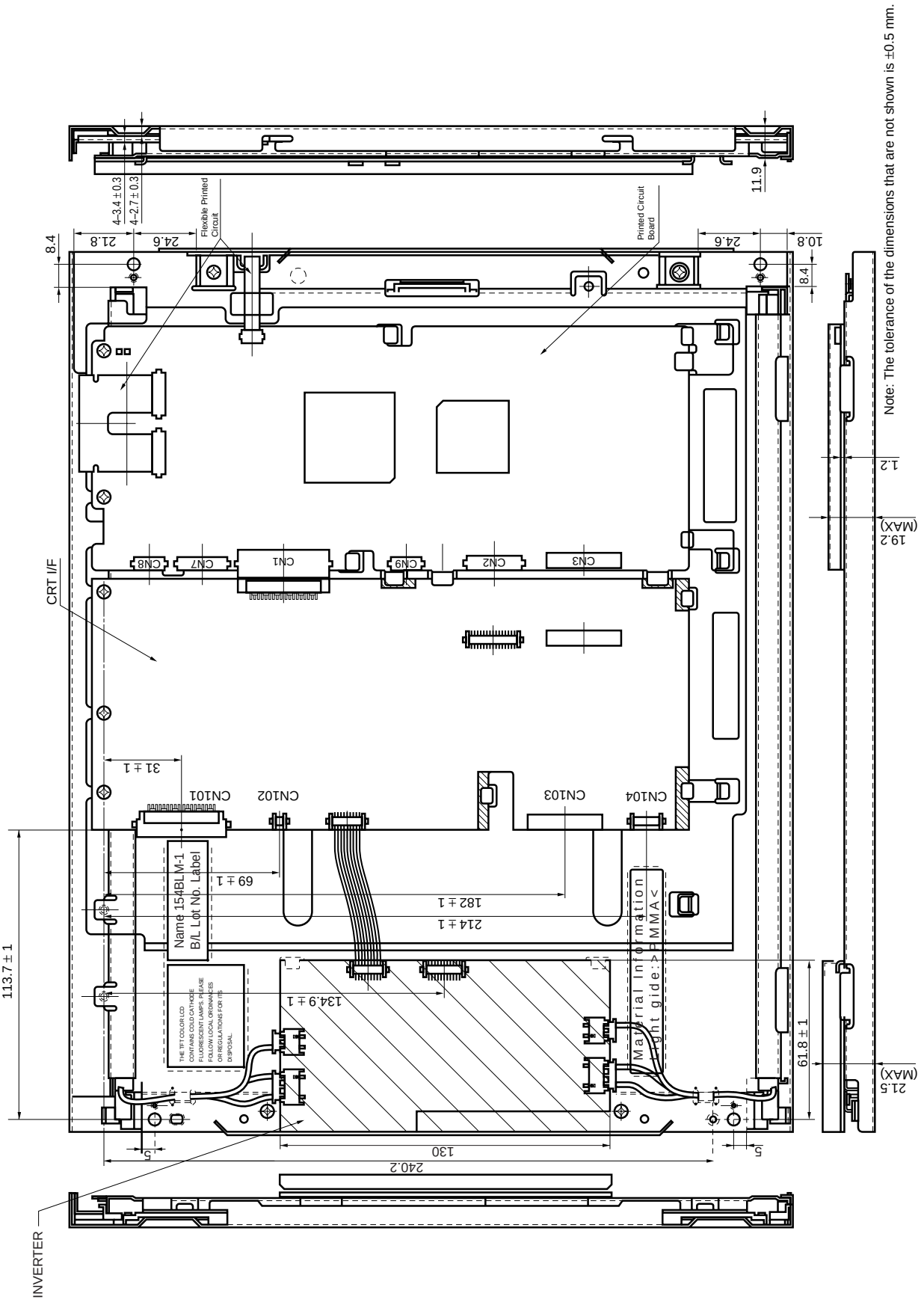
- The display condition of LCD module may be affected by the ambient temperature.
- The LCD module uses cold cathode tube for backlighting. Optical characteristics, like luminance or uniformity, will change during time.
- Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING: Front View (Unit: mm)



Remark The torque to mounting screw should never exceed 0.392 · Nm (4 kgf · cm).

OUTLINE DRAWING: Rear View (Unit: mm)



Remark The torque to mounting screw should never exceed 0.392 · Nm (4 kgf · cm).

[MEMO]