Data Sheet No. PD60174 Rev.D

International
IOR Rectifier

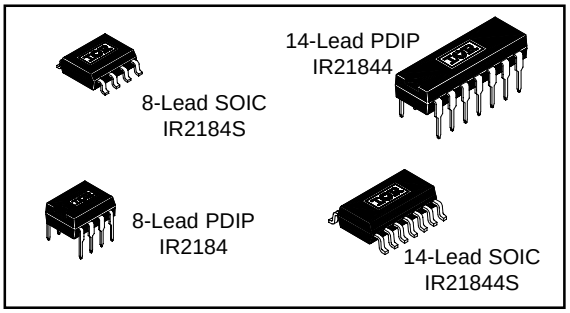
# IR2184(4)(S)

## HALF-BRIDGE DRIVER

## Features

- Floating channel designed for bootstrap operation
  - Fully operational to +600V
  - Tolerant to negative transient voltage
  - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A

## Packages



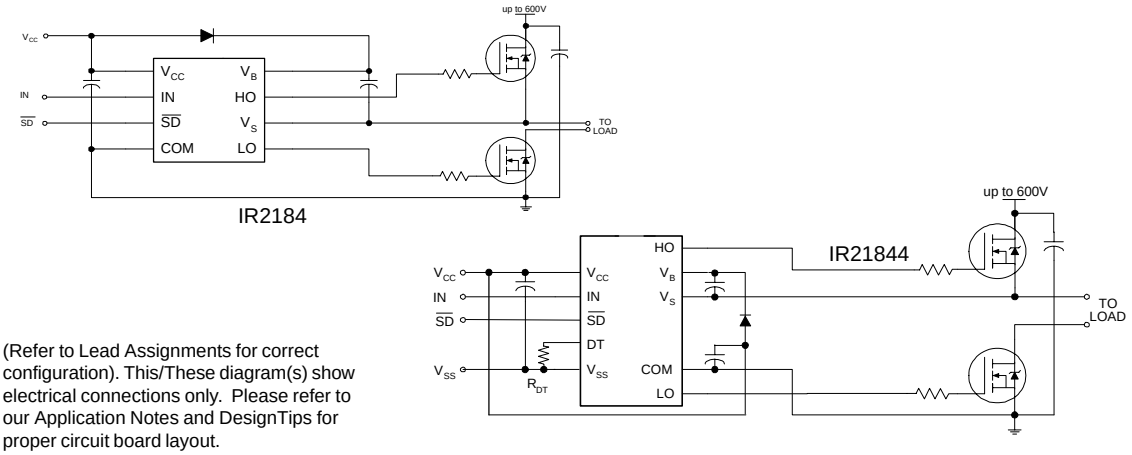

## Description

The IR2184(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

### IR2181/IR2183/IR2184 Feature Comparison

| Part | Input logic | Cross-conduction prevention logic | Dead-Time | Ground Pins | Ton/Toff |
|---|---|---|---|---|---|
| 2181 | HIN/LIN | no | none | COM | 180/220 ns |
| 21814 | | | | VSS/COM | |
| 2183 | HIN/$\overline{\text{LIN}}$ | yes | Internal 500ns | COM | 180/220 ns |
| 21834 | | | Program 0.4 ~ 5 us | VSS/COM | |
| 2184 | IN/$\overline{\text{SD}}$ | yes | Internal 500ns | COM | 680/270 ns |
| 21844 | | | Program 0.4 ~ 5 us | VSS/COM | |

## Typical Connection




(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High side floating absolute voltage | | -0.3 | 625 | V |
| $V_S$ | High side floating supply offset voltage | | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High side floating output voltage | | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Low side and logic fixed supply voltage | | -0.3 | 25 | |
| $V_{LO}$ | Low side output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| DT | Programmable dead-time pin voltage (IR21844 only) | | $V_{SS}$ - 0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic input voltage (IN & $\overline{SD}$) | | $V_{SS}$ - 0.3 | $V_{SS}$ + 10 | |
| $V_{SS}$ | Logic ground (IR21844 only) | | $V_{CC}$ - 25 | $V_{CC}$ + 0.3 | |
| $dV_S/dt$ | Allowable offset supply voltage transient | | — | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq +25°C$ | (8-lead PDIP) | — | 1.0 | W |
| | | (8-lead SOIC) | — | 0.625 | |
| | | (14-lead PDIP) | — | 1.6 | |
| | | (14-lead SOIC) | — | 1.0 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | (8-lead PDIP) | — | 125 | °C/W |
| | | (8-lead SOIC) | — | 200 | |
| | | (14-lead PDIP) | — | 75 | |
| | | (14-lead SOIC) | — | 120 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -50 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The $V_S$ and $V_{SS}$ offset rating are tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| VB | High side floating supply absolute voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High side floating supply offset voltage | Note 1 | 600 | |
| $V_{HO}$ | High side floating output voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Low side and logic fixed supply voltage | 10 | 20 | |
| $V_{LO}$ | Low side output voltage | 0 | $V_{CC}$ | |
| $V_{IN}$ | Logic input voltage (IN & $\overline{SD}$) | $V_{SS}$ | $V_{SS}$ + 5 | |
| DT | Programmable dead-time pin voltage (IR21844 only) | $V_{SS}$ | $V_{CC}$ | |
| $V_{SS}$ | Logic ground (IR21844 only) | -5 | 5 | |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

Note 1: Logic operational for $V_S$ of -5 to +600V. Logic state held for $V_S$ of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: IN and SD are internally clamped with a 5.2V zener diode.

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $V_{SS}$ = COM, $C_L$ = 1000 pF, $T_A$ = 25°C, DT = VSS unless otherwise specified.

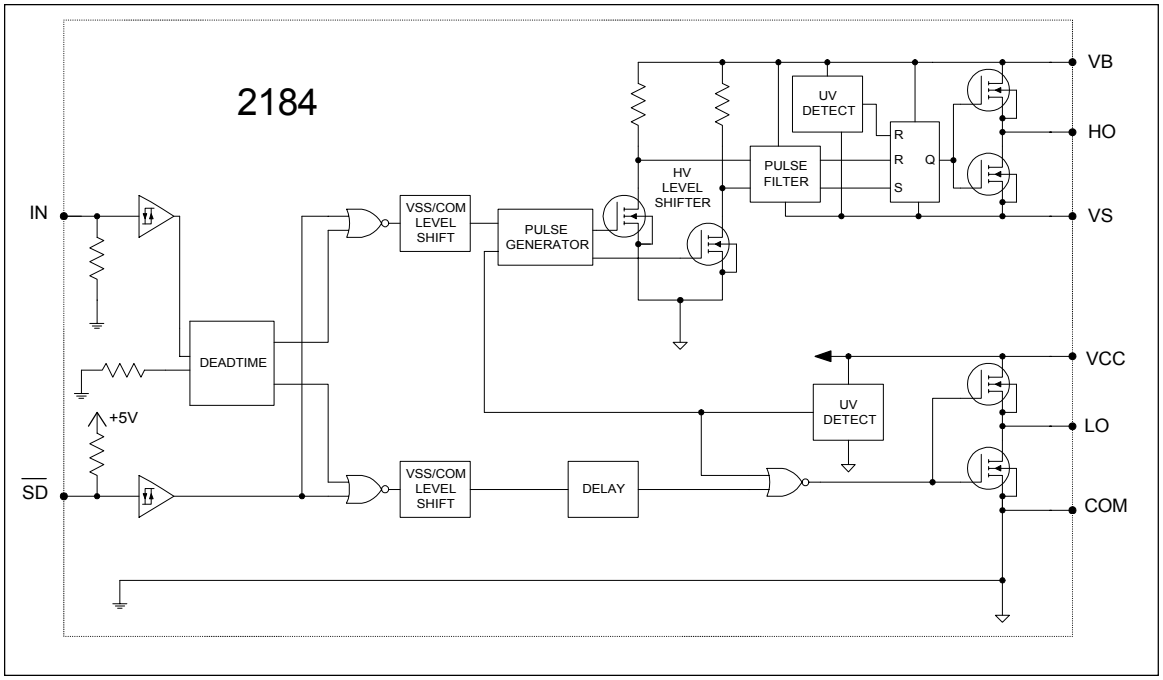
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | — | 680 | 900 | nsec | $V_S$ = 0V |
| $t_{off}$ | Turn-off propagation delay | — | 270 | 400 | | $V_S$ = 0V or 600V |
| $t_{sd}$ | Shut-down propagation delay | — | 180 | 270 | | |
| MTon | Delay matching, HS & LS turn-on | — | 0 | 90 | | |
| MToff | Delay matching, HS & LS turn-off | — | 0 | 40 | | |
| $t_r$ | Turn-on rise time | — | 40 | 60 | | $V_S$ = 0V |
| $t_f$ | Turn-off fall time | — | 20 | 35 | | $V_S$ = 0V |
| DT | Deadtime: LO turn-off to HO turn-on($DT_{LO-HO}$) & | 280 | 400 | 520 | | RDT= 0 |
| | HO turn-off to LO turn-on ($DT_{HO-LO}$) | 4 | 5 | 6 | µsec | RDT = 200k |
| MDT | Deadtime matching = $DT_{LO\ -\ HO}$ - $DT_{HO-LO}$ | — | 0 | 50 | nsec | RDT=0 |
| | | — | 0 | 600 | | RDT = 200k |

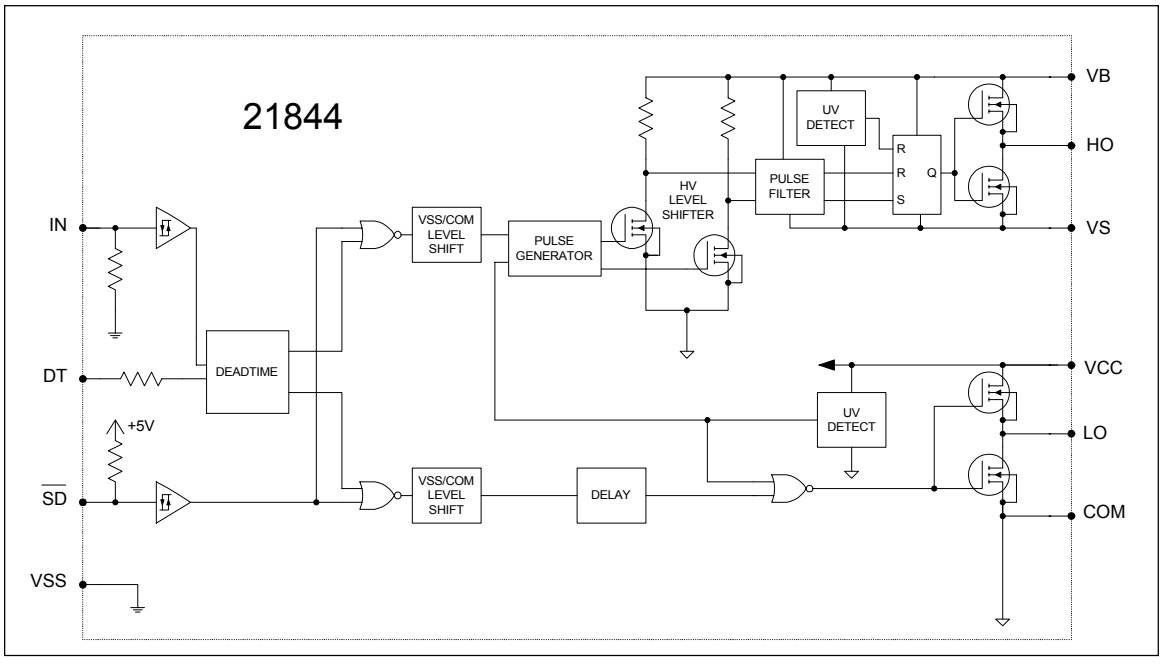
## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $V_{SS}$ = COM, DT= $V_{SS}$ and $T_A$ = 25°C unless otherwise specified. The $V_{IL}$, $V_{IH}$ and $I_{IN}$ parameters are referenced to $V_{SS}$/COM and are applicable to the respective input leads: IN and $\overline{SD}$. The $V_O$, $I_O$ and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic “1” input voltage for HO & logic “0” for LO | 2.7 | — | — | V | $V_{CC}$ = 10V to 20V |
| $V_{IL}$ | Logic “0” input voltage for HO & logic “1” for LO | — | — | 0.8 | | $V_{CC}$ = 10V to 20V |
| $V_{SD,TH+}$ | $\overline{SD}$ input positive going threshold | 2.7 | — | — | | $V_{CC}$ = 10V to 20V |
| $V_{SD,TH-}$ | $\overline{SD}$ input negative going threshold | — | — | 0.8 | | $V_{CC}$ = 10V to 20V |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ - $V_O$ | — | — | 1.2 | | $I_O$ = 0A |
| $V_{OL}$ | Low level output voltage, $V_O$ | — | — | 0.1 | | $I_O$ = 0A |
| $I_{LK}$ | Offset supply leakage current | — | — | 50 | µA | $V_B$ = $V_S$ = 600V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | 20 | 60 | 150 | | $V_{IN}$ = 0V or 5V |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | 0.4 | 1.0 | 1.6 | mA | $V_{IN}$ = 0V or 5V |
| $I_{IN+}$ | Logic “1” input bias current | — | 5 | 20 | µA | IN = 5V, $\overline{SD}$ = 0V |
| $I_{IN-}$ | Logic “0” input bias current | — | 1 | 2 | | IN = 0V, $\overline{SD}$ = 5V |
| $V_{CCUV+}$ $V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V | |
| $V_{CCUV-}$ $V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 | | |
| $V_{CCUVH}$ $V_{BSUVH}$ | Hysteresis | 0.3 | 0.7 | — | | |
| $I_{O+}$ | Output high short circuit pulsed current | 1.4 | 1.9 | — | A | $V_O$ = 0V, PW ≤ 10 µs |
| $I_{O-}$ | Output low short circuit pulsed current | 1.8 | 2.3 | — | | $V_O$ = 15V, PW ≤ 10 µs |

## Functional Block Diagrams

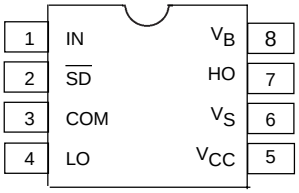


## Lead Definitions

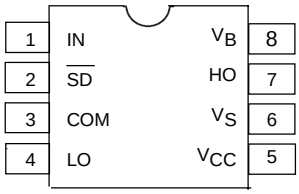
| Symbol | Description |
|---|---|
| IN | Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2184 and VSS for IR21844) |
| $\overline{SD}$ | Logic input for shutdown (referenced to COM for IR2184 and VSS for IR21844) |
| DT | Programmable dead-time lead, referenced to VSS. (IR21844 only) |
| VSS | Logic Ground (21844 only) |
| $V_B$ | High side floating supply |
| HO | High side gate drive output |
| $V_S$ | High side floating supply return |
| $V_{CC}$ | Low side and logic fixed supply |
| LO | Low side gate drive output |
| COM | Low side return |

## Lead Assignments



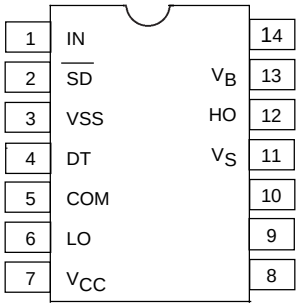

8-Lead PDIP

**IR2184**



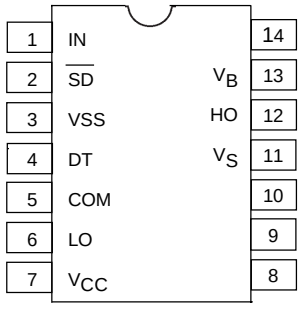

8-Lead SOIC

**IR2184S**



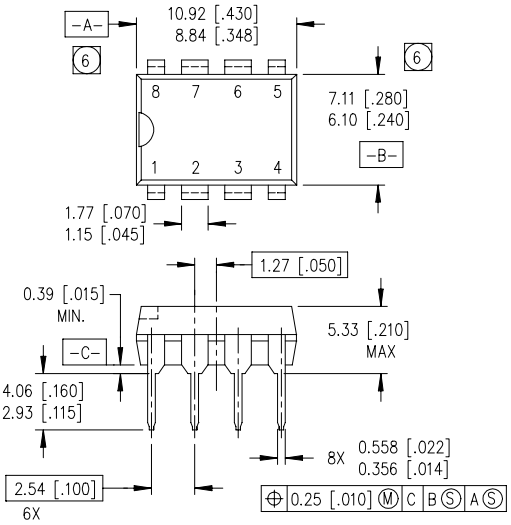

14-Lead PDIP

**IR21844**



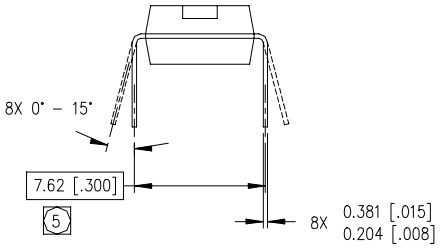

14-Lead SOIC

**IR21844S**



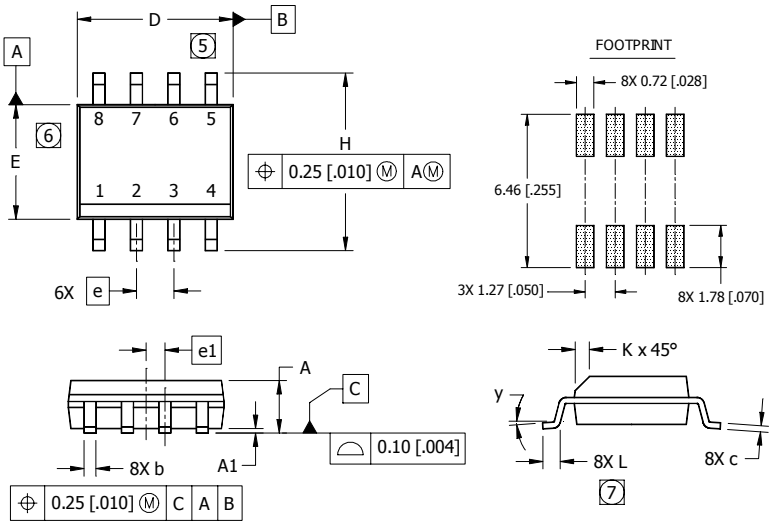

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].




**8-Lead PDIP**

01-6014
01-3003 01 (MS-001AB)



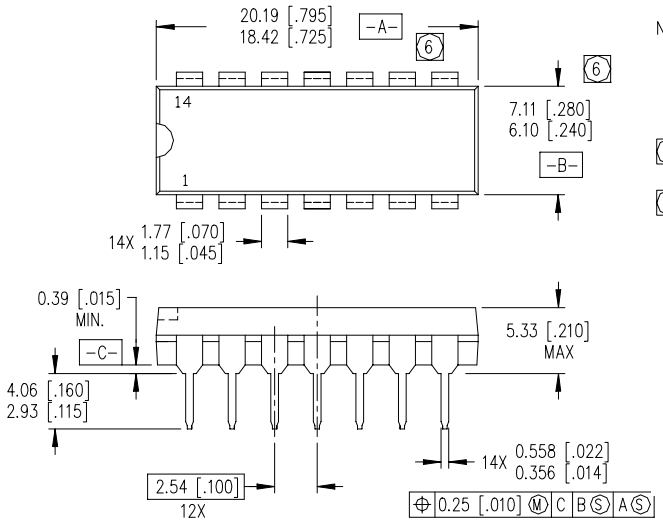

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

NOTES:

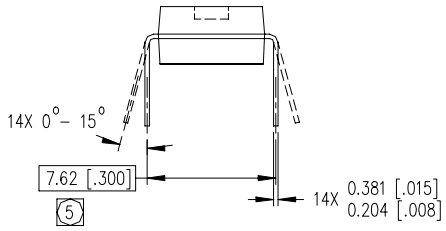
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

**8-Lead SOIC**

01-6027
01-0021 11 (MS-012AA)

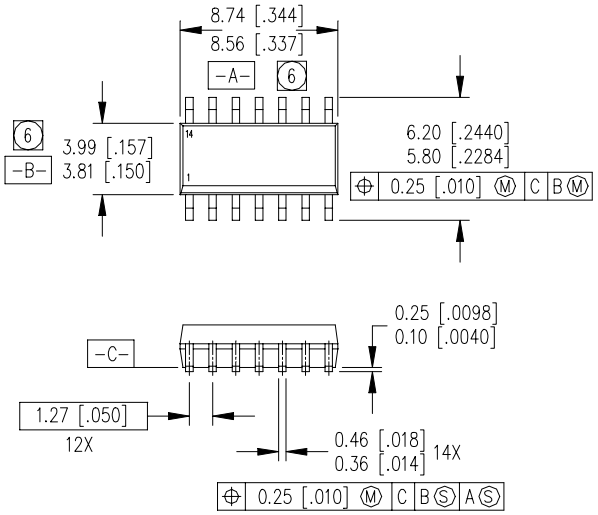



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

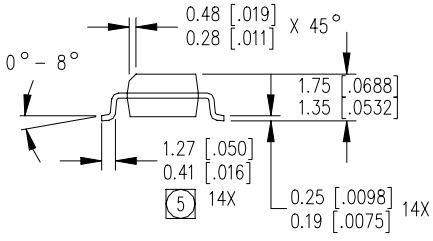



**14-Lead PDIP**

01-6010
01-3002 03 (MS-001AC)




NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006 ].




**14-Lead SOIC (narrow body)**

01-6019
01-3063 00 (MS-012AB)

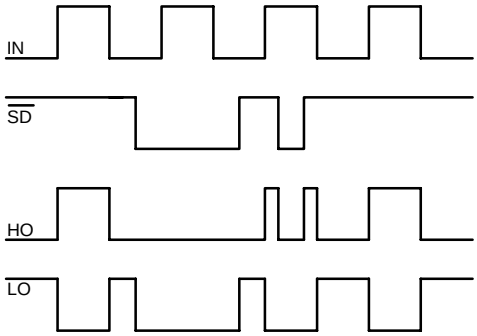



**Figure 1. Input/Output Timing Diagram**

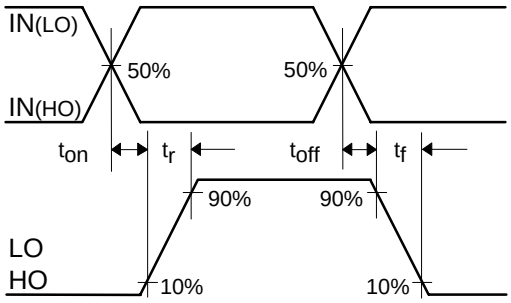



**Figure 2. Switching Time Waveform Definitions**

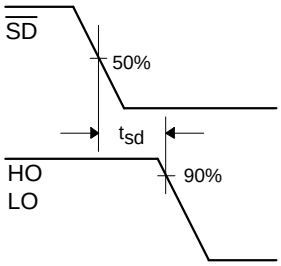



**Figure 3. Shutdown Waveform Definitions**

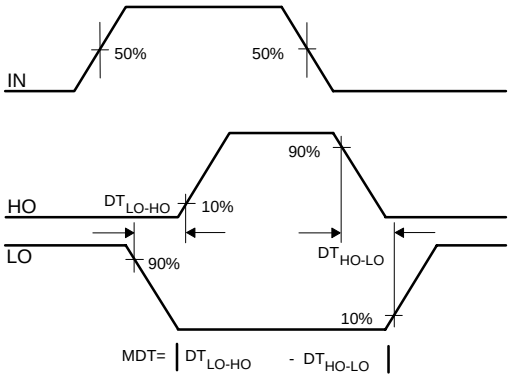



**Figure 4. Deadtime Waveform Definitions**

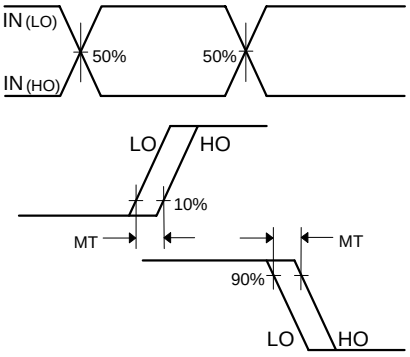



**Figure 5. Delay Matching Waveform Definitions**