FREQUENCY SYNTHESISER CONTROLLER

GENERAL DESCRIPTION

The MMC 381 is one of a pair of CMOS integrated circuits, primarly intended for use in frequency synthesiser. The complementary deyice is the special D/B divider for frequency synthesiser MMC 382/383.
The MMC 381 E/F/G/H tipes are supplied in the 16 lead dual-in-line ceramic or plastic packages

FEATURES

- Wide choice of reference frequency using a single crystal
- maximal reference frequency ≥ 5 MHz
- flexible programming:
  - — direct interface to ROM or PROMS
  - — microprocesor compatible
- wide programme range for the reference counter 6 ÷ 4098
- on-chip crystal controlled oscillator
- cut-down of the power supply of ROM or PROM capabilities
- synchronisation output for switching power supply
- wide range of power supply 3V ÷ 18V
- high noise immunity and low power consumption

APPLICATIONS

- Professional frequency synthetisers

ABSOLUTE MAXIMUM RATINGS

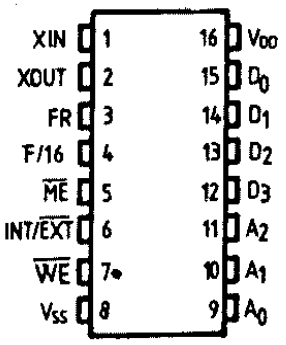
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	8	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



PIN DESIGNATION

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	XIN XOUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal generated reference signal may alternatively be applied to OSC IN. This may be a low signal AC coupled into OSC IN or it may be DC coupled if a full logic swing is available. The programme range of the reference counter is 6-4096 in steps of 2.
3	FR	Reference divider output. The output is logic high, except one period of the crystal oscillator.
4	F/16	Output of the crystal oscillator signal divided by 16 is mainly intended for use switching power supply synchronisation.
5	$\overline{ME}$	An open-drain output for use in controlling the power supply to an external ROM or PROM. The output is low during the data read period and in high impedance at other times.
6	INT/$\overline{EXT}$	This pin allows selection between internal and external programming modes. — external mode — this pin is grounded. ME output is not active, WE is a write enable input for D0—D3. — internal mode — a positive pulse on this pin initiates a programming cycle. The settle time of the external memory is controlled by the high level slot of this pulse. Its width depends on the power-up time of the external memory.
7	WE	Bidirectional write enable pin. In the internal mode the WE signal is internally generated by MMC 381 and is applied to MMC 382/383 (pin 11). In the external mode, WE is a write enable input (whitch triggers the internal data latches). When WE is going high, the input data (D0—D3) will be latched.
8	V_{SS}	Negative supply (normally ground)
9, 10, 11	A0—A2	Bidirectional data select pins — internal mode — tri-state data select outputs intended to address external memory and the MMC 382/383 — external mode — select inputs for the data latches
12—15	D0—D3	Information on these inputs is transfered in the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
16	V_{DD}	Positive supply

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	VALUES 25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		15		0.12	15		450	
			0/10			10		30		0.12	30		900	
			0/15			15		60		0.12	60		1800	
			0/20			20		300		0.24	300		9000	μA
		E, F types	0/ 5			5		50		0.12	50		450	
			0/10			10		100		0.12	100		900	
			0/15			15		200		0.12	200		1800	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		
			0/10		< 1	10	9.95		9.95			9.95		V
			0/15		< 1	15	14.95		14.95			14.95		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min	max	
V_{OL}	Output low voltage		5/0 10/0 15/0		<1 <1 <1	5 10 15		0.05 0.05 0.05			0.05 0.05 0.05		0.05 0.05 0.05	V
V_{IH}	Input high voltage			0.5/4.5 1/9 1.5/13.5	<1 <1 <1	5 10 15	3.5 7 11		3.5 7 11			3.5 7 11		V
V_{IL}	Input low voltage			4.5/0.5 9/1 13.5/1.5	<1 <1 <1	5 10 15		1.5 3 4			1.5 3 4		1.5 3 4	V
I_{OH}	Output drive current	G, H types	0/5 0/5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	−2 −0.64 −1.6 −4.2		−1.6 −0.51 −1.3 −3.4	−3.2 −1 −2.6 −6.8		−1.15 −0.36 −0.9 −2.4		mA
		E, F types	0/5 0/5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	−1.53 −0.52 1.3 −3.6		−1.36 −0.44 −1.1 −3.0	−3.2 −1 −2.6 −6.8		−1.1 −0.36 −0.9 −2.4		
I_{OL}	Output sink current	G, H types	0/5 0/10 0/15	0.4 0.5 1.5		5 10 15	0.64 1.6 4.2		0.51 1.3 3.4	1 2.6 6.8		0.36 0.9 2.4		mA
		E, F types	0/5 0/10 0/15	0.4 0.5 1.5		5 10 15	0.52 1.3 3.6		0.44 1.1 3.0	1 2.6 6.8		0.36 0.9 2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A=25°C; C_L=50pF; R_L=200K; typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			Min.	Typ.	Max.	
t_{THL} t_{TLH}	Transition time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V			200 100 80	ns ns ns
t_{PHL} t_{PLH}	Propagation delay time (INT/EXT to ME)	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V R_L = 200K			400 200 160	ns ns ns
f_{CL}	Maximum clock frequency	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		5 10 15		MHz MHz MHz
t_W(I)	INT/EXT command	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		200 140 100		ns ns ns
t_W(WE)	Write enable pulse width (WE)	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		120 60 50		ns ns ns
t_{SU}	Date setup time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		80 40 30		ns ns ns
t_{P1-H} t_{PO-H}	3-state propagation delay times: output high or low to high	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V R_L = 1 K			300 150 120	ns ns ns
t_{PH-1} t_{PH-1}	Output high impedance to high or low	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V R_L = 1 K			300 150 120	ns ns ns

FUNCTIONAL DESCRIPTION

Reference oscillator

The reference oscillator normally operates with an external crystal. The internal circuitry can be used as a buffer amplifier in case an external reference should be required.

Reference divider

The reference divider is a 12 stages ripple-carry binary counter. The last 11 stages are presettable The programme range of the reference counter is 6—4098 in steps of 2, the division ratie being the programmed number (see date map).
The programme number is loaded from the internal latches at the end os each dividing cycle. The out put is logic high, except each period of the crystal oscillator.

Programming in internal mode

When in internal mode, programming information is supplied by an external ROM or PROM under the control of the MMC 381. Thirty-two data bits are required for frequency synthesiser channel organised as eight 4-bit words. (see date map).
Reading of this data is normally done in a single shot mode with the data read cycle started by a positive pulse, on the program enable pin (int/ext). A memory enable signal is supplied to allow power-down of the memory when not in use. The power-up time of the memory is provided during the positive logic slot of the memory enable pulse. This delay does not depend on the crystal oscillator frequency and is easily correlated with the type of memory in use.

DATA MAP

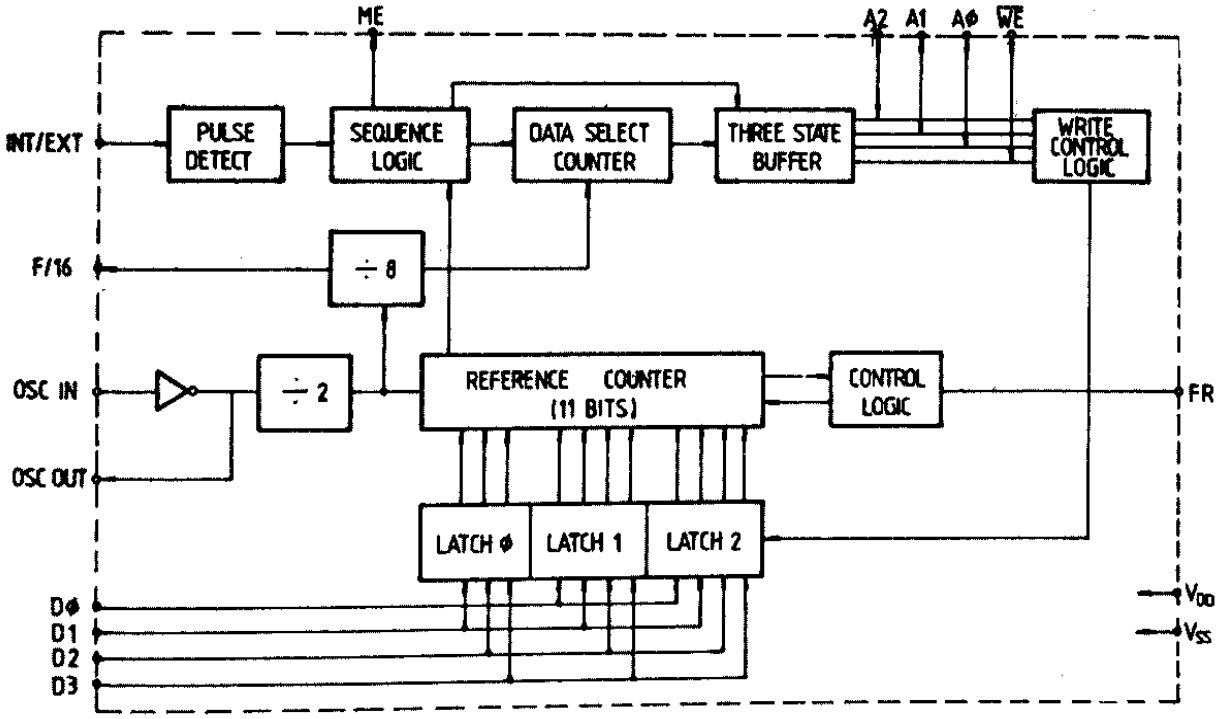
WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	A3	A2	A1	A0
2	0	0	1	B3	B2	B1	B0
3	0	1	0	C03	C02	C01	C00
4	0	1	1	C13	C12	C11	C10
5	1	0	0	C23	C22	C21	C20
6	1	0	1	D3	D2	D1	C30
7	1	1	0	D7	D6	D5	D4
8	1	1	1	D11	D10	D9	D8

The data read cycle is generated from a program clock at 1/16 th of the reference oscillator frequency.
During programming, the division rate will be neither the old one nor the new one. In order to minimize the time of out-of-lock operation, the read cycle is triggered by the output signal.
Data select outputs and WE output remain in a high impedance state when the read cycle is completed to release the data select bus (to allow the address bus to be used for other functions if desired).

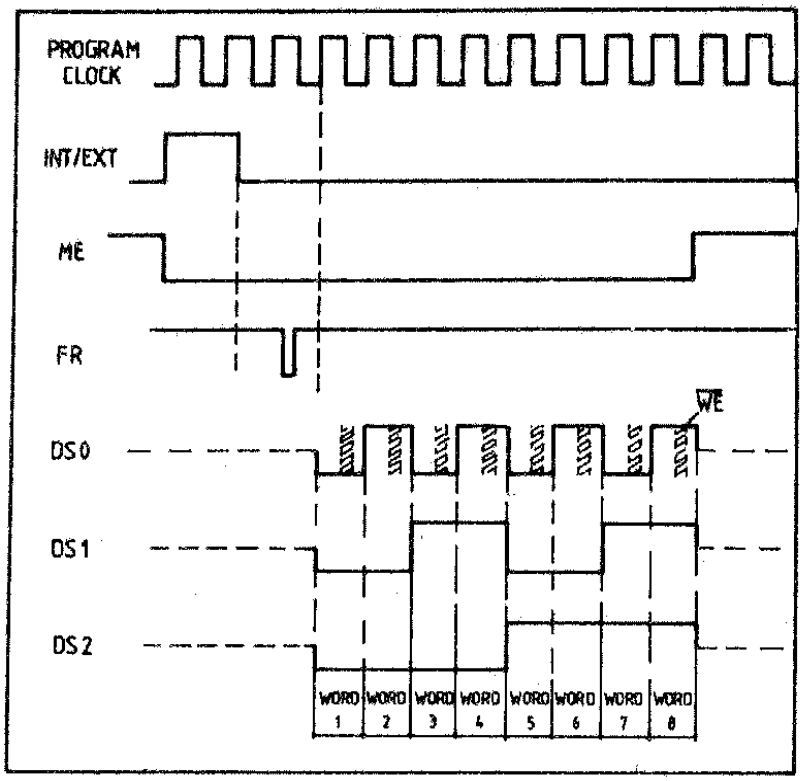
Programming in external mode

This mode of operation is selected by grounding the program pin (INT/EXT). In this mode timing is generated externally, normally by a microprocessor and allows the user to change the data in appropriated latches. The data map is with the WE pin used as a strobe input for the data latches.

BLOCK DIAGRAM



DATA SELECTION



TYPICAL APPLICATION