MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Document order number: MPC17511A
Rev 1.0, 03/2004

Advance Information

17511A

1.0 A 6.8 V H-Bridge Motor Driver IC

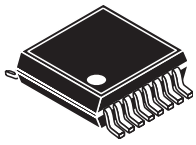
1.0 A 6.8 V H-BRIDGE MOTOR DRIVER IC

The 17511A is a monolithic H-Bridge designed to be used in portable electronic applications to control small DC motors or bipolar step motors. End applications include head positioners (CDROM or disk drive), camera focus motors, and camera shutter solenoids.

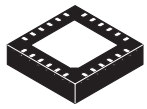
The 17511A can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V. Its low $R_{DS(ON)}$ H-Bridge output MOSFETs (0.46 Ω typical) can provide continuos motor drive currents of 1.0 A and handle peak currents up to 3.0 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

The 17511A has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).



EV (Pb-FREE) SUFFIX
CASE 1563-01
16-LEAD VMFP



EP (Pb-FREE) SUFFIX
CASE 1508-01
24-LEAD QFN

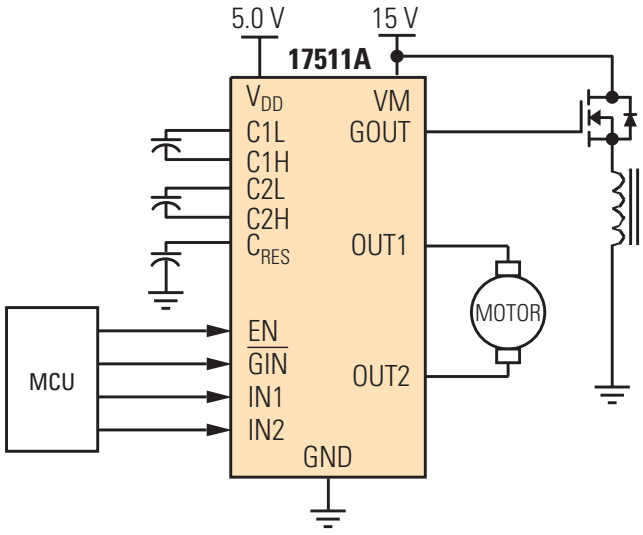
ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MPC17511AEV/EL	-20°C to 65°C	16 VMFP
MPC17511AEP/R2		24 QFN

Features

- 2.0 V to 6.8 V Continuous Operation
- Output Current 1.0 A (DC), 3.0 A (Peak)
- MOSFETs < 600 mΩ $R_{DS(ON)}$ @ 25°C Guaranteed
- 3.0 V/5.0 V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown
- Cross-Conduction Suppression
- Low Power Consumption
- Pb-Free Packaging Designated by Suffix Codes EV and EP

17511A Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

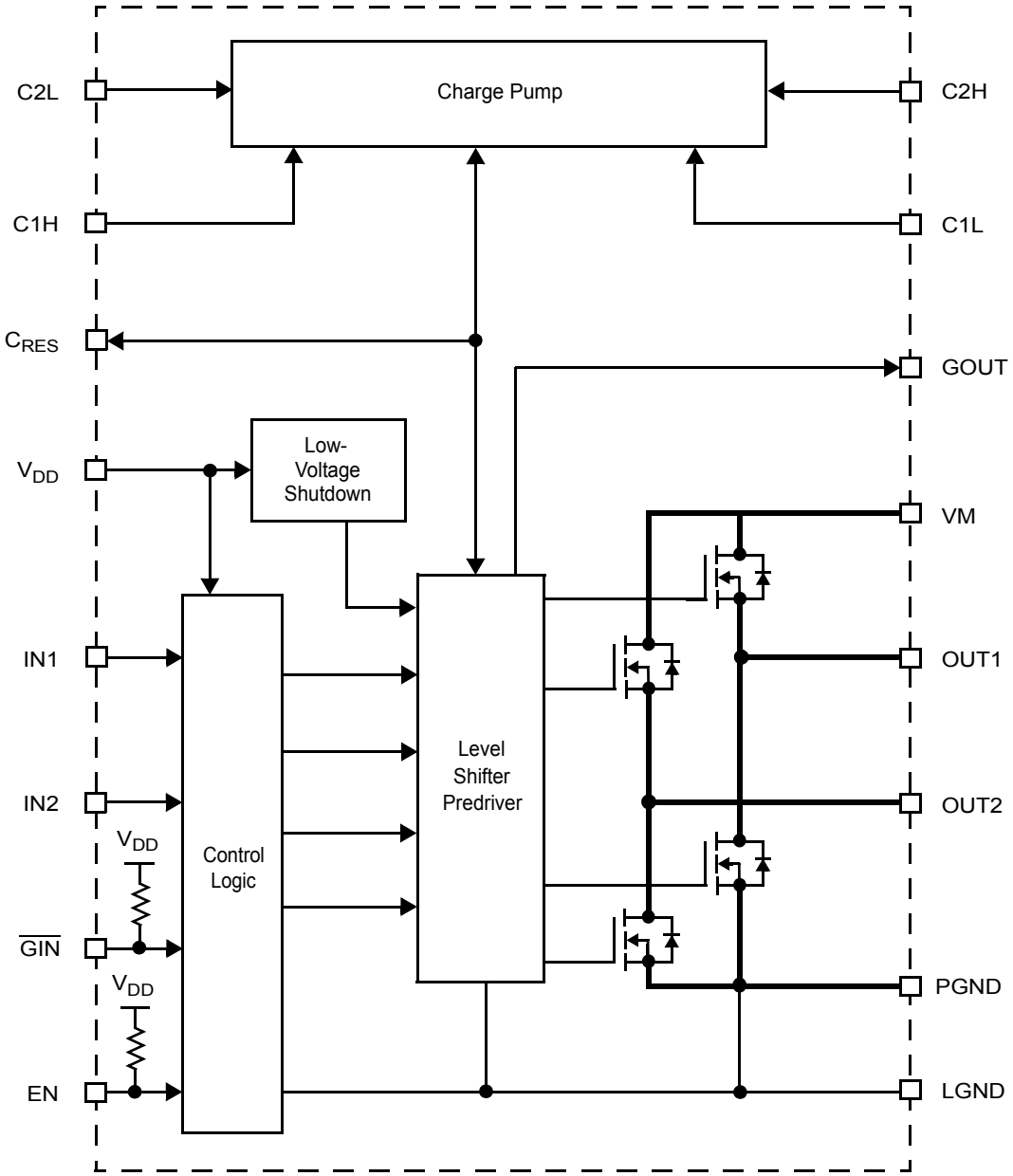
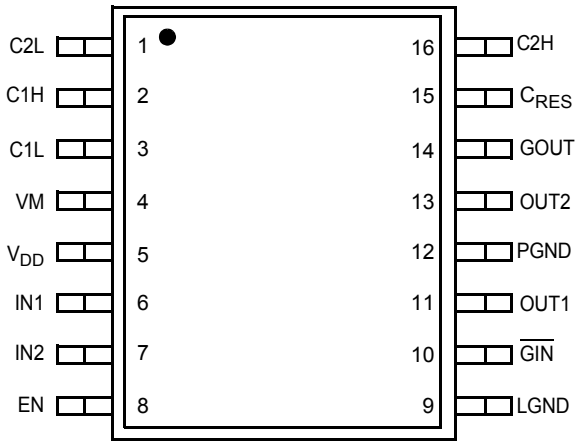
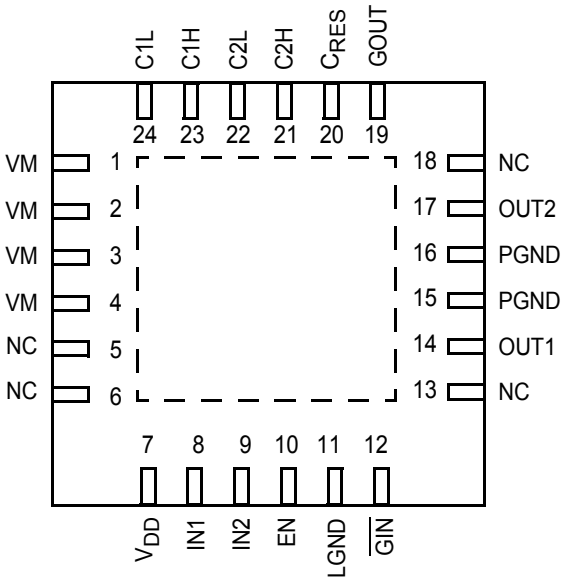


Figure 1. 17511A Simplified Internal Block Diagram



VMFP TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
2	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
3	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
4	VM	Motor Drive Power Supply	Driver power supply voltage input terminal.
5	V_{DD}	Logic Supply	Control circuit power supply terminal.
6	IN1	Input Control 1	Control signal input 1
7	IN2	Input Control 2	Control signal input 2.
8	EN	Enable Control	Enable control signal input terminal.
9	LGND	Logic Ground	Logic ground terminal.
10	$\overline{GIN}$	Gate Driver Input	LOW = True control signal for GOUT terminal.
11	OUT1	H-Bridge Output 1	Driver output 1 (right half of H-Bridge).
12	PGND	Power Ground	Driver ground terminal.
13	OUT2	H-Bridge Output 2	Driver output 2 (left half of H-Bridge).
14	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
15	C_{RES}	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor terminal.
16	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).



QFN TERMINAL FUNCTION DESCRIPTION

Terminals	Terminal Name	Formal Name	Definition
1, 2, 3, 4	VM	Motor Drive Power Supply	Driver power supply voltage input terminal.
5, 6, 13, 18	NC	No Connect	This terminal is not used.
7	V_{DD}	Logic Supply	Control circuit power supply terminal.
8	IN1	Logic Input Control 1	Control signal input 1.
9	IN2	Logic Input Control 2	Control signal input 2.
10	EN	Enable Control	Enable control signal input terminal.
11	LGND	Logic Ground	Logic ground terminal.
12	$\overline{GIN}$	Gate Driver Input	LOW = True control signal for GOUT terminal.
14	OUT1	Output 1	Driver output 1 (right half of H-Bridge).
15, 16	PGND	Power Ground	Driver ground terminal.
17	OUT2	Output 2	Driver output 2 (left half of H-Bridge).
19	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
20	C_{RES}	Pre-Driver Power Supply	Pre-driver circuit power supply terminal.
21	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
22	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
23	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
24	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Charge Pump Output Voltage	$V_{C_{RES}}$	-0.5 to 14.0	V
Logic Supply Voltage	V_{DD}	-0.5 to 7.0	V
Signal Input Voltage (EN, IN1, IN2, $\overline{GIN}$)	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current			A
Continuous	I_O	1.0	
Peak (Note 1)	I_{OPK}	3.0	
ESD Voltage			V
Human Body Model (Note 2)	V_{ESD1}	±1800	
Machine Model (Note 3)	V_{ESD2}	±100	
Storage Temperature Range	T_{STG}	-65 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Operating Junction Temperature	T_J	-20 to 150	°C
Thermal Resistance (Note 4)	$R_{\theta JA}$	150	°C/W
Power Dissipation (Note 5)	P_D	830	mW
Soldering Temperature (Note 6)	T_{SOLDER}	260	°C

Notes

1. T_A = 25°C, 10 ms pulse width at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. 37 x 50 x 1.6 [mm] glass EPOXY board mount.
5. Maximum at T_A = 25°C.
6. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_M = V_{DD} = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Driver Circuit Power Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	5.0	5.7	V
Capacitor for Charge Pump	C1, C2, C3	0.01	0.1	1.0	μF
Standby Power Supply Current					
Motor Supply Standby Current	I_{VMSTBY}	–	–	1.0	μA
Logic Supply Standby Current (Note 7)	$I_{VDDSTBY}$	–	–	1.0	mA
Operating Power Supply Current					
Logic Supply Current (Note 8)	I_{VDD}	–	–	3.0	mA
Charge Pump Circuit Supply Current	I_{CRES}	–	–	0.7	mA
Low V_{DD} Detection Voltage (Note 9)	V_{DD}DET	1.5	2.0	2.5	V
Driver Output ON Resistance (Note 10)	$R_{DS(ON)}$	–	0.46	0.60	Ω
GATE DRIVE					
Gate Drive Voltage (Note 11) No Current Load	V_{CRES}	12	13	13.5	V
Gate Drive Ability (Internally Supplied) I_{CRES} = -1.0 mA	$V_{CRESload}$	10	11.2	–	V
Gate Drive Output					V
I_{OUT} = -50 μA	$V_{GOUThigh}$	V_{CRES}-0.5	V_{CRES}-0.1	V_{CRES}	
I_{IN} = 50 μA	$V_{GOUTlow}$	LGND	LGND+0.1	LGND+0.5	
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Input Function (2.7 V < V_{DD} < 5.7 V)					
High-Level Input Voltage	V_{IH}	V_{DD} x 0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x 0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	μA
Low-Level Input Current	I_{IL}	-1.0	–	–	μA
Pull-Up Resistance (EN, $\overline{GIN}$)	R_{PU}	50	100	200	kΩ

Notes

7. $I_{VDDSTBY}$ includes current to the predriver circuit.
8. I_{VDD} includes current to the predriver circuit.
9. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, V_{CRES} = 7.5 V.
10. I_O = 1.0 A source + sink.
11. Input logic signal not present.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, $V_M = V_{DD}$ = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT (EN, IN1, IN2, $\overline{GIN}$)					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (Note 12)	t_R	–	–	1.0 (Note 13)	μs
Input Pulse Fall Time (Note 14)	t_F	–	–	1.0 (Note 13)	μs
OUTPUT					
Propagation Delay Time					μs
Turn-ON Time	t_{PLH}	–	0.55	1.0	
Turn-OFF Time	t_{PHL}	–	0.55	1.0	
GOUT Propagation Delay Time					μs
Turn-ON Time	t_{SON}	–	0.15	0.5	
Turn-OFF Time	t_{SOFF}	–	0.15	0.5	
Charge Pump Circuit (Note 15)	$tV_{CRES}on$				ms
Rise Time (Note 16)		–	0.1	3.0	
Low-Voltage Detection Time	$t_{VDD}DET$	–	–	10	ms

Notes

12. Time is defined between 10% and 90%.
13. That is, the input waveform slope must be steeper than this.
14. Time is defined between 90% and 10%.
15. When C1 = C2 = C3 = 0.1 μF.
16. Time to charge C_{RES} to 11 V after application of V_{DD}.

Timing Diagrams

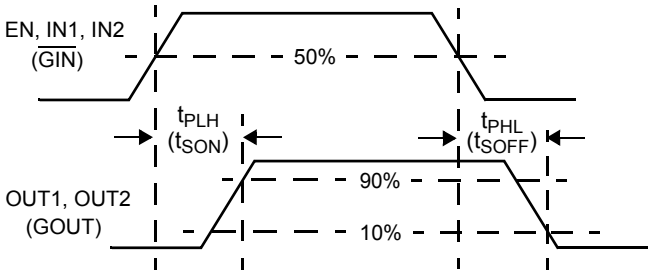


Figure 2. t_{PLH}, t_{PHL}, and t_{PZH} Timing

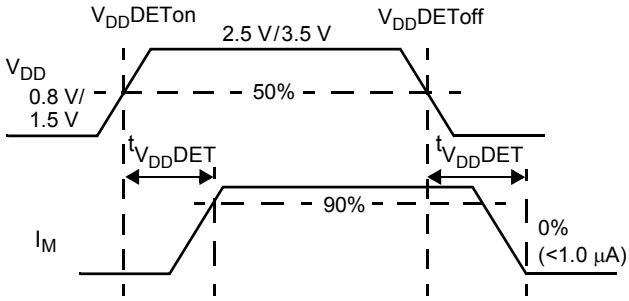


Figure 3. Low-Voltage Detection

Table 1. Truth Table

INPUT				OUTPUT		
EN	**IN1**	**IN2**	**$\overline{GIN}$**	**OUT1**	**OUT2**	**GOUT**
H	H	H	X	L	L	X
H	H	L	X	H	L	X
H	L	H	X	L	H	X
H	L	L	X	Z	Z	X
L	X	X	X	L	L	L
H	X	X	H	X	X	L
H	X	X	L	X	X	H

H = High.
L = Low.
Z = High impedance.
X = Don't care.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 17511A is a monolithic H-Bridge power IC applicable to small DC motors used in portable electronics. The 17511A can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V, and it can provide continuos motor drive currents of 1.0 A while handling peak currents up to 3.0 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17511A has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

Basic protection and operational features (direction, dynamic braking, PWM control of speed and torque, main power supply undervoltage detection and shutdown, logic power supply undervoltage detection and shutdown), in addition to the 1.0 A rms output current capability, make the 17511A a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 17511A devices can be used to control bipolar step motors. The 17511A can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 1, 17511A Simplified Internal Block Diagram, page 2, the 17511A is a monolithic H-Bridge with built-in charge pump circuitry. For a DC motor to run, the input conditions need to be set as follows: ENable input logic HIGH, one INput logic LOW, and the other INput logic HIGH (to define output polarity). The 17511A can execute dynamic braking by setting both IN1 and IN2 logic HIGH, causing both low-side MOSFETs in the output H-Bridge to turn ON. Dynamic braking can also implemented by taking the ENable logic LOW. The output of the H-Bridge can be set to an open-circuit high-impedance (Z) condition by taking both IN1 and IN2 logic LOW. (refer to Table 1, Truth Table, page 8).

The 17511A outputs are capable of providing a continuous DC load current of up to 1.2 A. An internal charge pump supports PWM frequencies to 200 kHz. The EN terminal also controls the charge pump, turning it off when EN = LOW, thus allowing the 17511A to be placed in a power-conserving sleep mode.

FUNCTIONAL TERMINAL DESCRIPTION

OUT1 and OUT2

The OUT1 and OUT2 terminals provide the connection to the internal power MOSFET H-Bridge of the IC. A typical load connected between these terminals would be a small DC motor. These outputs will connect to either VM or PGND, depending on the states of the control inputs (refer to Table 1, Truth Table, page 8).

PGND and LGND

The power and logic ground terminals (PGND and LGND) should be connected together with a very low-impedance connection.

C_{RES}

The C_{RES} terminal provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively this terminal can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor. The voltage at the C_{RES} terminal will be approximately three times the V_{DD} voltage, as the internal charge pump utilizes a voltage tripler circuit. The $^{V}C_{RES}$ voltage is used by the IC to supply gate drive for the internal power MOSFET H-Bridge.

VM

The VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUT1 and OUT2. All VM terminals must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between terminals.

VM has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

IN1, IN2, and EN

The IN1, IN2, and EN terminals are input control terminals used to control the outputs. These terminals are 5.0 V CMOS-compatible inputs with hysteresis. The IN1, IN2, and EN work together to control OUT1 and OUT2 (refer to Table 1, Truth Table).

$\overline{GIN}$

The $\overline{GIN}$ input controls the GOUT terminal. When $\overline{GIN}$ is set logic LOW, GOUT supplies a level-shifted high-side gate drive signal to an external MOSFET. When $\overline{GIN}$ is set logic HIGH, GOUT is set to GND potential.

C1L and C1H, C2L and C2H

These two pairs of terminals, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

GOUT

The GOUT output terminal provides a level-shifted, high-side gate drive signal to an external MOSFET with C_{iss} up to 500 pF.

V_{DD}

The V_{DD} terminal carries the 5.0 V supply voltage and current into the logic sections of the IC. V_{DD} has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

APPLICATIONS

Figure 4 shows a typical application for the 17511A. When applying the gate voltage to the C_{RES} terminal from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = {}^{V}C_{RES}/0.02\ \Omega$.

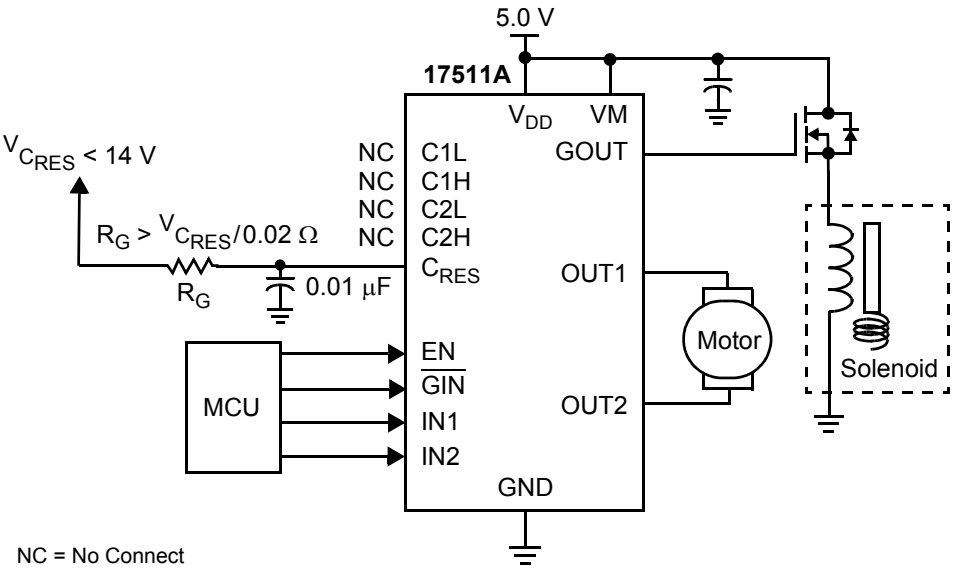


Figure 4. 17511A Typical Application Diagram

CEMF Snubbing Techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply terminal (VM) (see Figure 5).

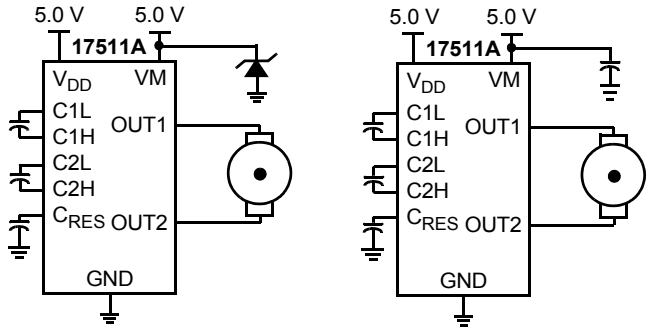
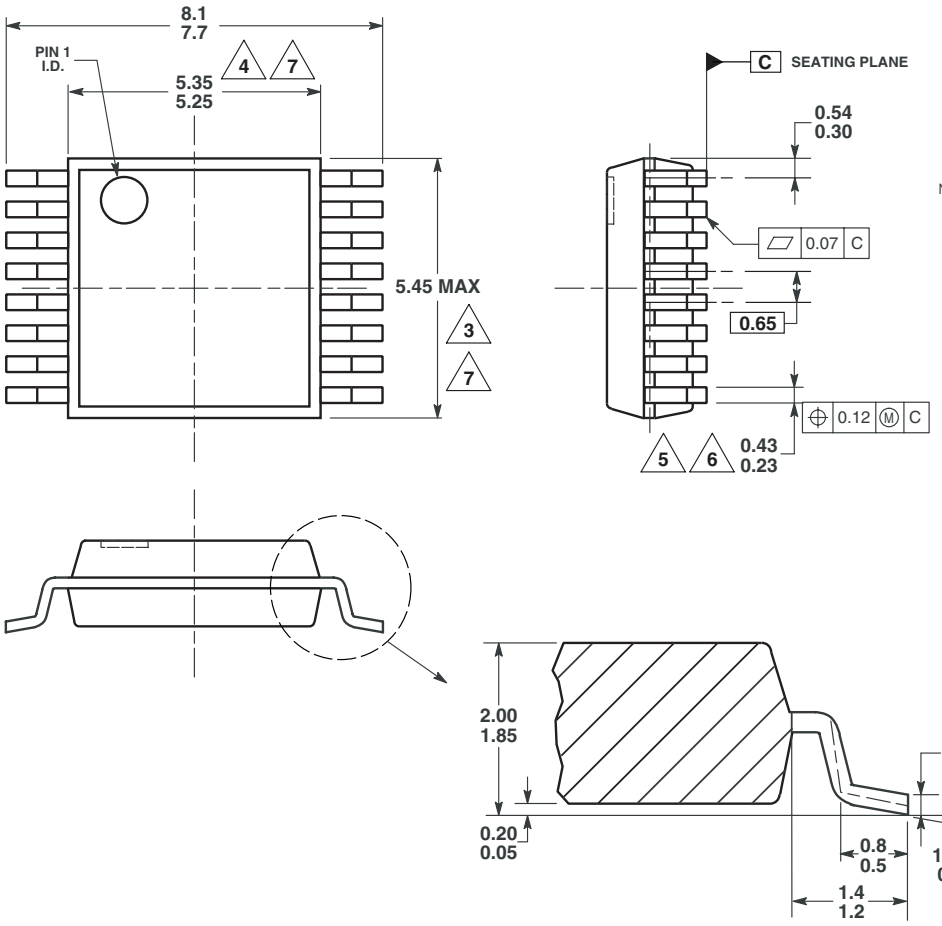


Figure 5. CEMF Snubbing Techniques

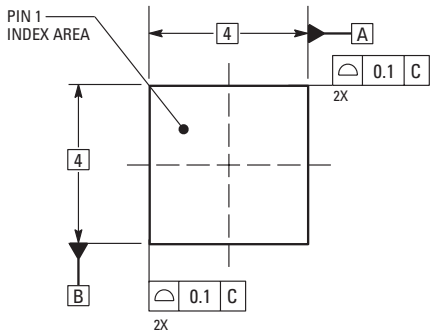
PACKAGE DIMENSIONS

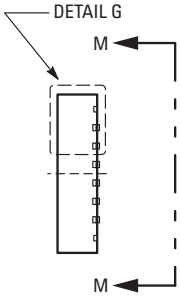
EV (Pb-FREE) SUFFIX
16-LEAD VMFP
PLASTIC PACKAGE
CASE 1563-01
ISSUE O



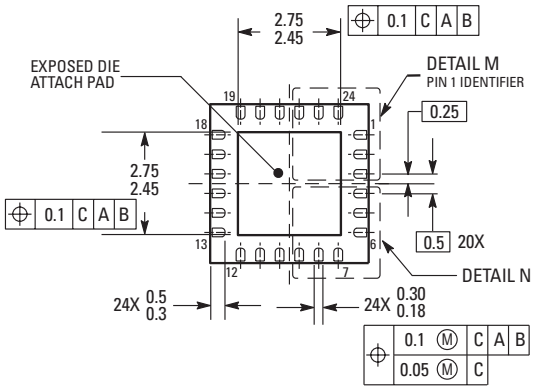
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM AND 0.25MM FROM THE LEAD TIP.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASITC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

EP (Pb-FREE) SUFFIX
24-LEAD QFN
NON-LEADED PACKAGE
CASE 1508-01
ISSUE O

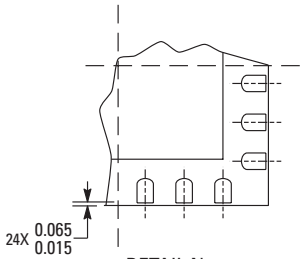




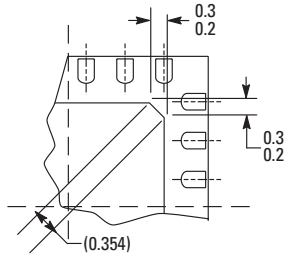
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.



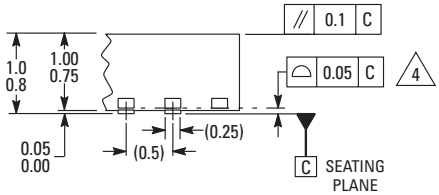
VIEW M-M



DETAIL N
CORNER CONFIGURATION



DETAIL M
PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CLOCKWISE

NOTES

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