SC410

3A EcoSpeed ™ Step-Down Regulator with LDO and Ultrasonic Power Save

POWER MANAGEMENT

Features

- Input voltage — 5.5V to 24V
- Output voltage — 0.75V to 7.5V
- Output current — Up to 3A
- Internal reference — ± 1%
- Small ceramic capacitors
- Power good pin (open-drain)
- Patented adaptive on-time control:
  - Excellent transient response
  - Programmable pseudo-fixed frequency during CCM
- Fault protection features:
  - Cycle-by-cycle current limit
  - Short circuit protection
  - Over and under output voltage protection
  - Over-temperature
- Internal soft-start
- Ultrasonic power save and smart PSAVE
- Internal LDO for bias voltage
- Ultra-small lead-free 3 x 3mm, 10-Pin MLPD package
- WEEE and RoHS compliant

Applications

- Networking Equipment, Embedded Systems
- Medical Equipment, Office Automation
- Instrumentation, Portable Systems
- Consumer Devices such as DTV and Set-top Boxes
- POL Converters

Description

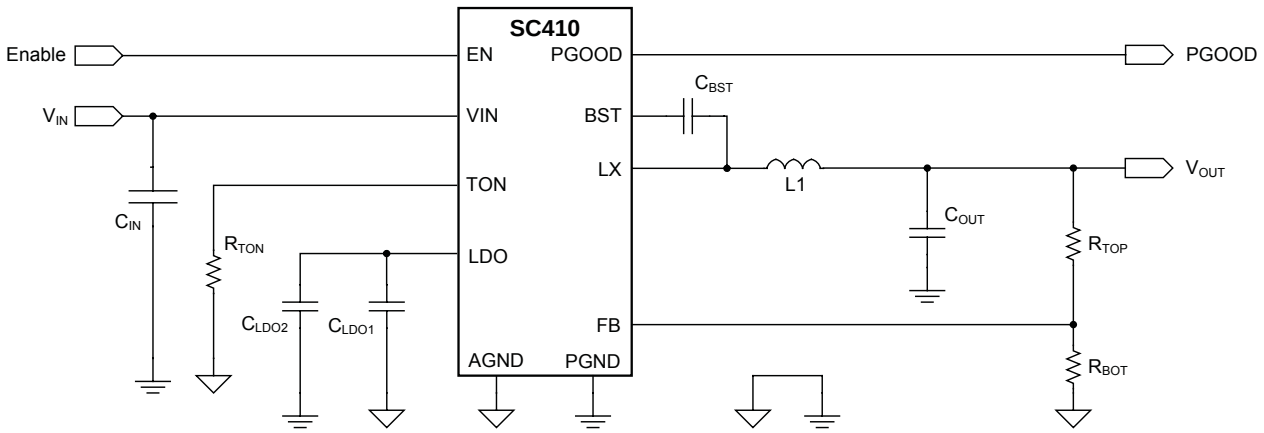
The SC410 is an integrated, synchronous 3A EcoSpeed™ step-down regulator. It incorporates Semtech's advanced, patented adaptive on-time architecture to achieve best-in-class dynamic performance using point-of-load applications. The input voltage range is 5.5V to 24V with a programmable output voltage from 0.75V up to 7.5V. The device features an internal LDO and ultrasonic PSAVE mode for high efficiency across the output load range.

Adaptive on-time control provides programmable pseudo-fixed frequency operation in continuous conduction and excellent transient performance. The switching frequency can be set from 200kHz to 1MHz, allowing the designer to reduce external LC filtering and minimize light load (standby) losses.

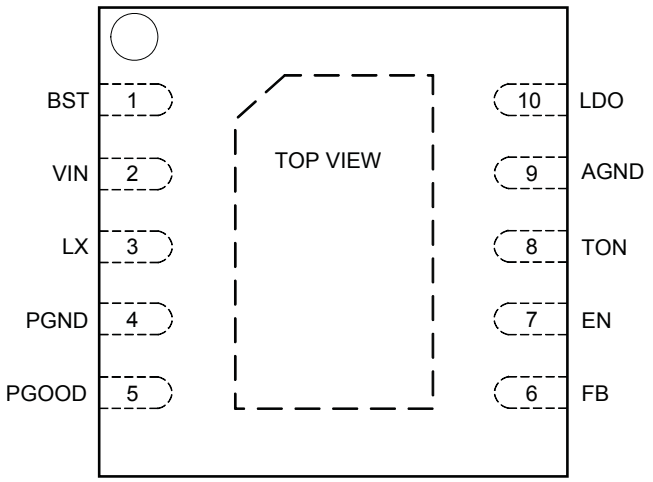
Additional features include cycle-by-cycle current limit, soft start, input UVLO and output OV protection, and over temperature protection. The open-drain PGOOD pin provides output status. Standby current is less than 10µA when disabled.

The device is available in a low profile, thermally enhanced MLPD 3 x 3mm 10-pin package.

Typical Application Circuit



Pin Configuration



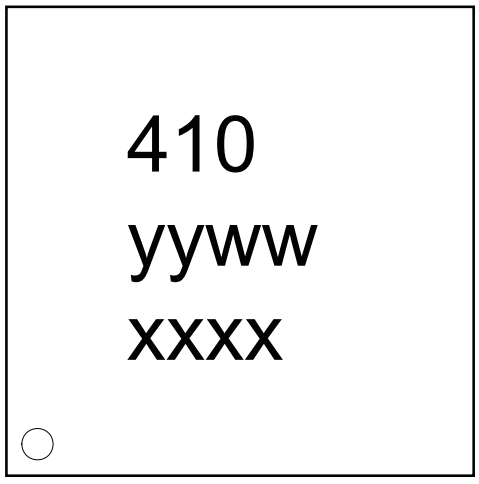
MLPD; 3 x 3, 10 LEAD
θ_{JA} = 40°C/W

Ordering Information

Device	Package
SC410MLTRT[1][2]	MLPD-10 3 x 3
SC410EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date code
xxxx = Lot number

Absolute Maximum Ratings

LX to GND (V) ..... -0.3 to +28
VIN to PGND, EN/PSV to AGND (V) ..... -0.3 to +28
VIN to LDO (V) ..... - 0 . 3
BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +34
LDO to AGND (V) ..... -0.3 to +6.0
FB, PGOOD, TON (V) ..... -0.3 to LDO +0.3
AGND to PGND (V) ..... -0.3 to +0.3
Maximum Peak Inductor Current (A) 5.5
Peak IR Reflow Temperature (°C) 260
ESD Protection Level (kV)[1] 2

Recommended Operating Conditions

Supply Input Voltage (V) ..... 5.5 to 24
Maximum Continuous Output Current (A) 3
Maximum Peak Inductor Current (A) 5.0

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal Resistance, Junction to Ambient[2] (°C/W) 40

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A=+25°C for Typ, -40°C to +85°C for Min and Max, T_J < 125°C, per detailed application circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
VIN UVLO Threshold	Programmable with EN pin after 2 switching cycles		1.5		V
VIN UVLO Hysteresis			50		mV
Internal Bias UVLO Threshold	Rising UVLO V_{TH}		4		V
Internal Bias UVLO Hysteresis			0.3		V
VIN Supply Current	V_{EN} = 0V		9		µA
	I_{OUT}= 0A, f_{SW}=25kHz[1]		2.5		mA
Controller					
FB On-Time Threshold		0.7425	0.75	0.7575	V
Frequency Programming Range	See R_{TON} Calculation	200		1000	kHz
Minimum Frequency Range	during Ultrasonic PSAVE		22		kHz
FB Input Bias Current	FB=5V or 0V	-1		+1	µA

Electrical Characteristics (continued)

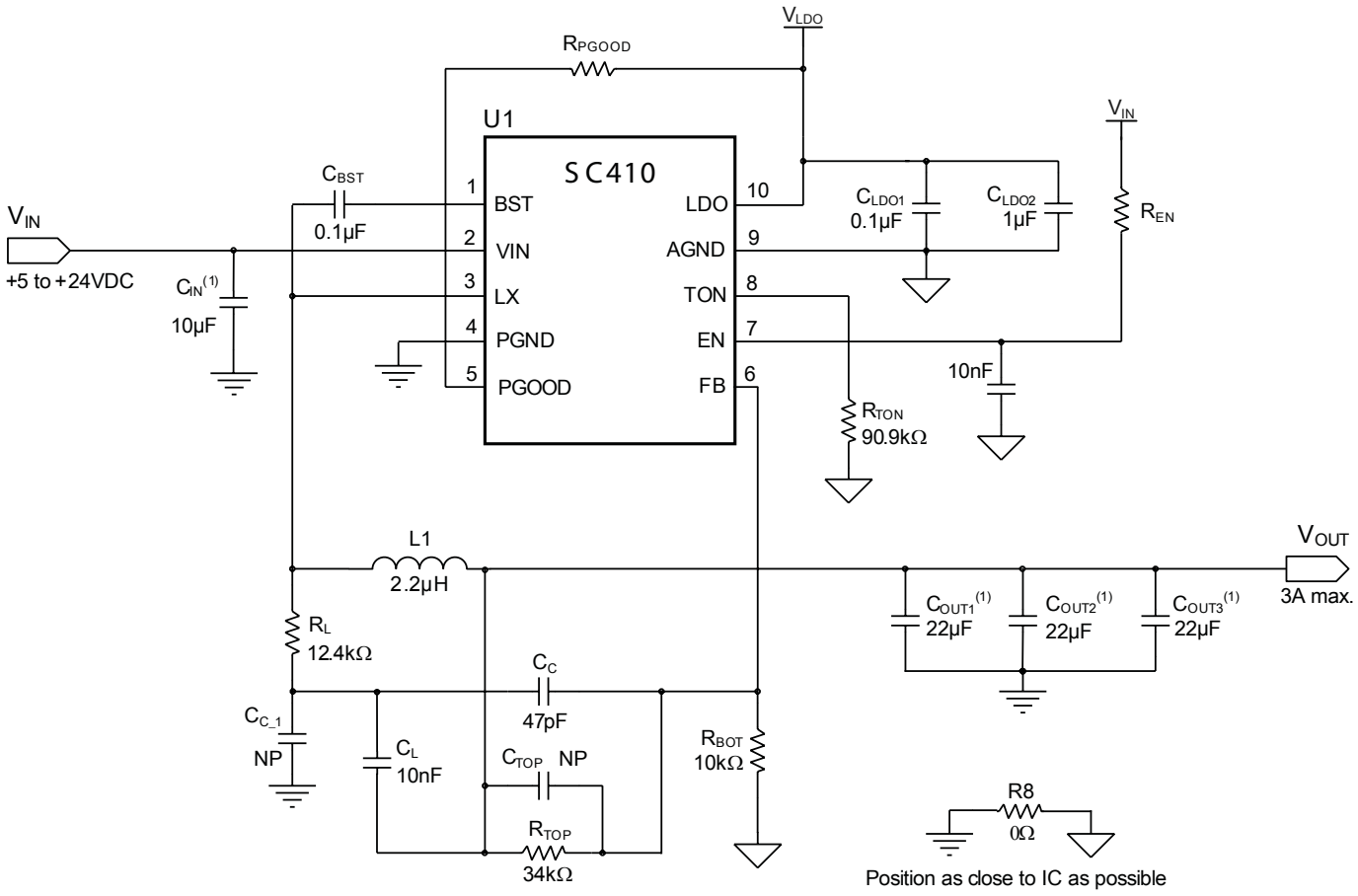
Parameter	Conditions	Min	Typ	Max	Units
Timing					
On-Time	Continuous Mode V_{IN}=15V, V_{OUT}=3V, R_{TON}= 200kΩ	0.9	1	1.1	µs
Minimum On-Time(1)			100		ns
Minimum Off-Time(1)			320		ns
Soft start					
Soft start Time(1)	Delay from PWM Switching to Output Regulation		850		µs
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND	-10	0	+10	mV
Power Good					
Power Good Threshold	Upper Limit, V_{FB} > internal 750mV reference		120		%V_{REF}
	Lower Limit, V_{FB} < internal 750mV reference		90		
PGOOD Delay Time(1)	Between VOUT at 90% of its regulation value and the PGOOD signal transitioning to high		1		ms
Noise Immunity Delay Time (1)			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω
Fault Protection					
Output Under-Voltage Fault	FB with Respect to REF, 8 Consecutive Switching Cycles		75		%V_{REF}
Output Over-Voltage Fault	FB with Respect to REF		120		%V_{REF}
Smart PowerSave Protection Threshold	FB with Respect to REF		110		%V_{REF}
OV, UV Fault Noise Immunity Delay (1)			5		µs
Over-Temperature Shutdown (1)	OT Latched		145		°C
Enable Logic					
PWM Output Enabled(1)			1.5		V
LDO Output Enabled			0.8		V
EN Input Bias Current	V_{EN} = 5V	-10		10	µA

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Gate Drivers					
BST Switch On resistance			25		Ω
Internal Power MOSFETs					
Current Limit[2]	Inductor Valley Current Limit, VLDO=5V	2.4	3.2		A
LX Leakage Current	VIN=24V, LX=0V, High Side		1	10	µA
Switch Resistance	High Side		215		mΩ
	Low Side		110		
Non-overlap time [1]			15		ns
Linear Regulator (The LDO is shorted to the bias node, internally)					
LDO Accuracy		-4		4	$\%V_{LDO}$
LDO Current Limit	Short circuit protection, V_{IN} = 12V, V_{LDO} <80% of final V_{LDO} value		35		mA
	Operating current limit, V_{IN} = 12V, V_{LDO} > 80% of final V_{LDO} value		100		
LDO Drop Out Voltage	From V_{IN} to V_{LDO}, I_{LDO} = 100mA		1.2		V

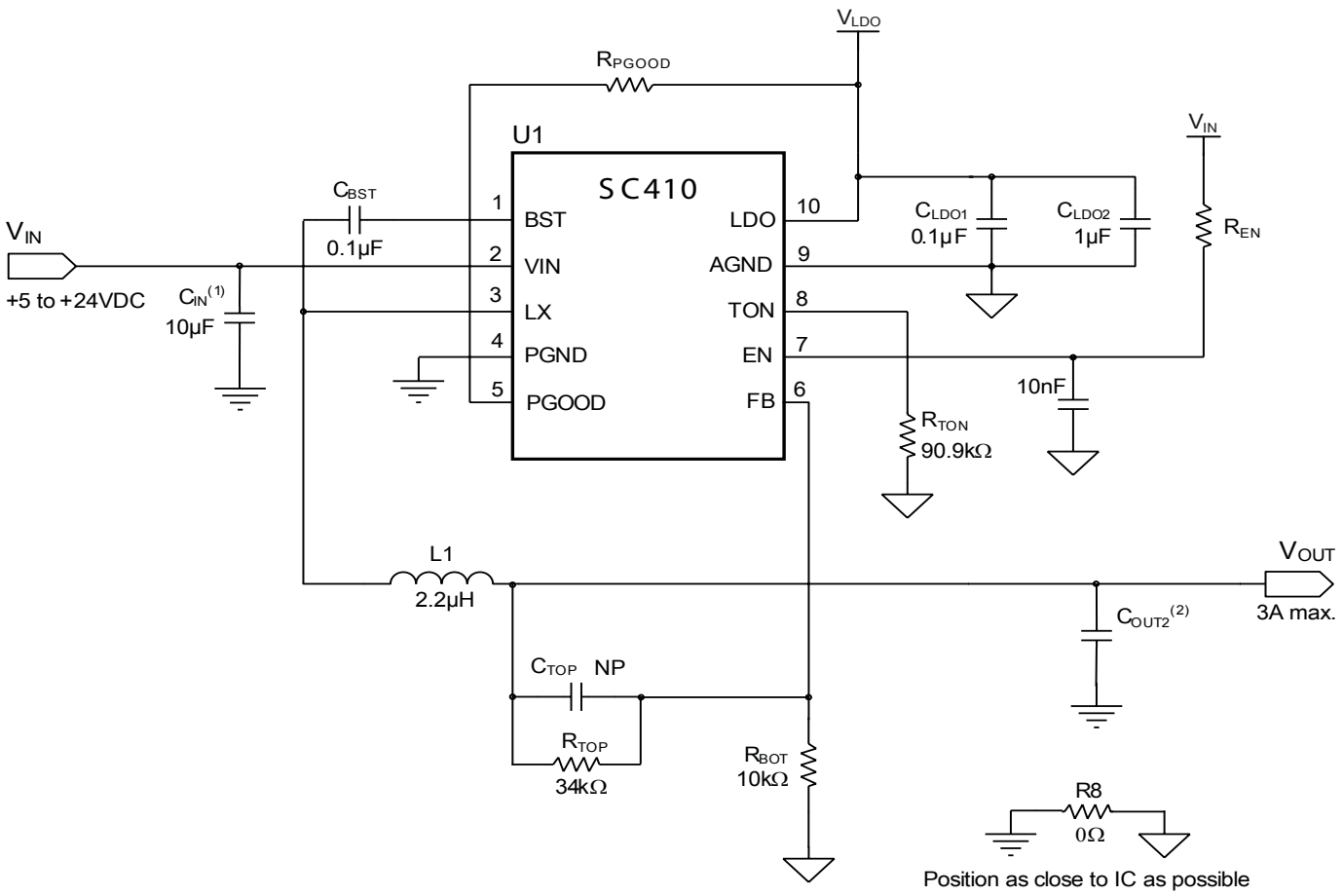
Note:
(1) Typical value from EVB, not ATE tested.
(2) The minimum inductor valley current limit of 2.4V gives an average output current limit of 3A assuming 1.2A inductor ripple current.

Detailed Application Circuit-1



Note: (1) Ceramic capacitors

Detailed Application Circuit-2

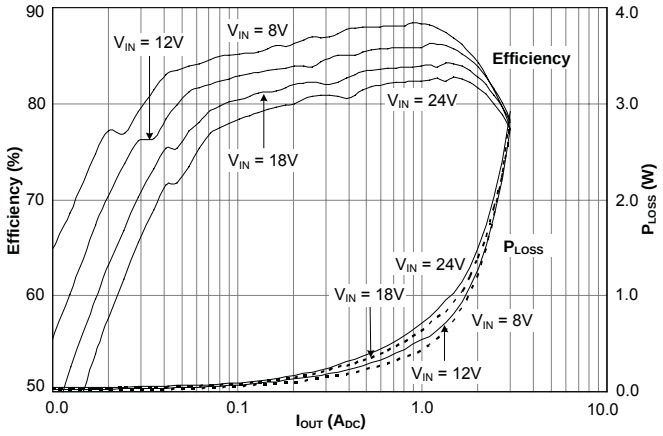


Notes: (1) Ceramic capacitor
(2) Capacitor must provide ESR for user application

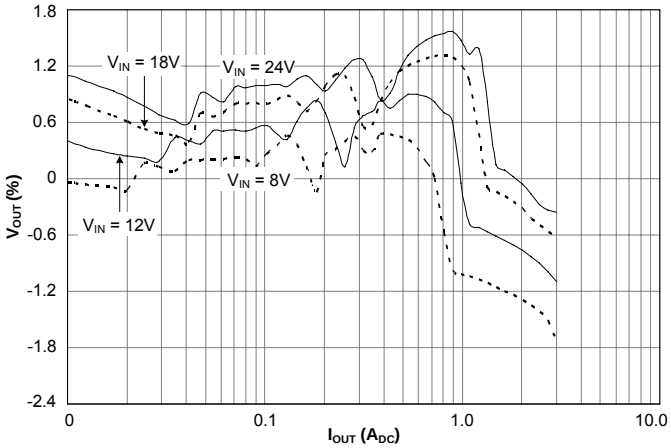
Typical Characteristics

Characteristics are based on a circuit with V_{IN} = 12V, L = 2.2µH (DCR = 35mΩ), C_{OUT} = 66µF, V_{OUT} = 3.3V, V_{LDO} = 5V, R_{TON} = 90.9kΩ.

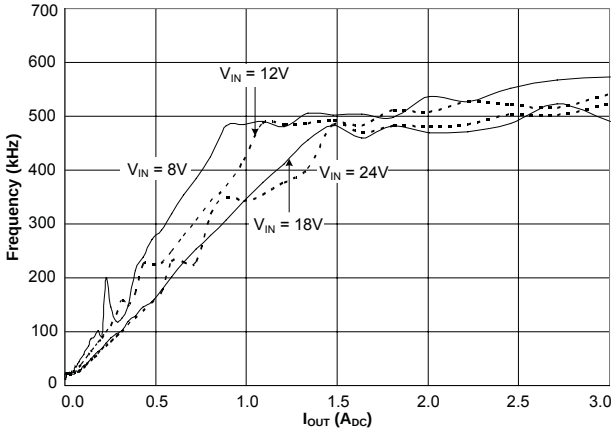
Efficiency — Power Loss



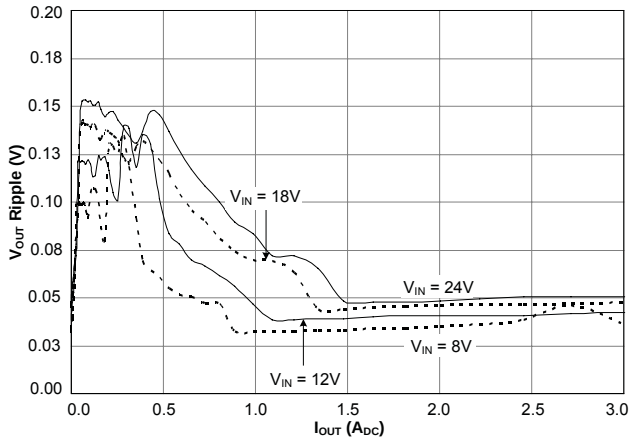
Load Regulation



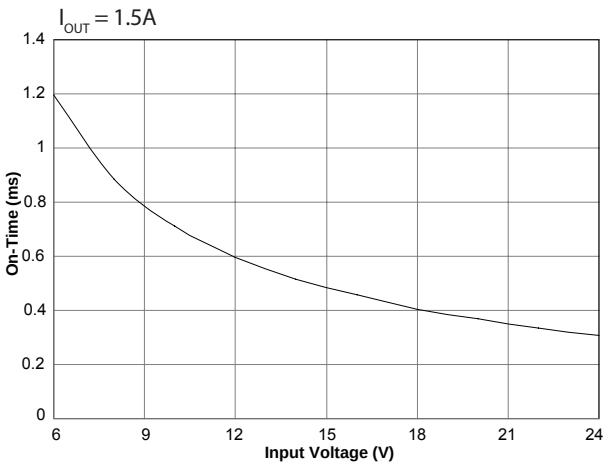
Switching Frequency



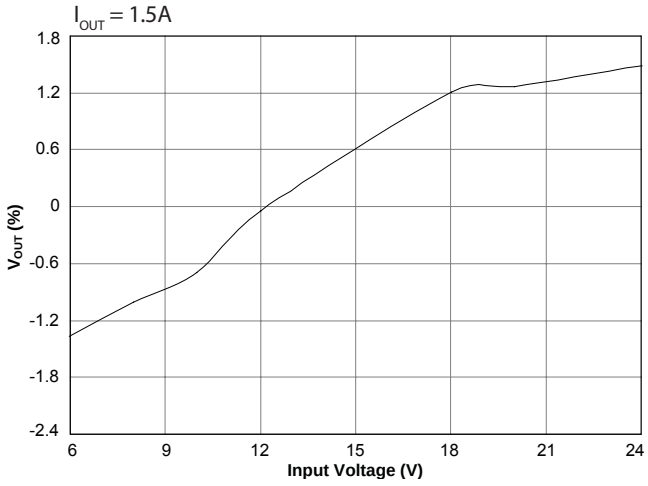
Switching Ripple



On-Time vs. V_{IN}



Line Regulation

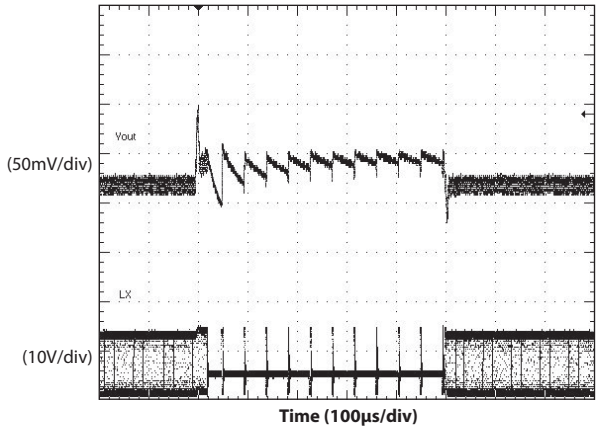


Typical Characteristics (continued)

Characteristics are based on a circuit with V_{IN} = 12V, L = 2.2µH (DCR = 35mΩ), C_{OUT} = 66µF, V_{OUT} = 3.3V, V_{LDO} = 5V, R_{TON} = 90.9kΩ.

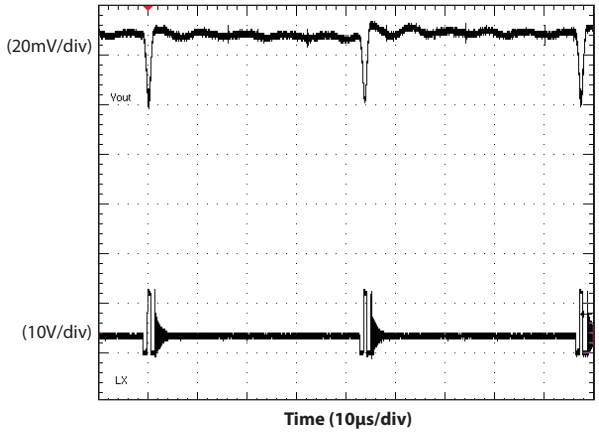
Transient Response

I_{OUT} = 3A to 0A



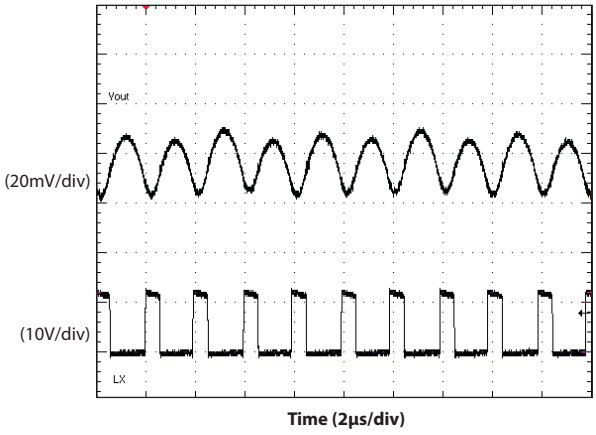
Power Save

I_{OUT} = 0A



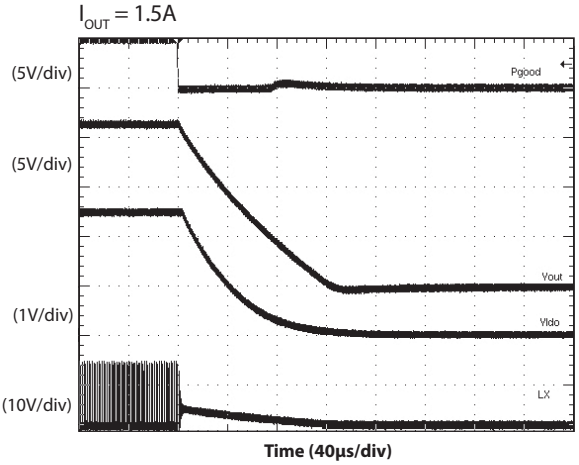
CCM

I_{OUT} = 1.5A



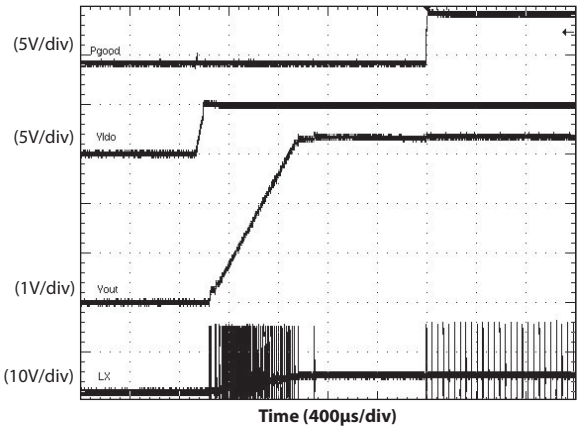
Shutdown

I_{OUT} = 1.5A



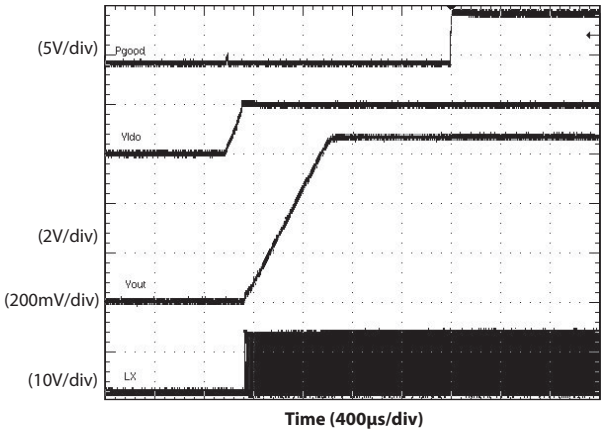
Start-up

I_{OUT} = 0A



Start-up

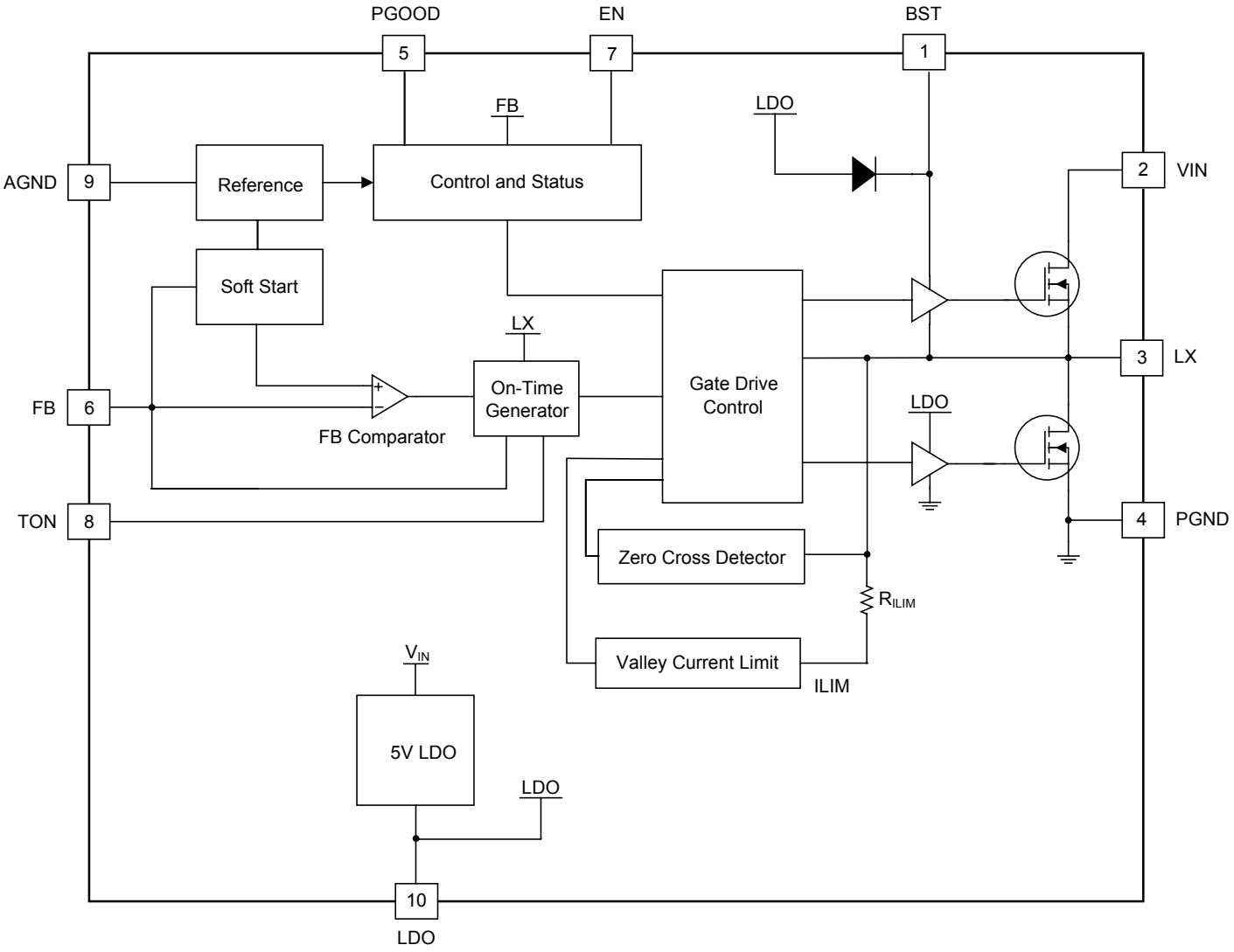
I_{OUT} = 1.5A



Pin Descriptions

Pin #	Pin Name	Pin Function
1	BST	Bootstrap pin — A capacitor is connected between BST to LX to develop the floating voltage for the high-side gate drive.
2	VIN	Power input supply voltage
3	LX	Switching (phase) node
4	PGND	Power ground
5	PGOOD	Open-drain power good indicator — High impedance indicates power is good. An external pull-up resistor is required.
6	FB	Feedback input for switching regulator — Connect to an external resistor divider from the output to program the output voltage.
7	EN	Enable input for switching regulator —Pull EN high to enable the part with ultrasonic power save mode enabled. Connect to AGND to disable the switching regulator. A voltage divider can be added between VIN and AGND pins for input UVLO functionality.
8	TON	On-time set input — Set the on-time by connecting a series resistor to AGND.
9	AGND	Analog Ground.
10	LDO	Output for the internal LDO and internal connection to the bias node — Decoupling capacitors are required to AGND and PGND regardless of the use of the LDO for external loads.
	PAD	Thermal pad for heatsinking purposes. (Not connected internally) Connect to AGND plane using multiple vias.

Block Diagram



Applications Information

Synchronous Buck Converter

The SC410 is a step down synchronous buck DC-DC regulator. The device is capable of 3A operation at very high efficiency in a tiny 3 x 3-10 pin package. The programmable operating frequency range of 200kHz – 1MHz enables the user to optimize the design for minimum board space and optimum efficiency.

The buck regulator employs pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response thereby lowering the size of the power components used in the system.

Input Voltage Range

The SC410 can operate with a wide input voltage ranging from 5.5V to 24V. The internal LDO generates a fixed 5V output that provides power for the bias of the SC410. The LDO can also provide additional power to an external load.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC410 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is divided down by the feedback resistor network and used as a PWM ramp signal. The ripple seen at the FB pin is used to trigger the on-time of the controller.

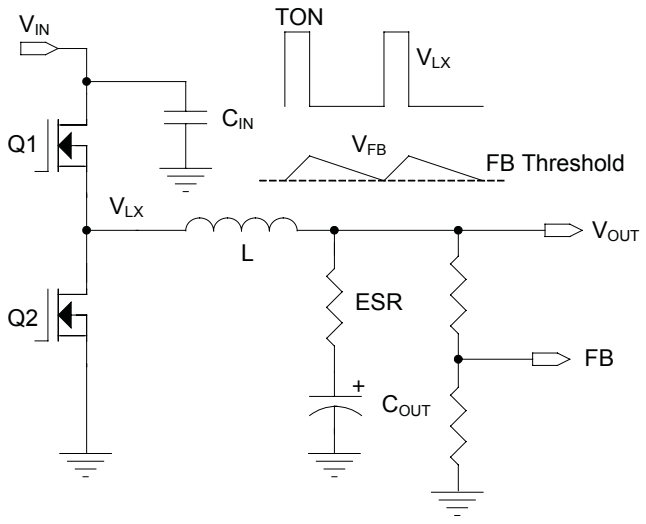


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the feedback ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by the output voltage value and V_{IN}. The period is proportional to output voltage and inversely proportional to input voltage. The value of the output voltage is obtained by filtering the voltage seen on the LX pin.

With this adaptive on-time design, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency during CCM compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

One-Shot Timer and Operating Frequency

The one-shot timer operates as shown in Figure 2. The feedback comparator output goes high when V_{FB} is less than the internal 750mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator, timing capacitor, and a low pass filter (LPF) which regenerates V_{OUT} from LX. One comparator input is connected to the filtered LX voltage, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

Applications Information (continued)

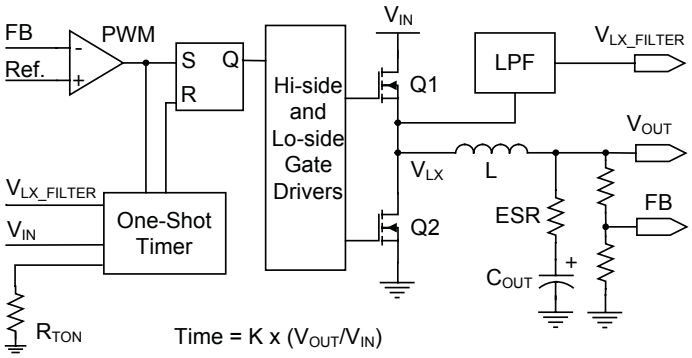


Figure 2 — On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state operating conditions in continuous conduction mode, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{t_{ON} \times V_{IN}}$$

The SC410 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide operating frequencies from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{1}{25pF \times f_{SW}} - 400\Omega \times \frac{V_{IN}}{V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{10 \times 1.5\mu A}$$

Immediately after the on-time, the DL (the drive signal for the low side FET) output drives high to turn on the low-side MOSFET. DL has a minimum high time of ~320ns, after which DL continues to stay high until one of the following occurs:

- V_{FB} falls below the 750mV reference
- The zero cross detector senses that the voltage on the LX node is below ground. PSAVE is activated 8 periods after the zero cross is detected.

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 750mV reference voltage, see Figure 3.

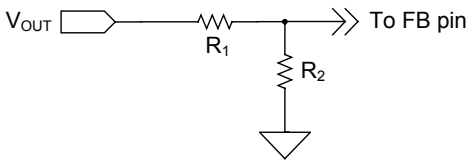


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.75 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

Enable Input

The EN input is used to enable or disable the switching regulator. When EN is low (grounded), the switching regulator and LDO are disabled and the SC410 is in its lowest power state. When disabled, the output power switches are tri-stated. When EN is higher than 0.8V, the internal LDO will be activated. The switching regulator remains off until the voltage at the EN pin exceeds 1.5V.

The EN pin can be used for implementing UVLO for the input voltage by configuring a voltage divider from VIN to EN to PGND.

Continuous Mode Operation

The SC410 operates in CCM (Continuous Conduction Mode) at larger load currents when the load is greater than or equal to half of the inductor ripple current (Figure 4). In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This mode of operation results in uniform frequency.

Applications Information (continued)

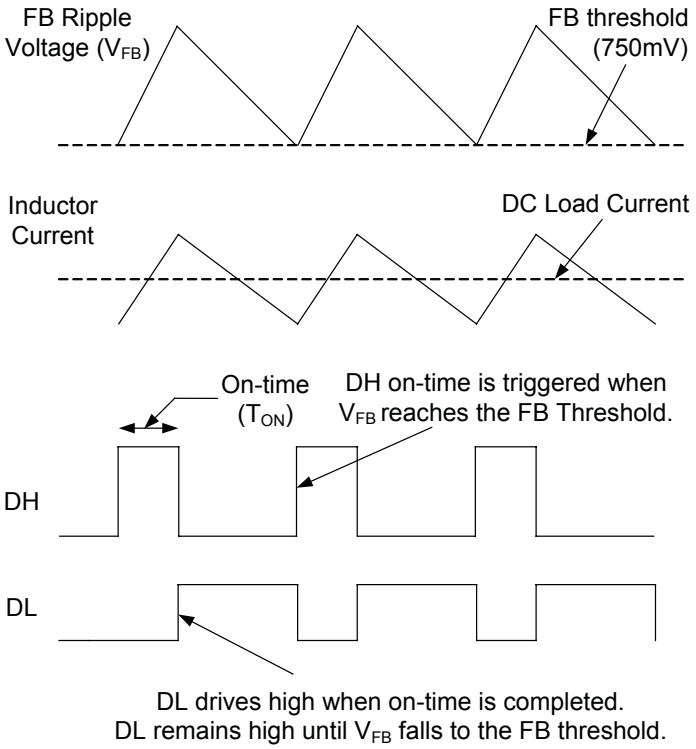


Figure 4 — Continuous Mode Operation

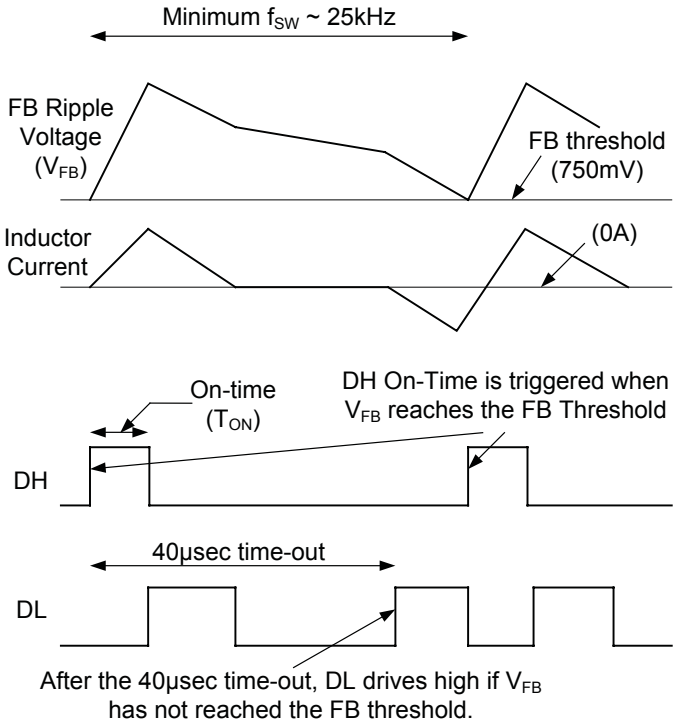


Figure 5 — Ultrasonic Power Save Operation

Ultrasonic Power Save Operation

The SC410 provides ultrasonic power save operation at light loads, with the minimum operating frequency fixed at 22kHz. This is accomplished using an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds 40µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 750mV threshold, the next DH on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

Because the on-times are forced to occur at intervals no greater than 40µs, the frequency will not fall below ~22kHz. Figure 5 shows ultrasonic power save operation.

Smart Power Save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shut-down. Smart power save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 825mV), the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 750mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. Figure 6 shows typical waveforms for the smart power save feature.

Applications Information (continued)

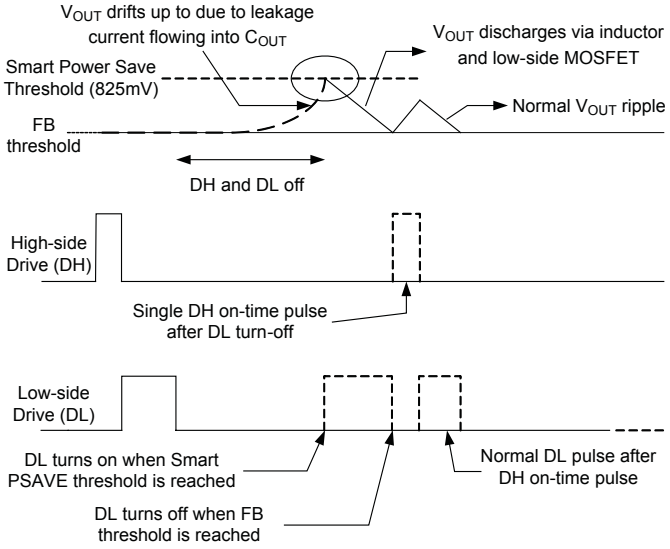


Figure 6 — Smart Power Save

Current Limit Protection

Programmable current limiting is accomplished by using the RDS_{ON} of the lower MOSFET for current sensing. The current limit is set by an internal resistor R_{ILIM}. The resistor connects from an ILIM node to the LX node which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~10µA current flows from the ILIM Node and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the RDS_{ON}. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM node will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by ILIM in Figure 7.

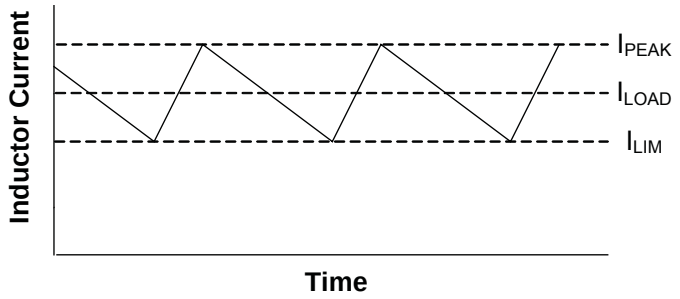


Figure 7 — Valley Current Limit

In the SC410, the valley current limit is set to 3A. This results in a peak inductor current of 3A plus the peak-to-peak ripple current. In this situation, the average (load) current through the inductor is 3A plus one-half the peak-to-peak ripple current.

The internal 10µA current source is temperature compensated at 2500ppm in order to provide tracking with the RDS_{ON}.

Peak Inductor Current

The peak current through the inductor and switching FETs must be less than 5A. The only way to meet this requirement is to select the switching frequency and inductor value so that the peak inductor current is less than or equal to 5A when the trough of the inductor current is 3A.

Soft start of PWM Regulator

Soft start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 750mV in ~1.8mV increments, using an internal ~500kHz oscillator. When the ramp voltage reaches 750mV, the ramp is ignored and the FB comparator switches over to a fixed 750mV threshold. During soft start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft start profile for a wide range of applications. Typical soft start ramp time is 850µs.

During soft start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output.

Power Good Output

The PGOOD (power good) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns to the nominal voltage. PGOOD is held low during soft start and activated approximately 1ms after V_{OUT} reaches regulation.

Applications Information (continued)

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold (900mV).

Output Over-Voltage Protection

OVP (Over-Voltage Protection) becomes active as soon as the device is enabled. The threshold is set at 750mV + 20% (900mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN input is toggled or V_{IN} is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls to 75% of its nominal voltage (falls to 562.5mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to turn off the MOSFETs. The controller stays off until EN is toggled or V_{IN} is cycled.

Over-Temperature Protection

If the temperature rises to 145°C the device will latch off. The device can be activated after the temperature is reduced below 145°C by cycling the EN pin.

V_{LDO} UVLO, and POR

UVLO (Under-Voltage Lock-Out) circuitry inhibits switching and tri-states the power FETs until V_{LDO} rises above 4.0V. An internal POR (Power-On Reset) occurs when V_{LDO} exceeds 4.0V, which resets the fault latch and soft start counter to begin the soft start cycle. The SC410 then begins a soft start cycle. The PWM will shut off if V_{LDO} falls below 3.7V.

Internal LDO Regulator

The SC410 has an internal regulator that supplies the bias voltage for the PWM controller. This LDO can also supply an additional external current for an external load through the LDO pin.

When activated, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. EN pin
2. V_{LDO} output voltage
3. VIN input voltage

While the EN pin is above 0.5V, the LDO will be activated. While the V_{LDO} output voltage remains below 4V (80% of the final LDO voltage), the LDO short-cicuit protection is enabled and limits the current to about 35mA. After the V_{LDO} exceeds 4.0V, then the LDO operates in its normal regulation mode where the current is limited to about 100mA.

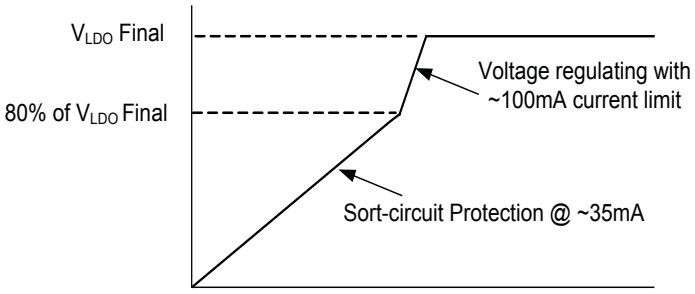


Figure 8 — LDO Start-Up

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

The two values of load current to evaluate are continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

Applications Information (continued)

The following values are used in this design example.

- V_{IN} = 12V ± 10%
- V_{OUT} = 3.3V ± 4%
- f_{SW} = 500kHz
- Load = 3A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 500kHz which results from using components selected for optimum size and cost.

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{1}{25pF \times f_{SW}} - 400\Omega \times \frac{V_{IN}}{V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

$$t_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

t_{ON} = 500 ns at 13.2V_{IN}, 3.3V_{OUT}, 500kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 78.5kΩ, use R_{TON} = 78.7kΩ

Now, t_{ON} = 501ns given that R_{TON} = 78.7kΩ.

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 2A then power-save operation will typically start for loads less than 1A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 75% of the maximum load current. Therefore ripple current will be 75% x 3A or 2.25A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2V - 3.3V) \times 501ns}{2.25A} = 2.204\mu H$$

A standard value of 2.2µH is selected. This gives a maximum I_{RIPPLE} of 2.53A. The peak ripple can be calculated by the equation, below where L_{TOL} is assumed to be an inductor tolerance of 20%.

$$I_{RIPPLE\_PEAK} = I_{RIPPLE\_MAX} \text{ x } (1 + L_{TOL}) = 2.705$$

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

$$I_{LSAT\_MIN} = I_{RIPPLE\_PEAK} \text{ X } 0.5 + I_{OUT} = 4.353$$

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$t_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 611ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(10.8V - 3.3V) \times 612ns}{2.2\mu H} = 2.08A$$

Applications Information (continued)

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is for the output voltage regulation to be ±4% under static conditions. The internal 750mV reference tolerance is 1%. Assuming a 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 132mV for a 3.3V output.

The maximum ripple current of 2.7A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{2 \times V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{132mV}{2.705A}$$

$$ESR_{MAX} = 48.8\ m\Omega$$

The output capacitance is chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L(1+L_{TOL}) \times \left(I_{OUT} + \frac{1}{2} \times I_{RIPPLE\_PEAK}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (132mV rise upon load release), and a 6A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{2.2\mu H(1+20\%)\left(3A + \frac{1}{2} \times 2.705A\right)^2}{(3.432V)^2 - (3.3V)^2}$$

$$COUT_{MIN} = 56\mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 750mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately V_{OUT}. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt. Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 3A + 1/2 \times 2.7A = 4.353A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 3A

$$C_{OUT} = I_{LPK} \times \frac{L \times (1+L_{TOL}) \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{d + I_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2A}{1\mu s}$$

This causes the output current to move from 3A to 0A in 4.8µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 4.353A \times \frac{2.2\mu H(1+20\%) \times \frac{4.353A}{3.3V} - \frac{3A}{2A} \times 1\mu s}{2(3.432V - 3.3V)}$$

Note that C_{OUT} is much smaller in this example, 33µF compared to 56µF based on a worst-case load release. To meet the two design criteria of minimum 56µF, select three capacitors rated at 22µF and 15mΩ ESR.

Applications Information (continued)

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout.

An alternate method to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 9. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be provided for this capacitor.

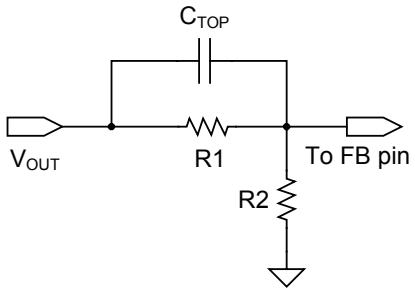


Figure 9 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple method of solving this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is a decrease in load regulation.

ESR Requirements

A minimum ESR is required for two reasons. The first reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications, the total output ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Using Ceramic Output Capacitors

When applications use ceramic output capacitors, the ESR is normally too small to meet the previously stated ESR criteria. In these applications it is necessary to add a small signal injection network as shown in Figure 10. In this network R_L and C_L filter the LX switching waveform to generate an in-phase ripple voltage comparable to the ripple seen on higher ESR capacitors. C_C is a coupling capacitor used to AC couple the generated ripple onto the FB pin.

Applications Information (continued)

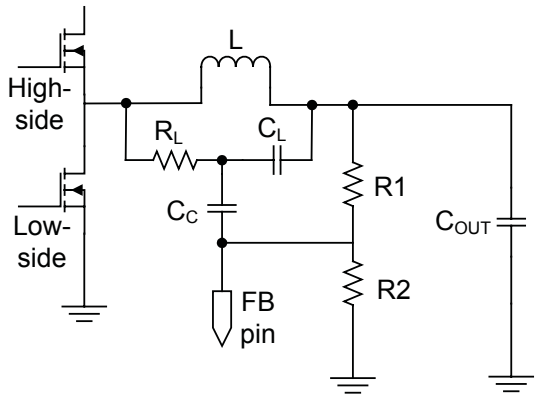


Figure 10 — Signal Injection Circuit

The values of R_L, C_L, and C_C are dependent on the conditions of the specific application such as V_{IN}, V_{OUT}, f_{SW} and I_{OUT}.

Select a value for C_L, like 10nF. Using C_L, calculate R_L as shown in the following equation:

$$R_L = \frac{L}{C_L \times DCR}$$

Where L is the inductor value and DCR is the resistance of the inductor.

The value for C_C can be between C_{C_MIN} and C_{C_MAX}.

$$C_{C\_MIN} = \frac{t_{ON}}{R_{EQ}}$$

$$C_{C\_MAX} = \frac{T}{R_{EQ}}$$

Where $T = 1/f_{SW}$ and R_{EQ} is represented by the following equation.

$$R_{EQ} = R_{BOTTOM} \times \frac{R_{TOP}}{R_{BOTTOM} + R_{TOP}}$$

It is beneficial to use the smallest value of C_C that provides stability and enough voltage ripple at feedback. Larger values of C_C may negatively affect the load regulation performance.

Output Voltage Dropout

The output voltage adjustable range for continuous-conduction operation is limited by the fixed 320ns (typical) minimum off-time. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy — V_{OUT} Controller

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 750mV, ±1%.

The on-time pulse from the SC410 in the design example is calculated to give a pseudo-fixed frequency of 500kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors may result in up to an additional 1% error. If tighter DC accuracy is required, resistors with lower tolerances should be used.

Applications Information (continued)

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variation

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the power FET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to fall slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT} and V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

Applications Information (continued)

PCB Layout Guidelines

The optimum layout for the SC410 is shown in Figure 11. This layout shows an integrated FET buck regulator with a maximum current of 3A. The total PCB area is approximately 19.1mm x 11.3mm.

Critical Layout Guidelines

The following critical layout guidelines must be followed to ensure proper performance of the device.

- IC Decoupling capacitors
- PGND plane
- AGND island
- FB and other analog control signals
- BST and LX
- Capacitors and Current Loops

IC Decoupling Capacitors

- A 0.1 µF capacitor must be located as close as possible to the IC and directly connected to pins 10 (LDO) and 9 (AGND).
- All other decoupling capacitors must be located as close as possible to the IC.

PGND Plane

- PGND requires its own copper plane with no other signal traces routed on it.
- Copper planes, multiple vias, and wide traces are needed to connect PGND to input capacitors, output capacitors, and the PGND pins on the IC.
- The PGND copper area between the input capacitors, output capacitors, and PGND pins must be as small as and as compact as possible to reduce the area of the PCB that is exposed to noise due to current flow on this node.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

AGND Island

- AGND should have its own island of copper with no other signal traces routed on this layer that connects the AGND pins and pad of the IC to the analog control components.
- All of the components for the analog control circuitry should be located so that the connections

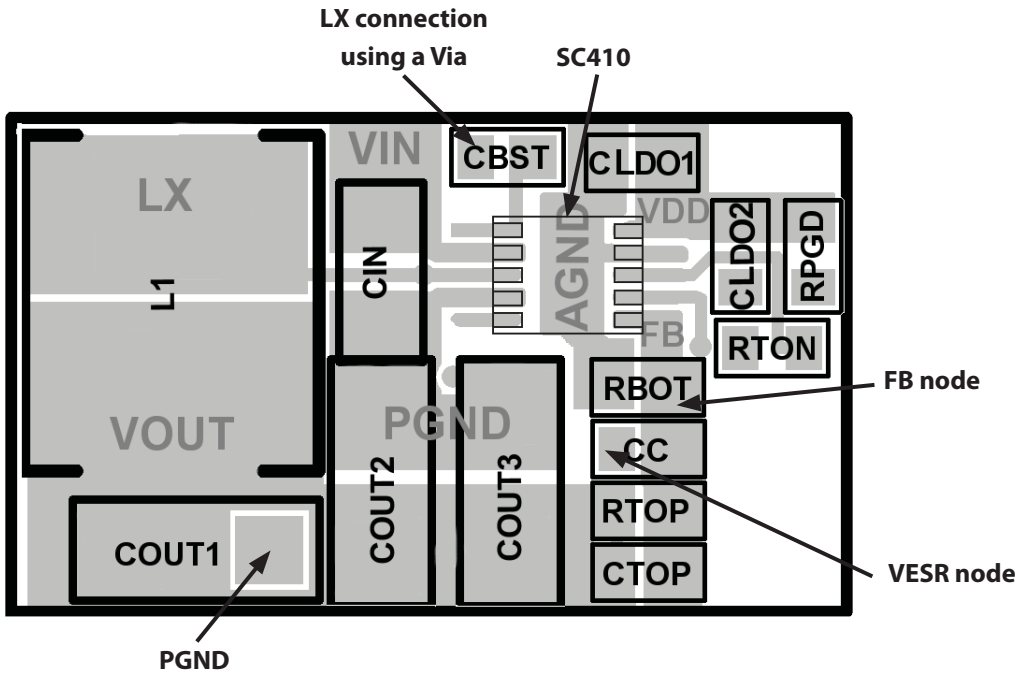


Figure 11 — PCB Layout

Applications Information (continued)

to AGND are done by wide copper traces or vias down to AGND.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

FB and Other Analog Control Signals

- The connection from the V_{OUT} power to the analog control circuitry must be routed from the output capacitors and located on a quiet layer.
- The traces between V_{OUT} and the analog control circuitry (AGND, and FB pins) must be as short as possible. The traces must also be routed away from noise sources, such as BST, LX, VIN, and PGND between the input capacitors, output capacitors, and the IC.
- The TON node must be as short as possible to ensure the best accuracy for the on time.
- The feedback components for the switcher need to be as close to the FB pin of the IC as possible to reduce the possibility of noise corrupting these analog signals.

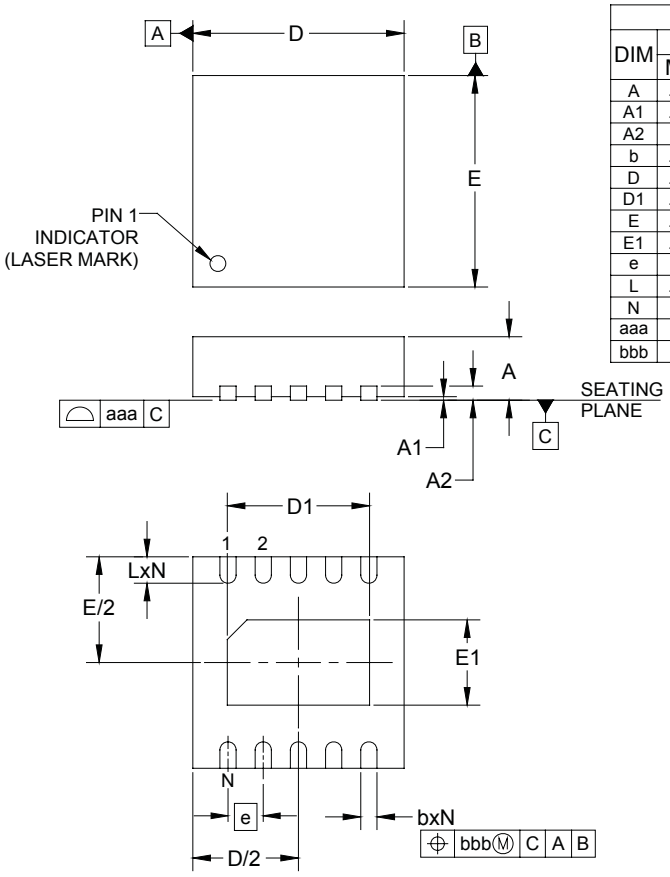
BST and LX

- LX and BST are very noisy nodes and must be carefully routed to minimized the PCB area that is exposed to these signals.
- The connections for the boost capacitor between the IC and LX must be short and directly connected to the LX (pin 3).
- The LX node between the IC and the inductor should be wide enough to handle the inductor current and short enough to eliminate the possibility of LX noise corrupting other signals.

Capacitors and Current Loops

- The current loops between the input capacitors, the IC, the inductor, and the output capacitors must be as close as possible to each other to reduce IR drop across copper planes and traces.
- All bypass and output capacitors must be connected as close as possible to their respective pin on the IC.

Outline Drawing — MLPD-10 3x3

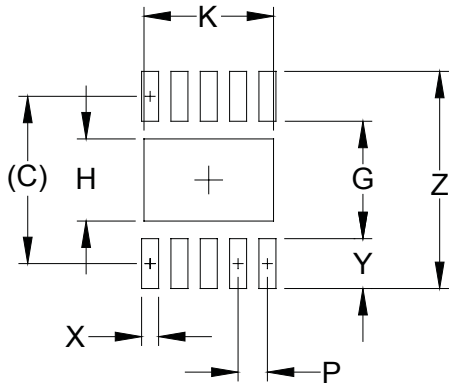


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.009	.011	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.074	.079	.083	1.87	2.02	2.12
E	.114	.118	.122	2.90	3.00	3.10
E1	.042	.048	.052	1.06	1.21	1.31
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — MLPD-10 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.055	1.40
K	.087	2.20
P	.020	0.50
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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