# NCV4276, NCV4276A

# 400 mA Low-Drop Voltage Regulator

The NCV4276 is a 400 mA output current integrated low dropout regulator family designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with fixed output voltage options of 1.8 V and 2.5 V with 4% output voltage accuracy while the 3.3 V, 5.0 V, and adjustable voltage versions are available either in 2% or 4% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and inhibit for control of the state of the output voltage. The NCV4276 family is available in DPAK and $D^2PAK$ surface mount packages. The output is stable over a wide output capacitance and ESR range.

### Features

- 2.5 V and 1.8 V ±4% Output Voltage
- 3.3 V, 5.0 V, and Adjustable Voltage Version (from 2.5 V to 20 V) ±4% or ±2% Output Voltage
- 400 mA Output Current
- 500 mV (max) Dropout Voltage (5.0 V Output)
- Inhibit Input
- Very Low Current Consumption
- Fault Protection
  - ♦ +45 V Peak Transient Voltage
  - ♦ −42 V Reverse Voltage
  - ♦ Short Circuit
  - ♦ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- Pb−Free Packages are Available



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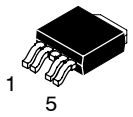
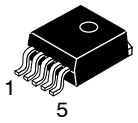



**DPAK**
**5−PIN**
**DT SUFFIX**
**CASE 175AA**




**$D^2PAK$**
**5−PIN**
**DS SUFFIX**
**CASE 936A**

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 20 of this data sheet.

### ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 21 of this data sheet.

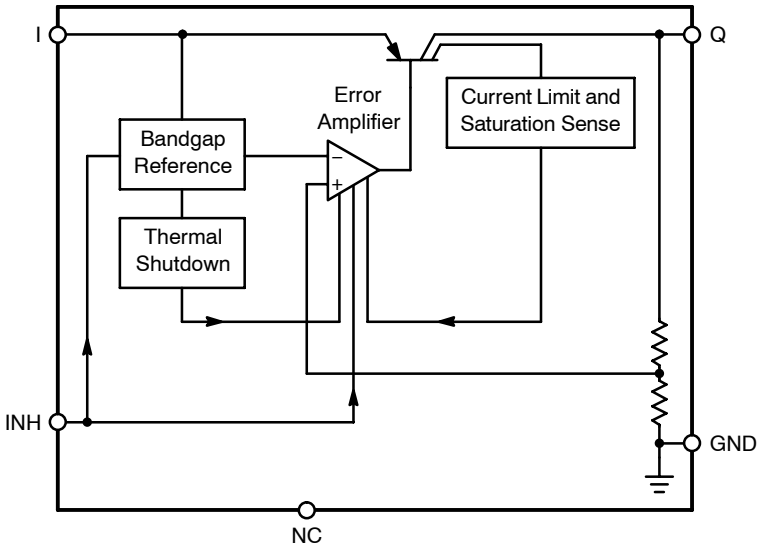



**Figure 1. 4276 Block Diagram**

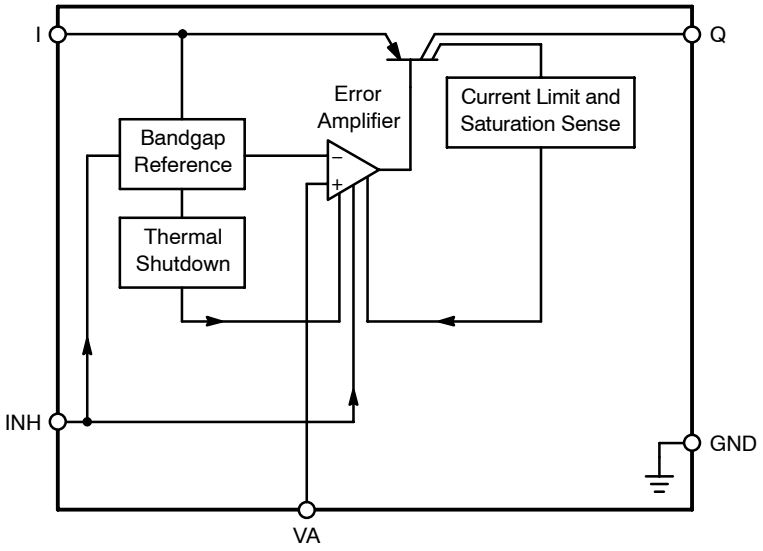



**Figure 2. 4276 Adjustable Block Diagram**

## PIN FUNCTION DESCRIPTION

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | I | Input; Battery Supply Input Voltage. |
| 2 | INH | Inhibit; Set low−to inhibit. |
| 3 | GND | Ground; Pin 3 internally connected to heatsink. |
| 4 | NC / VA | Not connected for fixed voltage version / Voltage Adjust Input for adjustable voltage version; use an external voltage divider to set the output voltage |
| 5 | Q | Use 22 μF, ESR < 2.5 Ω at 10 kHz to ground with the 5.0 V and adjustable regulators. See Figures 3, 4, and 5. Use 10 μF, ESR < 1.8 Ω at 10 kHz to ground with the 3.3 V, 2.5 V, and 1.8 V regulators. See Figures 3 and 6. |

## MAXIMUM RATINGS*

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage | $V_I$ | −42 | 45 | V |
| Input Peak Transient Voltage | $V_I$ | − | 45 | V |
| Inhibit INH Voltage | $V_{INH}$ | −42 | 45 | V |
| Output Voltage | $V_Q$ | −1.0 | 40 | V |
| Ground Current | $I_q$ | − | 100 | mA |
| Input Voltage Operating Range | $V_I$ | $V_Q$ + 0.5 V or 4.5 V (Note 1) | 40 | V |
| ESD Susceptibility (Human Body Model)<br>(Machine Model)<br>(Charged Device Model) | <br>−<br>− | <br>4.5<br>250<br>1.25 | <br>−<br>−<br>− | <br>kV<br>V<br>kV |
| Junction Temperature | $T_J$ | −40 | 150 | °C |
| Storage Temperature | $T_{stg}$ | −50 | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

## LEAD TEMPERATURE SOLDERING REFLOW (Note 2)

| | | | | |
|---|---|---|---|---|
| Lead Temperature Soldering | $T_{SLD}$ | | | °C |
| Reflow (SMD styles only), Leaded, 60−150 s above 183, 30 s max at peak | | − | 240 | |
| Reflow (SMD styles only), Lead Free, 60−150 s above 217, 40 s max at peak | | − | 265 | |
| Wave Solder (through hole styles only), 12 sec max | | − | 310 | |

## THERMAL CHARACTERISTICS

| Characteristic | Test Conditions (Typical Value) | | Unit |
|---|---|---|---|
| **DPAK 5−PIN PACKAGE** | | | |
| | **Min Pad Board** (Note 3) | **1″ Pad Board** (Note 4) | |
| Junction−to−Tab (psi−JLx, $\psi_{JLx}$) | 4.2 | 4.7 | C/W |
| Junction−to−Ambient ($R_{\theta JA}$, $\theta_{JA}$) | 100.9 | 46.8 | C/W |
| **D²PAK 5−PIN PACKAGE** | | | |
| | **0.4 sq. in. Spreader Board** (Note 5) | **1.2 sq. in. Spreader Board** (Note 6) | |
| Junction−to−Tab (psi−JLx, $\psi_{JLx}$) | 3.8 | 4.0 | C/W |
| Junction−to−Ambient ($R_{\theta JA}$, $\theta_{JA}$) | 74.8 | 41.6 | C/W |

1. Minimum $V_I$ = 4.5 V or ($V_Q$ + 0.5 V), whichever is higher.
2. Per IPC / JEDEC J−STD−020C.
3. 1 oz. copper, 0.26 inch$^2$ (168 mm$^2$) copper area, 0.062″ thick FR4.
4. 1 oz. copper, 1.14 inch$^2$ (736 mm$^2$) copper area, 0.062″ thick FR4.
5. 1 oz. copper, 0.373 inch$^2$ (241 mm$^2$) copper area, 0.062″ thick FR4.
6. 1 oz. copper, 1.222 inch$^2$ (788 mm$^2$) copper area, 0.062″ thick FR4.

**ELECTRICAL CHARACTERISTICS** ($V_I$ = 13.5 V; –40°C < $T_J$ < 150°C; unless otherwise noted.)

| Characteristic | Symbol | Test Conditions | NCV4276 | | | NCV4276A | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **OUTPUT** | | | | | | | | | |
| Output Voltage, 5.0 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 400 mA, 6.0 V < $V_I$ < 28 V | 4.8 | 5.0 | 5.2 | 4.9 | 5.0 | 5.1 | V |
| Output Voltage, 5.0 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 200 mA, 6.0 V < $V_I$ < 40 V | 4.8 | 5.0 | 5.2 | 4.9 | 5.0 | 5.1 | V |
| Output Voltage, 3.3 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 400 mA, 4.5 V < $V_I$ < 28 V | 3.168 | 3.3 | 3.432 | 3.234 | 3.3 | 3.366 | V |
| Output Voltage, 3.3 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 200 mA, 4.5 V < $V_I$ < 40 V | 3.168 | 3.3 | 3.432 | 3.234 | 3.3 | 3.366 | V |
| Output Voltage, 2.5 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 400 mA, 4.5 V < $V_I$ < 28 V | 2.4 | 2.5 | 2.6 | – | – | – | V |
| Output Voltage, 2.5 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 200 mA, 4.5 V < $V_I$ < 40 V | 2.4 | 2.5 | 2.6 | – | – | – | V |
| Output Voltage, 1.8 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 400 mA, 4.5 V < $V_I$ < 28 V | 1.728 | 1.8 | 1.872 | – | – | – | V |
| Output Voltage, 1.8 V Version | $V_Q$ | 5.0 mA < $I_Q$ < 200 mA, 4.5 V < $V_I$ < 40 V | 1.728 | 1.8 | 1.872 | – | – | – | V |
| Output Voltage, Adjustable Version | $AV_Q$ | 5.0 mA < $I_Q$ < 400 mA<br>$V_Q$+1 < $V_I$ < 40 V<br>$V_I$ > 4.5 V | –4% | – | +4% | –2% | – | +2% | V |
| Output Current Limitation | $I_Q$ | $V_Q$ = 90% $V_{QTYP}$ ($V_{QTYP}$ = 2.5 V for ADJ version) | 400 | 700 | 1100 | 400 | 700 | 1100 | mA |
| Quiescent Current (Sleep Mode)<br>$I_q = I_I - I_Q$ | $I_q$ | $V_{INH}$ = 0 V | – | – | 10 | – | – | 10 | μA |
| Quiescent Current, $I_q = I_I - I_Q$ | $I_q$ | $I_Q$ = 1.0 mA | – | 130 | 220 | – | 130 | 200 | μA |
| Quiescent Current, $I_q = I_I - I_Q$ | $I_q$ | $I_Q$ = 250 mA | – | 10 | 15 | – | 10 | 15 | mA |
| Quiescent Current, $I_q = I_I - I_Q$ | $I_q$ | $I_Q$ = 400 mA | – | 25 | 35 | – | 25 | 35 | mA |
| Dropout Voltage,<br>5.0 V Version<br>3.3 V Version<br>2.5 V Version<br>1.8 V Version<br>Adjustable Version | $V_{DR}$ | $I_Q$ = 250 mA,<br>$V_{DR} = V_I - V_Q$<br>$V_I$ = 5.0 V<br>$V_I$ = 4.5 V<br>$V_I$ = 4.5 V<br>$V_I$ = 4.5 V<br>$V_I$ > 4.5 V | <br>–<br>–<br>–<br>–<br>– | <br>250<br>–<br>–<br>–<br>250 | <br>500<br>1.332<br>2.1<br>2.772<br>500 | <br>–<br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>–<br>250 | <br>–<br>–<br>–<br>–<br>500 | <br>mV<br>V<br>V<br>V<br>mV |
| Dropout Voltage (5.0 V Version) | $V_{DR}$ | $I_Q$ = 250 mA (Note 7) | – | – | – | – | 250 | 500 | mV |
| Load Regulation | $\Delta V_{Q,LO}$ | $I_Q$ = 5.0 mA to 400 mA | – | 10 | 35 | – | 3.0 | 20 | mV |
| Line Regulation | $\Delta V_Q$ | $\Delta V_I$ = 12 V to 32 V,<br>$I_Q$ = 5.0 mA | – | 2.5 | 25 | – | 4.0 | 15 | mV |
| Power Supply Ripple Rejection | PSRR | $f_r$ = 100 Hz, $V_r$ = 0.5 $V_{PP}$ | – | 60 | – | – | 54 | – | dB |
| Temperature Output Voltage Drift | $d_{VQ/dT}$ | – | – | 0.5 | – | – | 0.5 | – | mV/K |
| **INHIBIT** | | | | | | | | | |
| Inhibit Voltage, Output High | $V_{INH}$ | $V_Q \geq V_{QMIN}$ | – | 2.8 | 3.5 | – | 2.3 | 3.5 | V |
| Inhibit Voltage, Output Low (Off) | $V_{INH}$ | $V_Q \leq$ 0.1 V | 0.5 | 1.7 | – | 0.5 | 2.2 | – | V |
| Input Current | $I_{INH}$ | $V_{INH}$ = 5.0 V | 5.0 | 10 | 20 | 5.0 | 10 | 20 | μA |
| **THERMAL SHUTDOWN** | | | | | | | | | |
| Thermal Shutdown Temperature* | $T_{SD}$ | $I_Q$ = 5.0 mA | 150 | – | 210 | 150 | – | 210 | °C |

*Guaranteed by design, not tested in production.

7. Measured when the output voltage $V_Q$ has dropped 100 mV from the nominal valued obtained at V = 13.5 V.

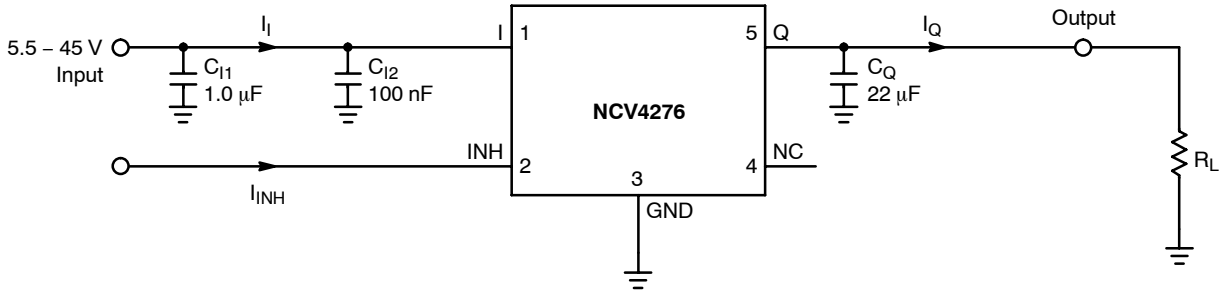



**Figure 3. Applications Circuit; Fixed Voltage Version**

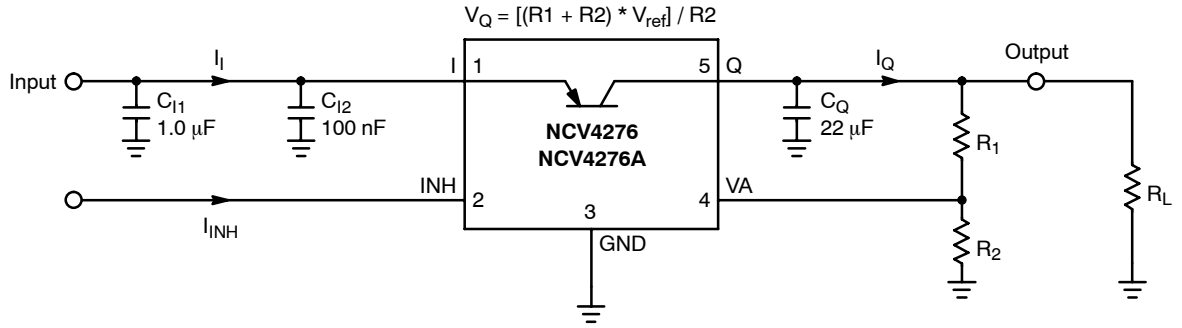



**Figure 4. Applications Circuit; Adjustable Voltage Version**

## TYPICAL PERFORMANCE CHARACTERISTICS

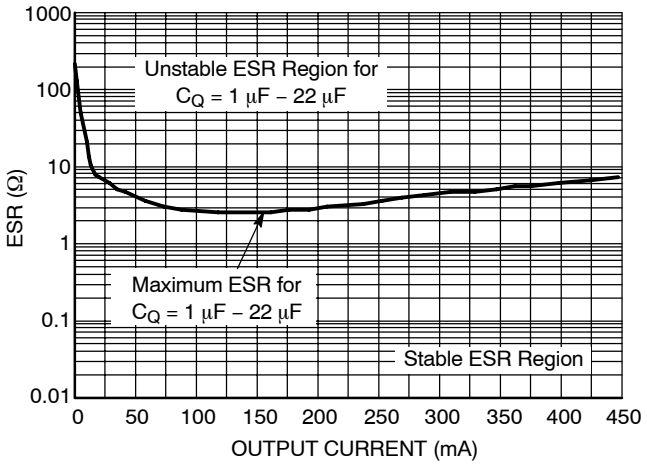



**Figure 5. Output Stability with Output Capacitor ESR, 5.0 V and Adjustable Regulator**

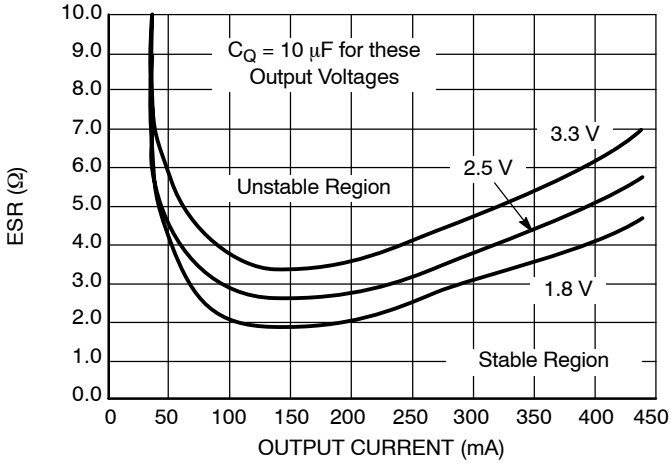



**Figure 6. Output Stability with Output Capacitor ESR, 1.8 V, 2.5 V, 3.3 V Regulators**

## TYPICAL PERFORMANCE CHARACTERISTICS – 4276 Version

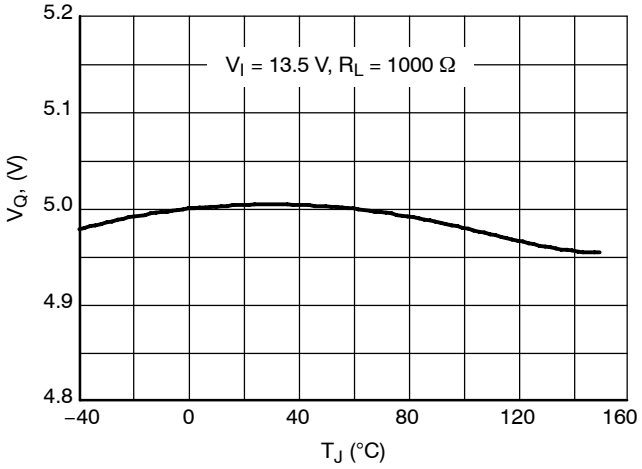



**Figure 7. Output Voltage $V_Q$ vs. Temperature $T_J$, 5.0 V Version**

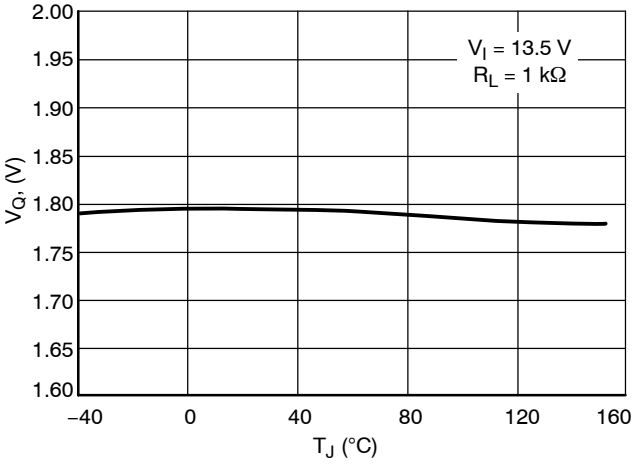



**Figure 8. Output Voltage $V_Q$ vs. Junction Temperature $T_J$, 1.8 V Version**

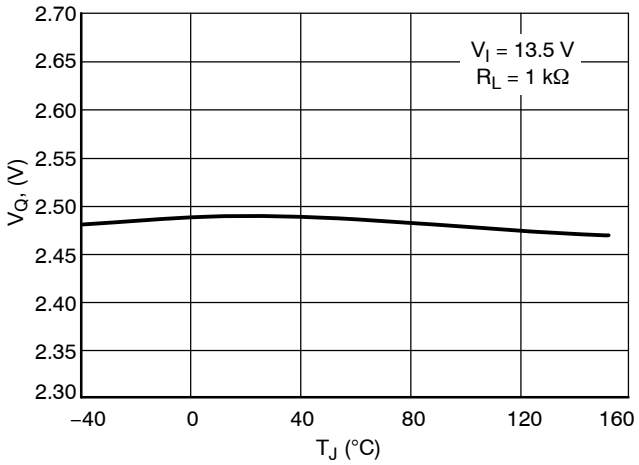



**Figure 9. Output Voltage $V_Q$ vs. Junction Temperature $T_J$, 2.5 V Version**

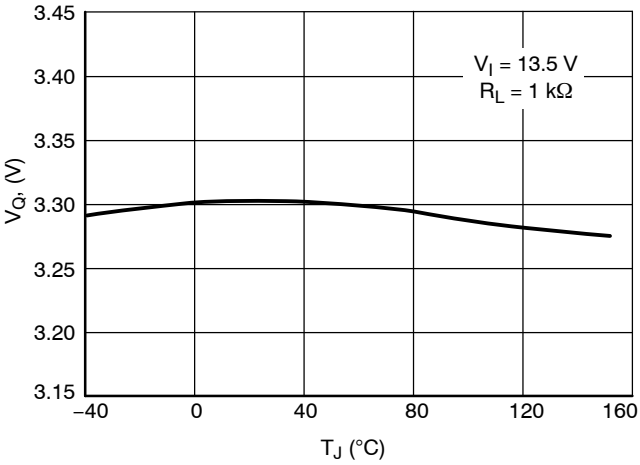



**Figure 10. Output Voltage $V_Q$ vs. Junction Temperature $T_J$, 3.3 V Version**

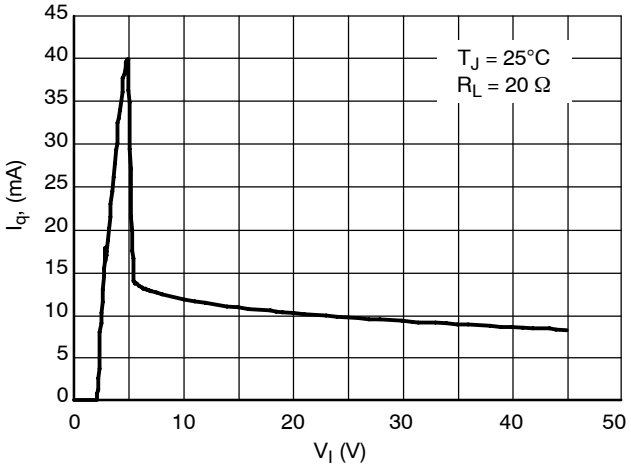



**Figure 11. Current Consumption $I_q$ vs. Input Voltage $V_I$, 5.0 V Version**

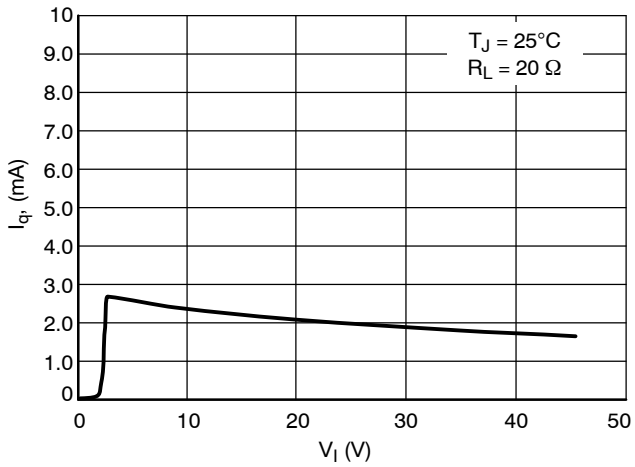



**Figure 12. Current Consumption $I_q$ vs. Input Voltage $V_I$, 1.8 V Version**

## TYPICAL PERFORMANCE CHARACTERISTICS – 4276 Version

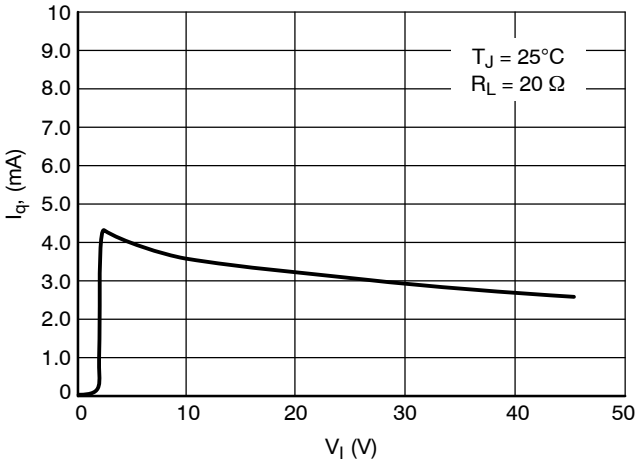



**Figure 13. Current Consumption $I_q$ vs. Input Voltage $V_I$, 2.5 V Version**

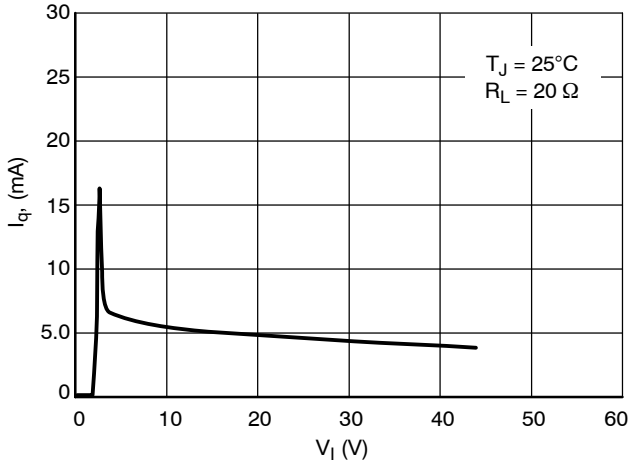



**Figure 14. Current Consumption $I_q$ vs. Input Voltage $V_I$, 3.3 V Version**

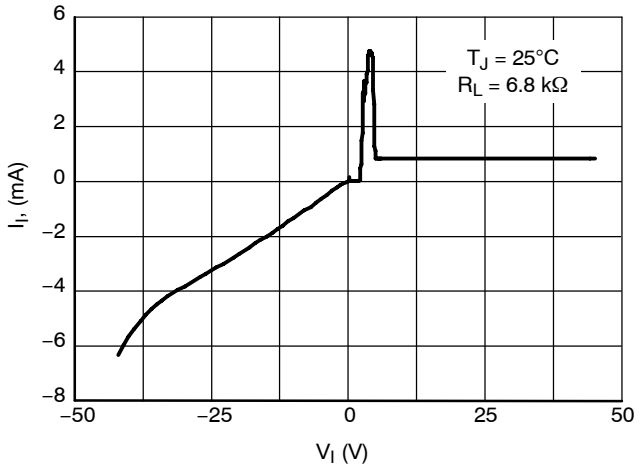



**Figure 15. High Voltage Behavior**

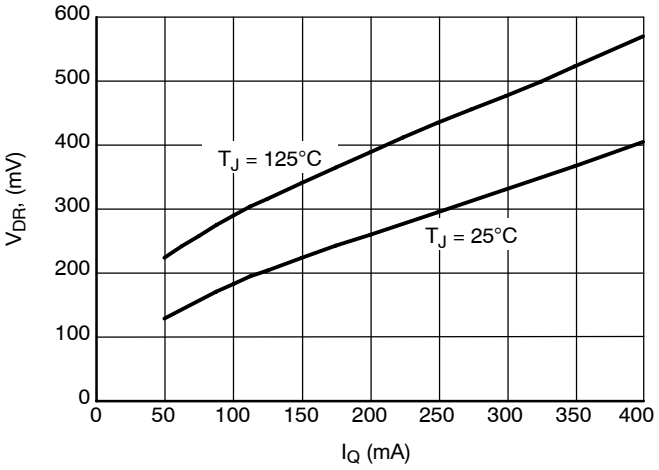



**Figure 16. Dropout Voltage $V_{DR}$ vs. Output Current $I_Q$, 5.0 V Version**

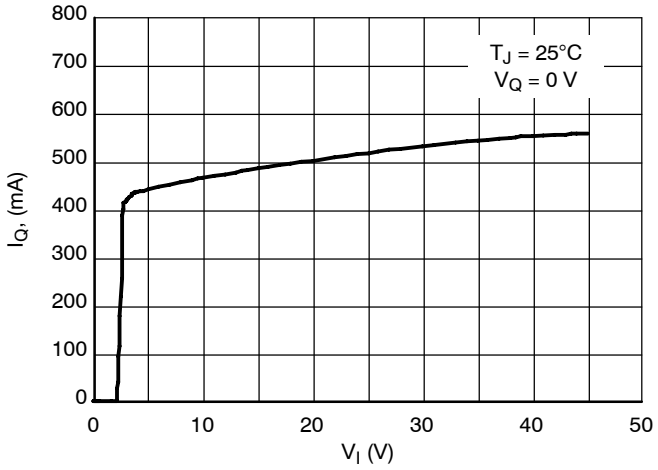



**Figure 17. Maximum Output Current $I_Q$ vs. Input Voltage $V_I$**

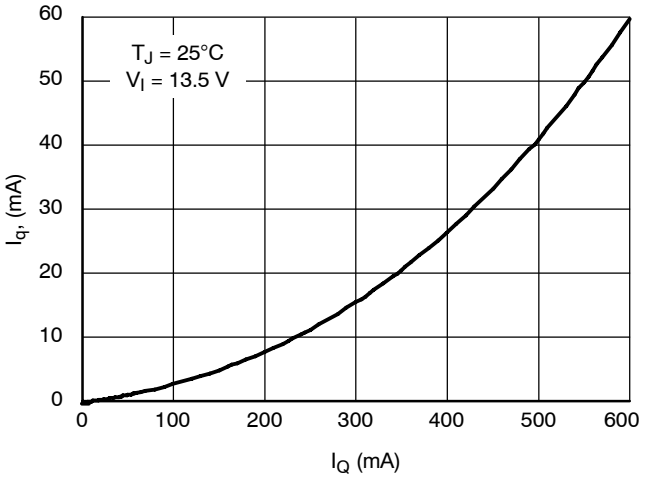



**Figure 18. Current Consumption $I_q$ vs. Output Current $I_Q$ (High Load)**

## TYPICAL PERFORMANCE CHARACTERISTICS – 4276 Version

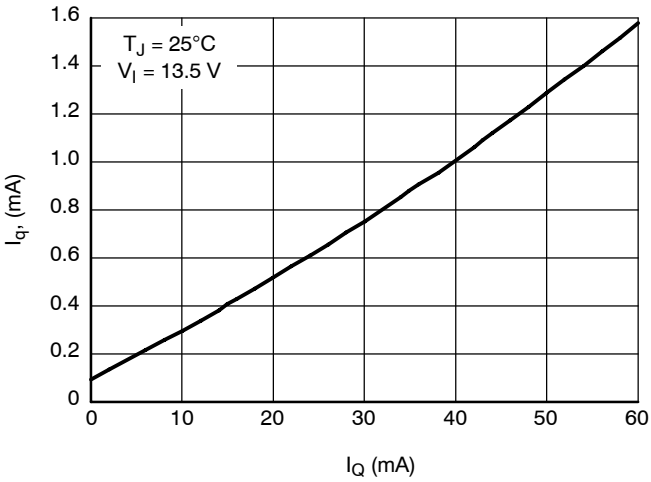



**Figure 19. Current Consumption $I_q$ vs. Output Current $I_Q$ (Low Load)**

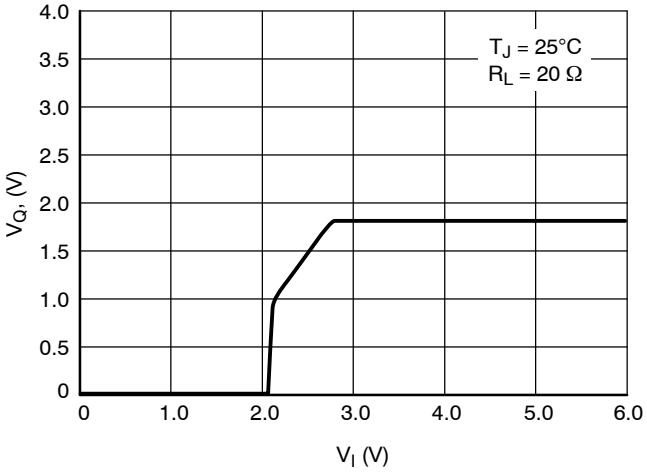



**Figure 20. Output Voltage $V_Q$ vs. Input Voltage $V_I$, 1.8 V Version**

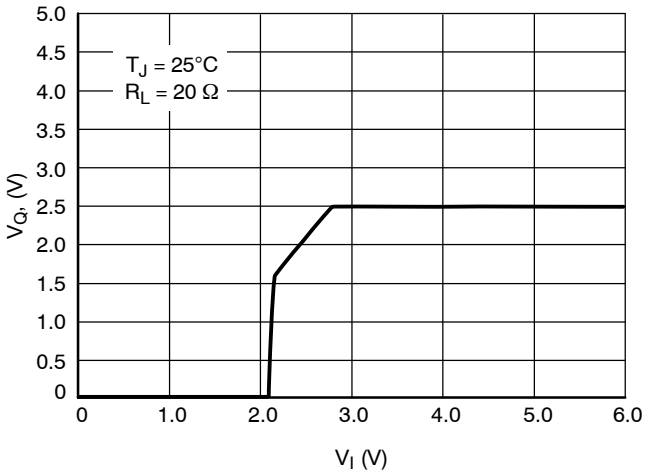



**Figure 21. Output Voltage $V_Q$ vs. Input Voltage $V_I$, 2.5 V Version**

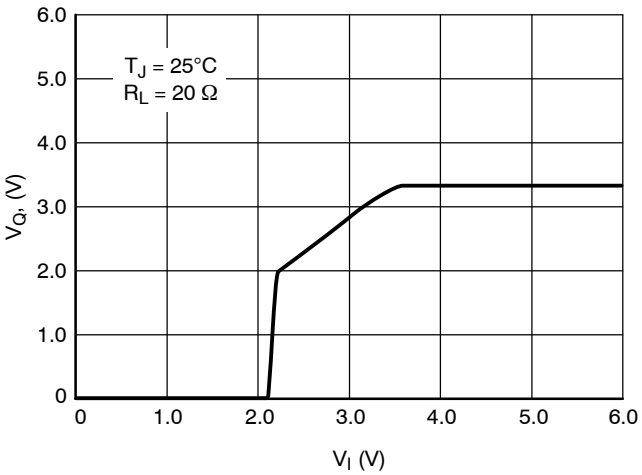



**Figure 22. Output Voltage $V_Q$ vs. Input Voltage $V_I$, 3.3 V Version**

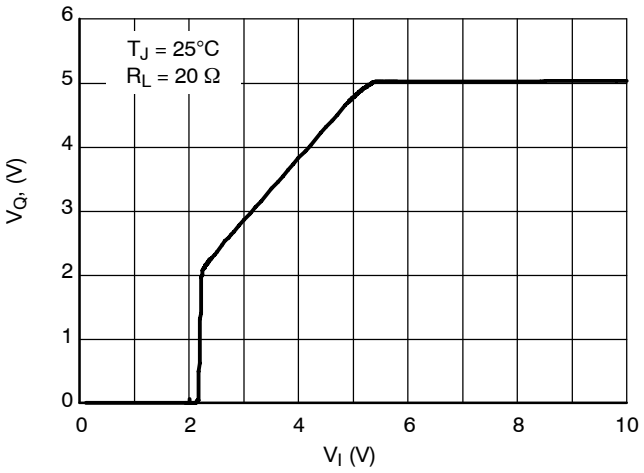



**Figure 23. Output Voltage $V_Q$ vs. Input Voltage $V_I$, 5.0 V Version**

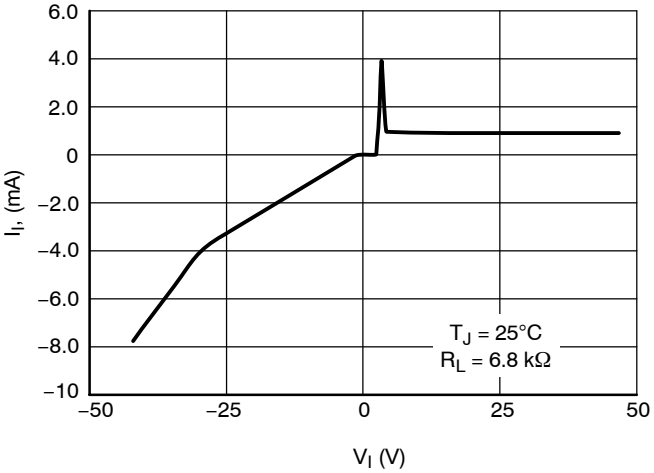



**Figure 24. Input Current $I_I$ vs. Input Voltage $V_I$, 5.0 V Version**

## TYPICAL PERFORMANCE CHARACTERISTICS – 4276 Version

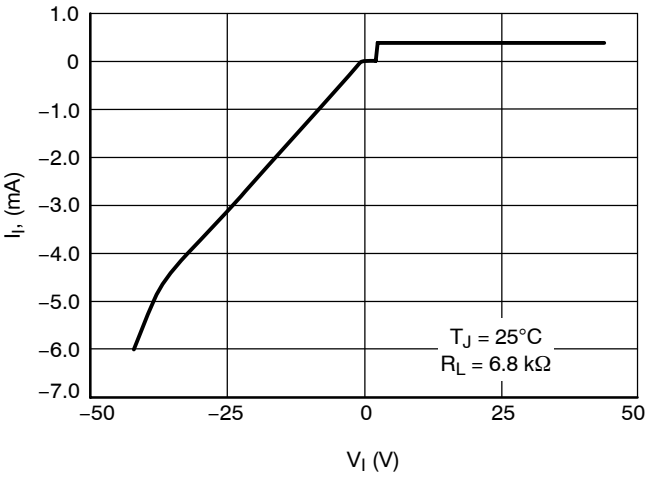



**Figure 25. Input Current $I_I$ vs. Input Voltage $V_I$, 1.8 V Version**

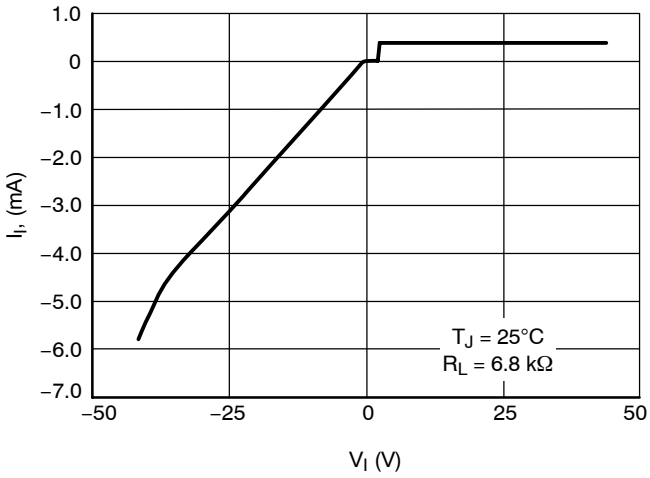



**Figure 26. Input Current $I_I$ vs. Input Voltage $V_I$, 2.5 V Version**

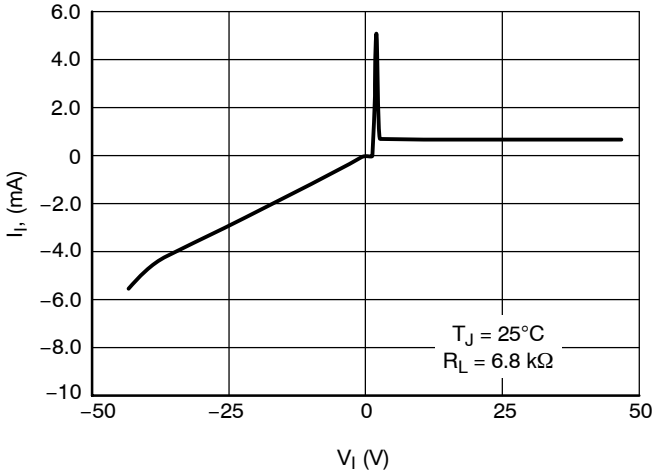



**Figure 27. Input Current $I_I$ vs. Input Voltage $V_I$, 3.3 V Version**

## TYPICAL PERFORMANCE CHARACTERISTICS – 4276A Version

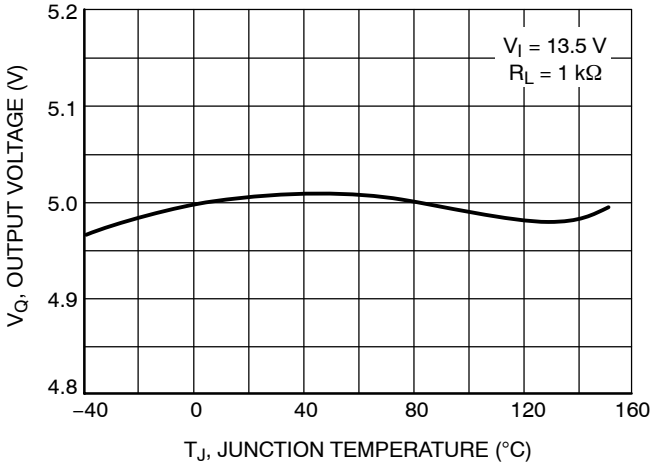



**Figure 28. Output Voltage $V_Q$ vs. Junction Temperature $T_J$, 5.0 V Version**

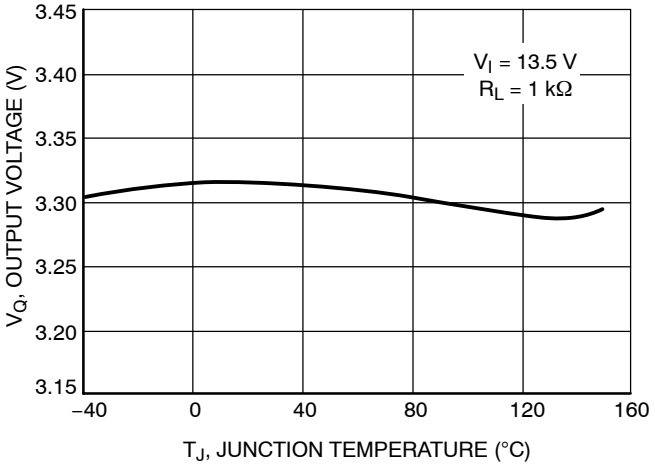



**Figure 29. Output Voltage $V_Q$ vs. Junction Temperature $T_J$, 3.3 V Version**

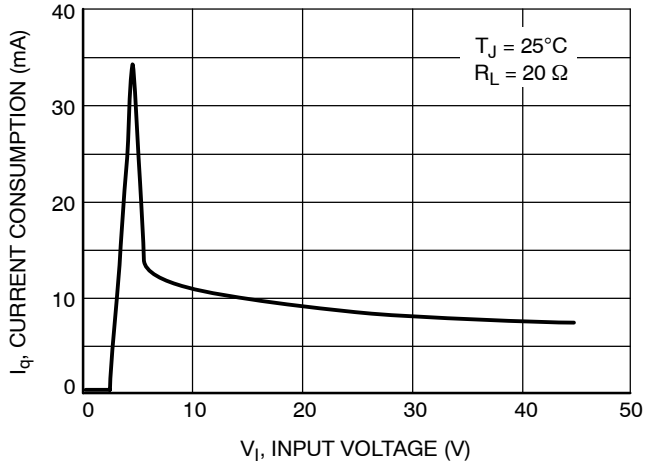



**Figure 30. Current Consumption $I_q$ vs. Input Voltage $V_I$, 5.0 V Version**

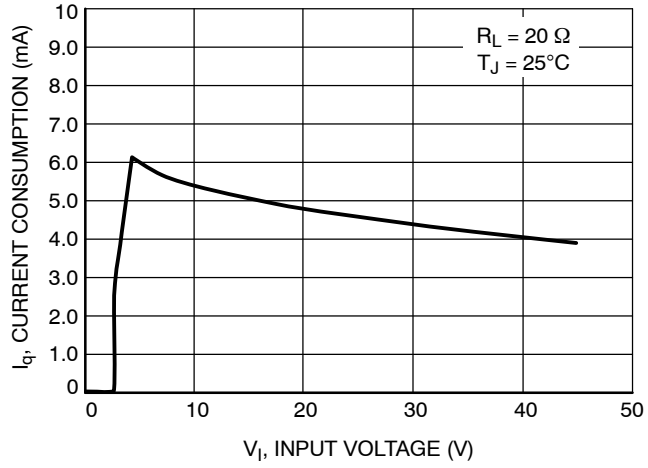



**Figure 31. Current Consumption $I_q$ vs. Input Voltage $V_I$, 3.3 V Version**

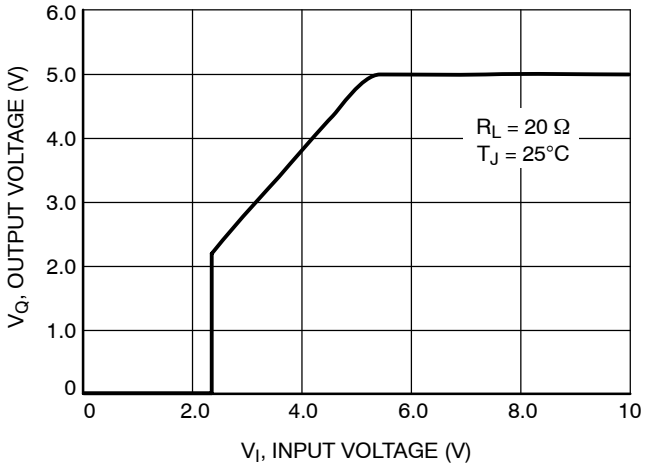



**Figure 33. Low Voltage Behavior, 5.0 V Version**

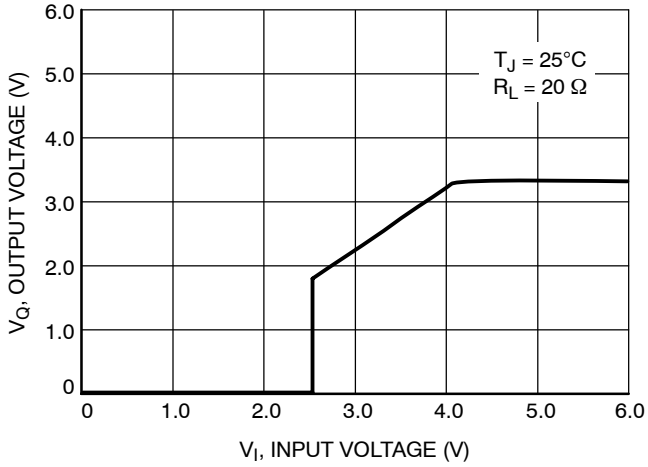



**Figure 32. Low Voltage Behavior, 3.3 V Version**

## TYPICAL PERFORMANCE CHARACTERISTICS – 4276A Version

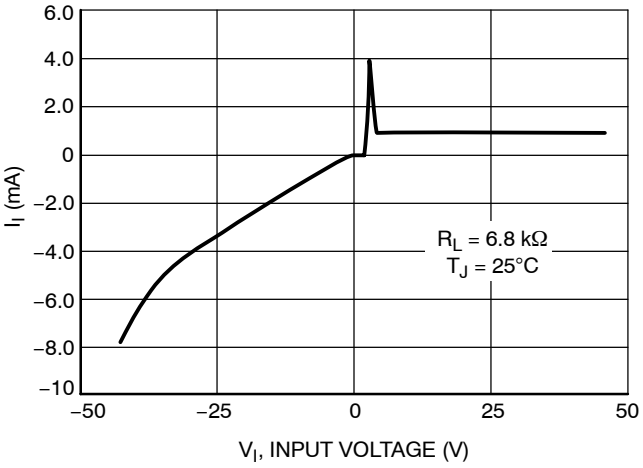



**Figure 34. Input Current vs. Input Voltage, 5.0 V Version**

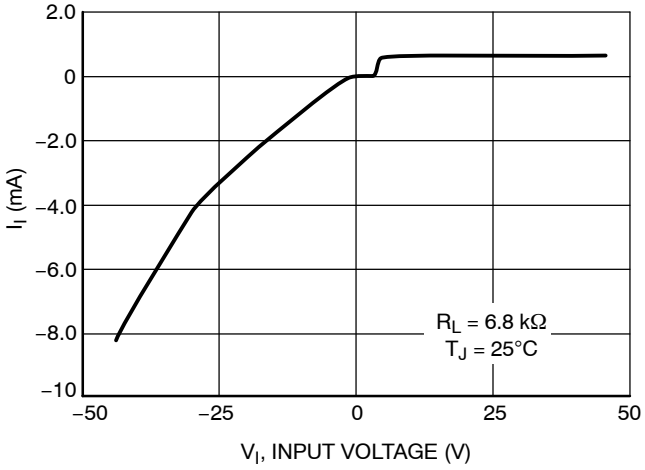



**Figure 35. Input Current $I_I$ vs. Input Voltage $V_I$, 3.3 V Version**

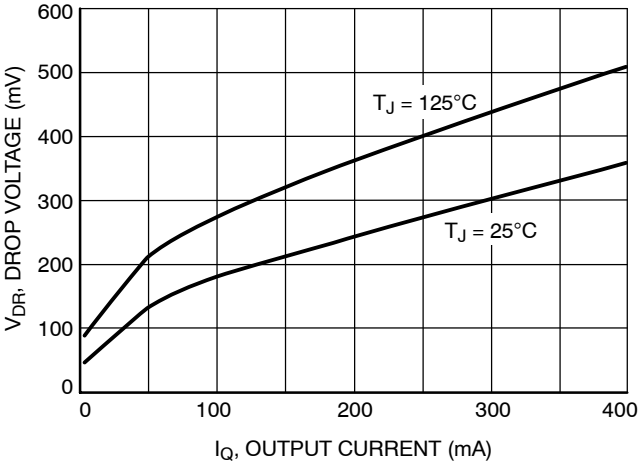



**Figure 36. Dropout Voltage $V_{DR}$ vs. Output Current $I_Q$**

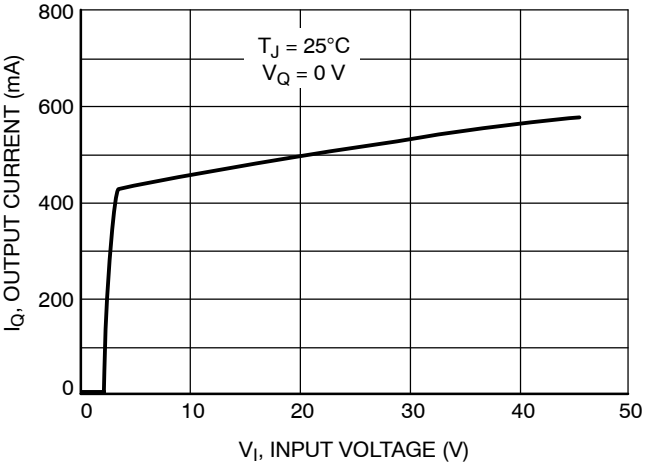



**Figure 37. Maximum Output Current $I_Q$ vs. Input Voltage $V_I$**

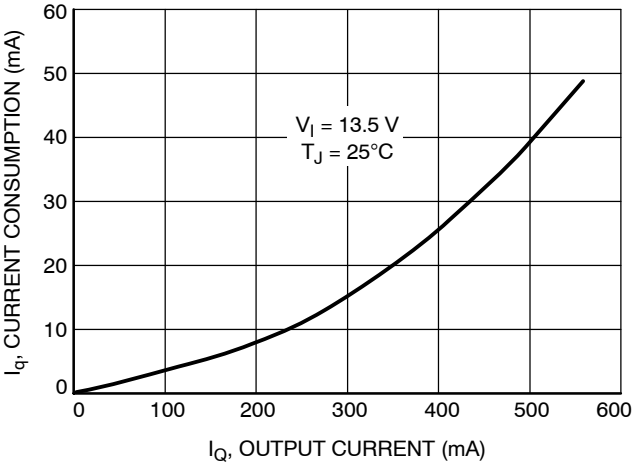



**Figure 38. Current Consumption $I_q$ vs. Output Current $I_Q$ (High Load)**

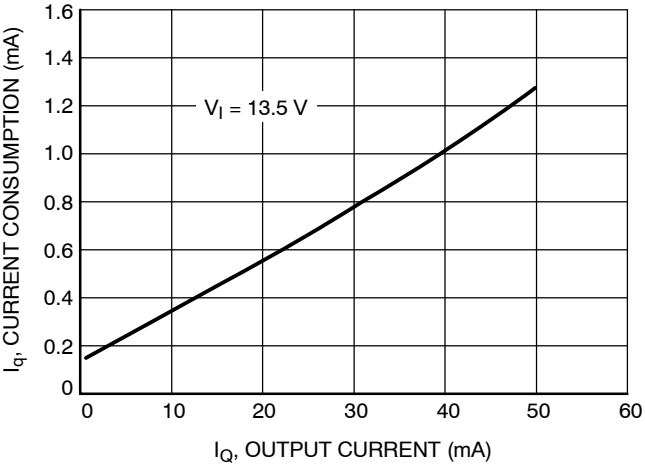



**Figure 39. Current Consumption $I_q$ vs. Output Current $I_Q$ (Low Load)**

## TYPICAL PERFORMANCE CHARACTERISTICS – Adjustable Version

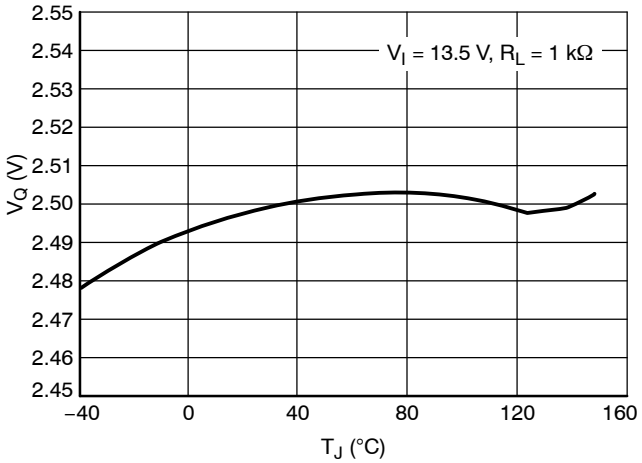



**Figure 40. Output Voltage $V_Q$ vs. Junction Temperature $T_J$, Adjustable Version**

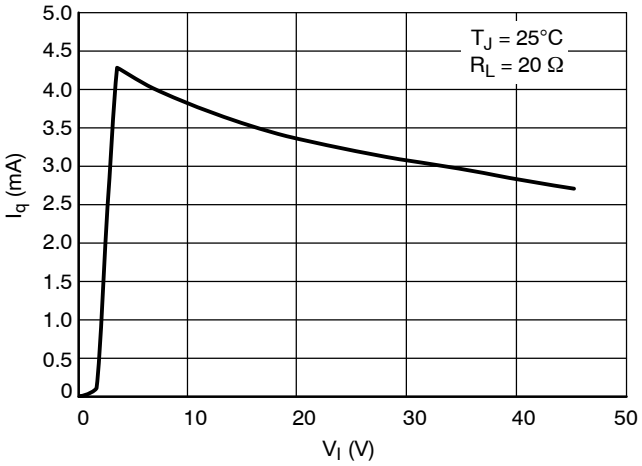



**Figure 41. Current Consumption $I_q$ vs. Input Voltage $V_I$, Adjustable Version**

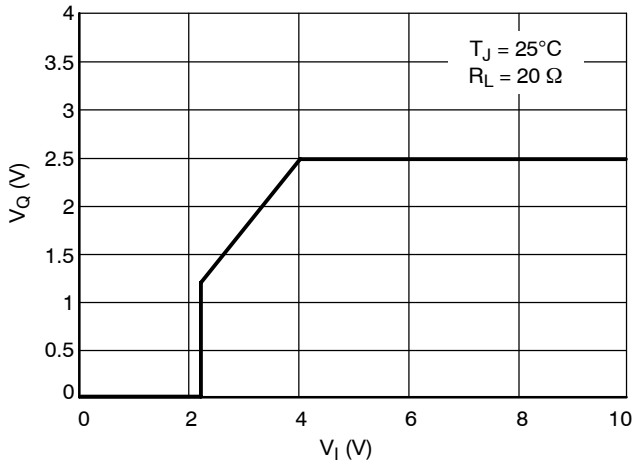



**Figure 42. Low Voltage Behavior, Adjustable Version**

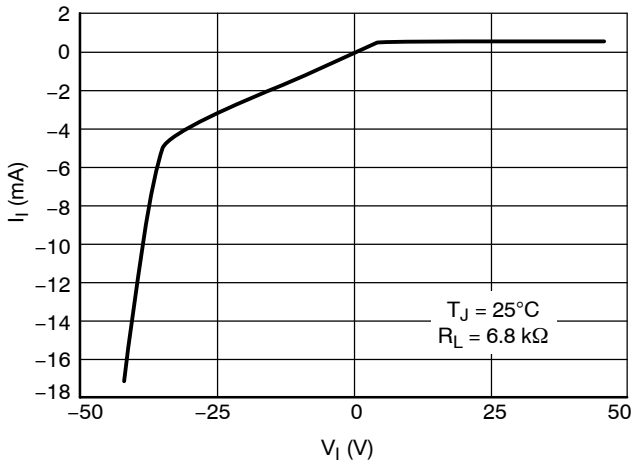



**Figure 43. High Voltage Behavior, Adjustable Version**

## TYPICAL PERFORMANCE CHARACTERISTICS – Adjustable Version

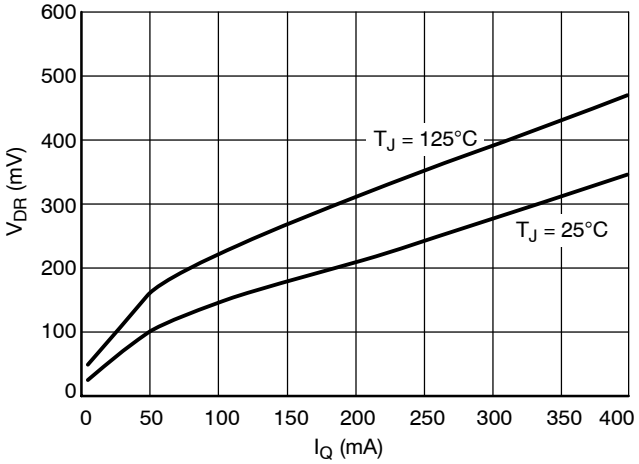



**Figure 44. Dropout Voltage $V_{DR}$ vs. Output Current $I_Q$, Regulator Set at 5.0 V, Adjustable Version**

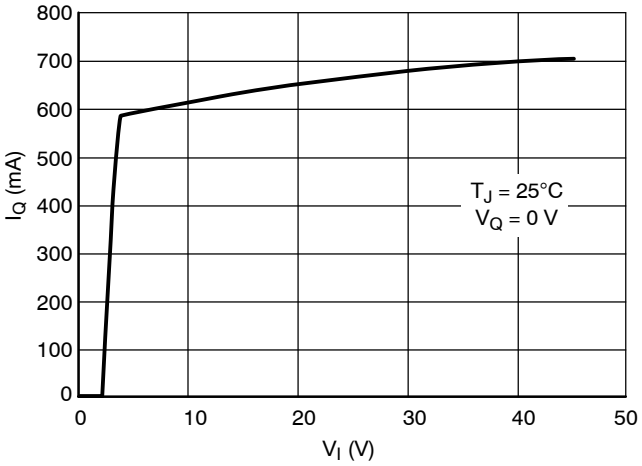



**Figure 45. Maximum Output Current $I_Q$ vs. Input Voltage $V_I$, Adjustable Version**

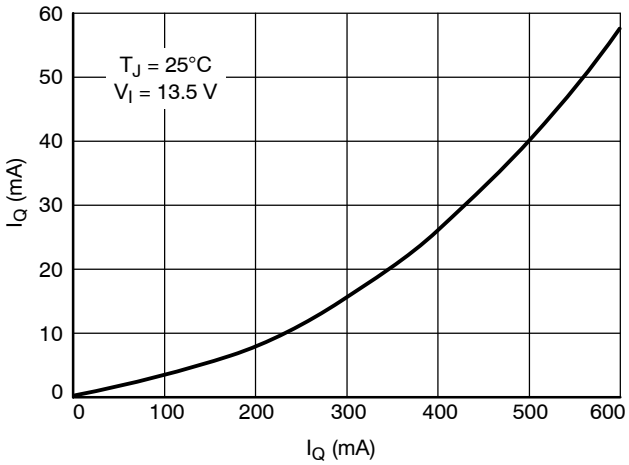



**Figure 46. Current Consumption $I_q$ vs. Output Current $I_Q$ (High Load), Adjustable Version**

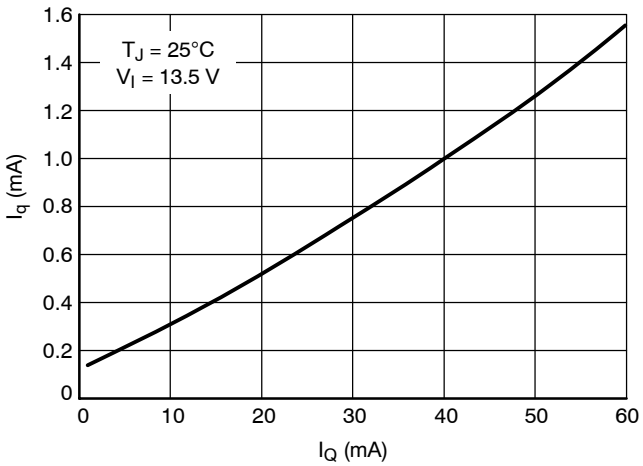



**Figure 47. Current Consumption $I_q$ vs. Output Current $I_Q$ (Low Load), Adjustable Version**

## Circuit Description

The NCV4276 is an integrated low dropout regulator that provides a regulated voltage at 400 mA to the output. It is enabled with an input to the inhibit pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 400 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

## Regulator

The error amplifier compares the reference voltage to a sample of the output voltage ($V_Q$) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. See Figure 5, Test Circuit, for circuit element nomenclature illustration.

## Regulator Stability Considerations

The input capacitors ($C_{I1}$ and $C_{I2}$) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with $C_{I2}$ can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor $C_Q$, shown in Figure 3, should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed for $C_Q \geq 22$ μF and an ESR $\leq 2.5$ Ω for the 5.0 V and Adjustable regulator and $C_Q \geq 10$ μF and an ESR $\leq 1.8$ Ω for the 1.8 V, 2.5 V, and 3.3 V regulators. See Figures 5 and 6 for output stability at various load and capacitive ESR conditions.

## Inhibit Input

The inhibit pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.5 V, the output of the regulator will be turned off. When the voltage on the Inhibit pin is greater than 3.5 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The inhibit pin may be connected directly to the input pin to give constant enable to the output regulator.

## Setting the Output Voltage (Adjustable Version)

The output voltage range of the adjustable version can be set between 2.5 V and 20 V (Figure ). This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin VA. The internal reference voltage is set to a temperature stable reference of 2.5 V.

The output voltage is calculated from the following formula. Ignoring the bias current into the VA pin:

$$V_Q = [(R1 + R2) * V_{ref}]/R2$$

Use R2 < 50 k to avoid significant voltage output errors due to VA bias current.

Connecting VA directly to Q without R1 and R2 creates an output voltage of 2.5 V.

Designers should consider the tolerance of R1 and R2 during the design phase.

The input voltage range for operation (pin 1) of the adjustable version is between ($V_Q$ + 0.5 V) and 40 V. Internal bias requirements dictate a minimum input voltage of 4.5 V. The dropout voltage for output voltages less than 4.0 V is (4.5 V − $V_Q$).

### Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 48) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad (1)$$

where

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application,
$I_q$ is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

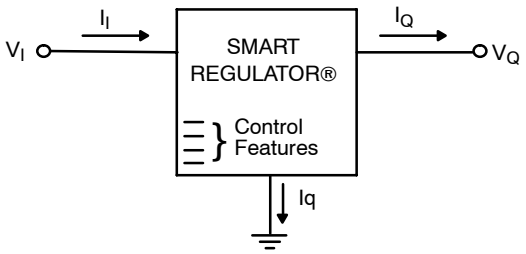



**Figure 48. Single Output Regulator with Key Performance Parameters Labeled**

### Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

## Thermal Model

A discussion of thermal modeling is in the ON Semiconductor web site: http://www.onsemi.com/pub/collateral/BR1487−D.PDF.

**Table 1. DPAK 5−Lead Thermal RC Network Models**

| **Drain Copper Area (1 oz thick)** | | | **168 mm²** | **736 mm²** | | **168 mm²** | **736 mm²** | |
|---|---|---|---|---|---|---|---|---|
| **(SPICE Deck Format)** | | | **Cauer Network** | | | **Foster Network** | | |
| | | | 168 mm² | 736 mm² | Units | Tau | Tau | Units |
| **C_C1** | **Junction** | **GND** | 1.00E−06 | 1.00E−06 | W−s/C | 1.36E−08 | 1.361E−08 | sec |
| **C_C2** | **node1** | **GND** | 1.00E−05 | 1.00E−05 | W−s/C | 7.41E−07 | 7.411E−07 | sec |
| **C_C3** | **node2** | **GND** | 6.00E−05 | 6.00E−05 | W−s/C | 1.04E−05 | 1.029E−05 | sec |
| **C_C4** | **node3** | **GND** | 1.00E−04 | 1.00E−04 | W−s/C | 3.91E−05 | 3.737E−05 | sec |
| **C_C5** | **node4** | **GND** | 4.36E−04 | 3.64E−04 | W−s/C | 1.80E−03 | 1.376E−03 | sec |
| C_C6 | node5 | GND | 6.77E−02 | 1.92E−02 | W−s/C | 3.77E−01 | 2.851E−02 | sec |
| C_C7 | node6 | GND | 1.51E−01 | 1.27E−01 | W−s/C | 3.79E+00 | 9.475E−01 | sec |
| C_C8 | node7 | GND | 4.80E−01 | 1.018 | W−s/C | 2.65E+01 | 1.173E+01 | sec |
| C_C9 | node8 | GND | 3.740 | 2.955 | W−s/C | 8.71E+01 | 8.59E+01 | sec |
| C_C10 | node9 | GND | 10.322 | 0.438 | W−s/C | | | sec |
| | | | 168 mm² | 736 mm² | | R's | R's | |
| **R_R1** | **Junction** | **node1** | 0.015 | 0.015 | C/W | 0.0123 | 0.0123 | C/W |
| **R_R2** | **node1** | **node2** | 0.08 | 0.08 | C/W | 0.0585 | 0.0585 | C/W |
| **R_R3** | **node2** | **node3** | 0.4 | 0.4 | C/W | 0.0304 | 0.0287 | C/W |
| **R_R4** | **node3** | **node4** | 0.2 | 0.2 | C/W | 0.3997 | 0.3772 | C/W |
| **R_R5** | **node4** | **node5** | 2.97519 | 2.6171 | C/W | 3.115 | 2.68 | C/W |
| R_R6 | node5 | node6 | 8.2971 | 1.6778 | C/W | 3.571 | 1.38 | C/W |
| R_R7 | node6 | node7 | 25.9805 | 7.4246 | C/W | 12.851 | 5.92 | C/W |
| R_R8 | node7 | node8 | 46.5192 | 14.9320 | C/W | 35.471 | 7.39 | C/W |
| R_R9 | node8 | node9 | 17.7808 | 19.2560 | C/W | 46.741 | 28.94 | C/W |
| R_R10 | node9 | GND | 0.1 | 0.1758 | C/W | | | C/W |

NOTE: Bold face items represent the package without the external thermal system.

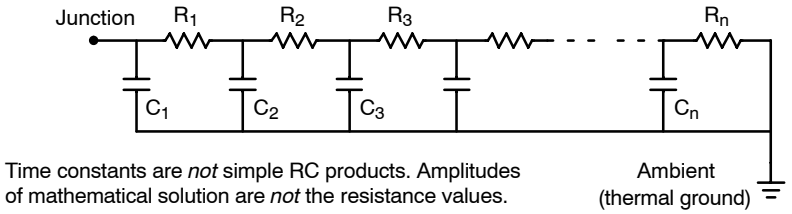



**Figure 49. Grounded Capacitor Thermal Network ("Cauer" Ladder)**

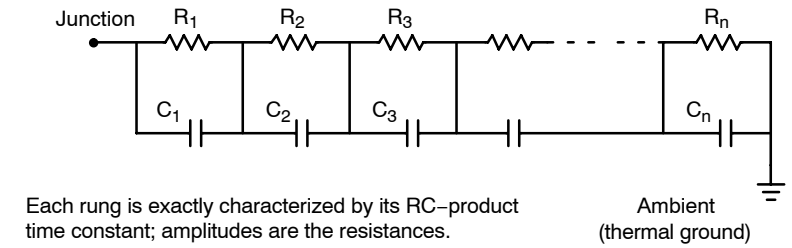



**Figure 50. Non−Grounded Capacitor Thermal Ladder ("Foster" Ladder)**

**Table 2. D²PAK 5−Lead Thermal RC Network Models**

| **Drain Copper Area (1 oz thick)** | | | **241 mm²** | **788 mm²** | | **241 mm²** | **788 mm²** | |
|---|---|---|---|---|---|---|---|---|
| **(SPICE Deck Format)** | | | **Cauer Network** | | | **Foster Network** | | |
| | | | 241 mm² | 653 mm² | Units | Tau | Tau | Units |
| **C_C1** | **Junction** | **GND** | 1.00E−06 | 1.00E−06 | W−s/C | 1.361E−08 | 1.361E−08 | sec |
| **C_C2** | **node1** | **GND** | 1.00E−05 | 1.00E−05 | W−s/C | 7.411E−07 | 7.411E−07 | sec |
| **C_C3** | **node2** | **GND** | 6.00E−05 | 6.00E−05 | W−s/C | 1.005E−05 | 1.007E−05 | sec |
| **C_C4** | **node3** | **GND** | 1.00E−04 | 1.00E−04 | W−s/C | 3.460E−05 | 3.480E−05 | sec |
| **C_C5** | **node4** | **GND** | 2.82E−04 | 2.87E−04 | W−s/C | 7.868E−04 | 8.107E−04 | sec |
| C_C6 | node5 | GND | 5.58E−03 | 5.95E−03 | W−s/C | 7.431E−03 | 7.830E−03 | sec |
| C_C7 | node6 | GND | 4.25E−01 | 4.61E−01 | W−s/C | 2.786E+00 | 2.012E+00 | sec |
| C_C8 | node7 | GND | 9.22E−01 | 2.05 | W−s/C | 2.014E+01 | 2.601E+01 | sec |
| C_C9 | node8 | GND | 1.73 | 4.88 | W−s/C | 1.134E+02 | 1.218E+02 | sec |
| C_C10 | node9 | GND | 7.12 | 1.31 | W−s/C | | | sec |
| | | | 241 mm² | 653 mm² | | R's | R's | |
| **R_R1** | **Junction** | **node1** | 0.015 | 0.0150 | C/W | 0.0123 | 0.0123 | C/W |
| **R_R2** | **node1** | **node2** | 0.08 | 0.0800 | C/W | 0.0585 | 0.0585 | C/W |
| **R_R3** | **node2** | **node3** | 0.4 | 0.4000 | C/W | 0.0257 | 0.0260 | C/W |
| **R_R4** | **node3** | **node4** | 0.2 | 0.2000 | C/W | 0.3413 | 0.3438 | C/W |
| **R_R5** | **node4** | **node5** | 1.85638 | 1.8839 | C/W | 1.77 | 1.81 | C/W |
| R_R6 | node5 | node6 | 1.23672 | 1.2272 | C/W | 1.54 | 1.52 | C/W |
| R_R7 | node6 | node7 | 9.81541 | 5.3383 | C/W | 4.13 | 3.46 | C/W |
| R_R8 | node7 | node8 | 33.1868 | 18.9591 | C/W | 6.27 | 5.03 | C/W |
| R_R9 | node8 | node9 | 27.0263 | 13.3369 | C/W | 60.80 | 29.30 | C/W |
| R_R10 | node9 | GND | 1.13944 | 0.1191 | C/W | | | C/W |

NOTE: Bold face items represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

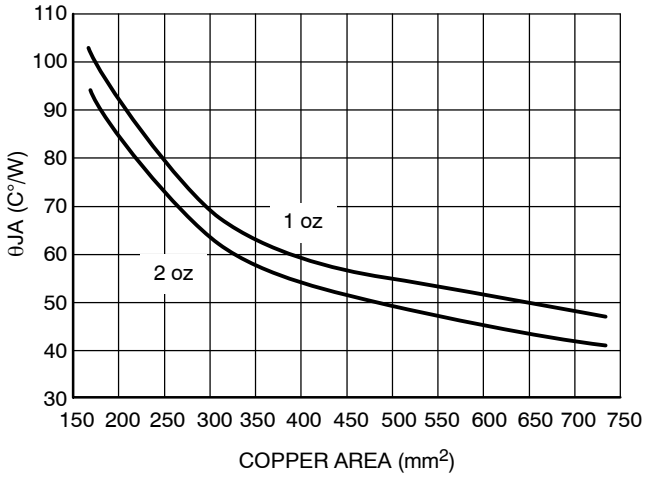



**Figure 51. θJA vs. Copper Spreader Area, DPAK 5−Lead**

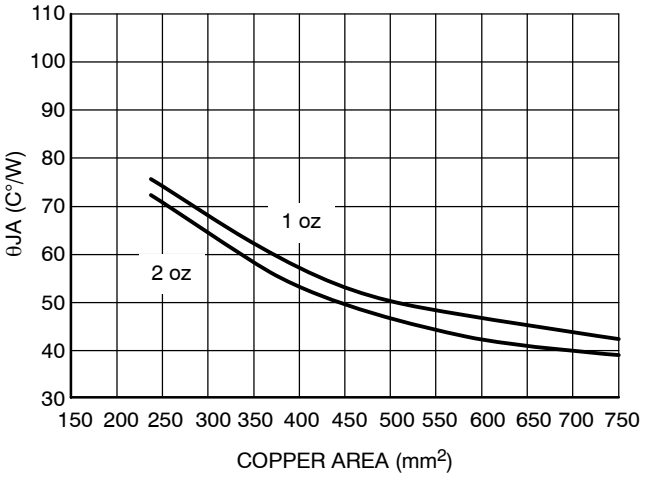



**Figure 52. θJA vs. Copper Spreader Area, D²PAK 5−Lead**

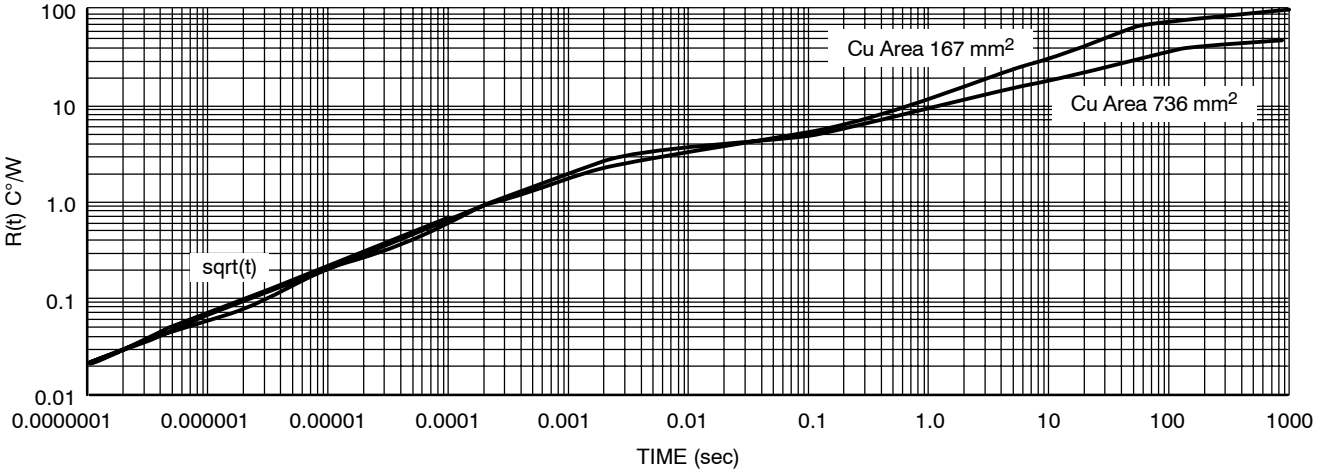



**Figure 53. Single−Pulse Heating Curves, DPAK 5−Lead**

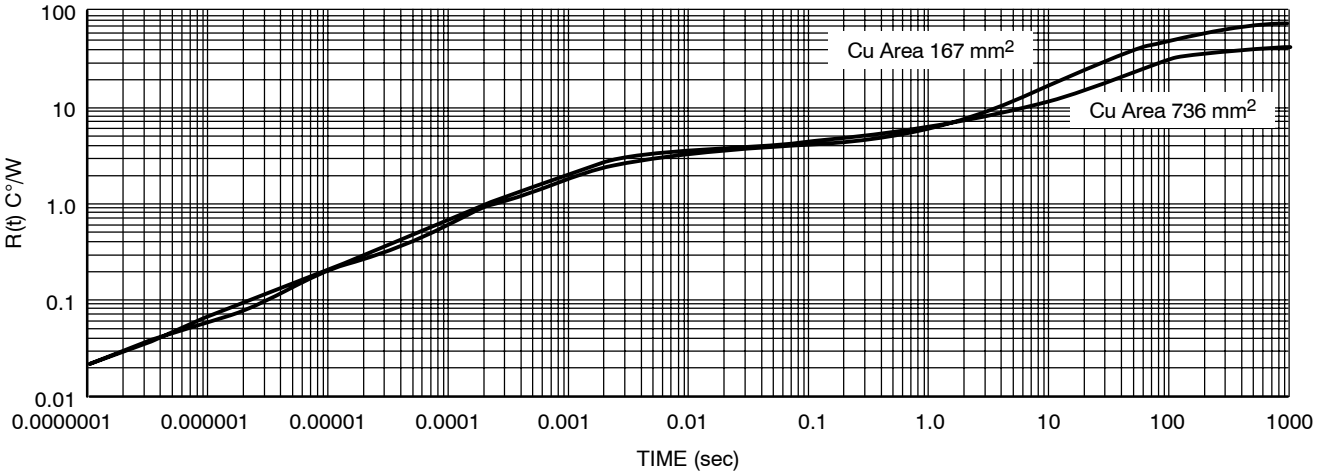



**Figure 54. Single−Pulse Heating Curves, D²PAK 5−Lead**

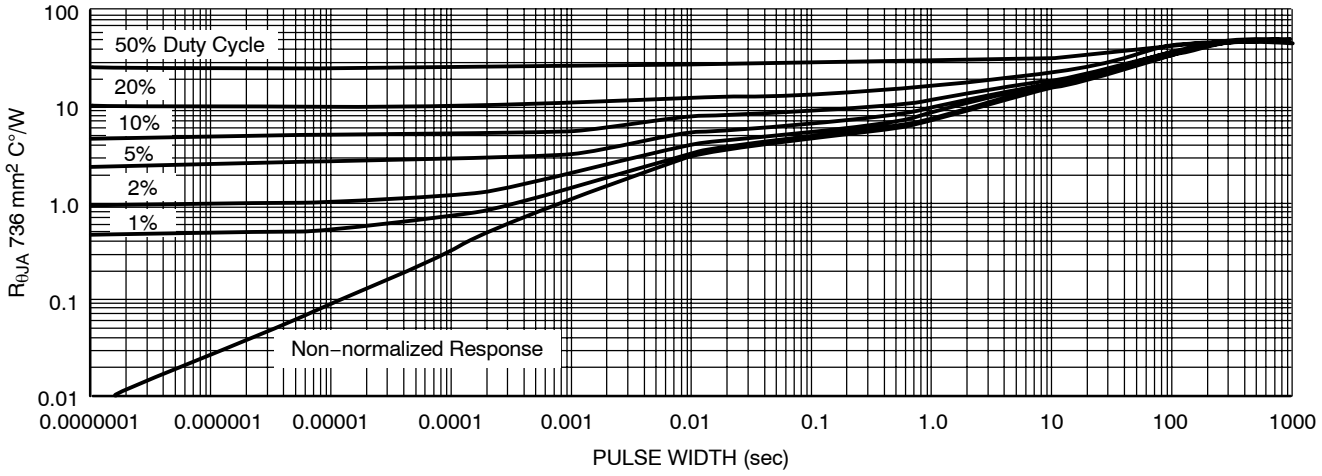



**Figure 55. Duty Cycle for 1″ Spreader Boards, DPAK 5−Lead**

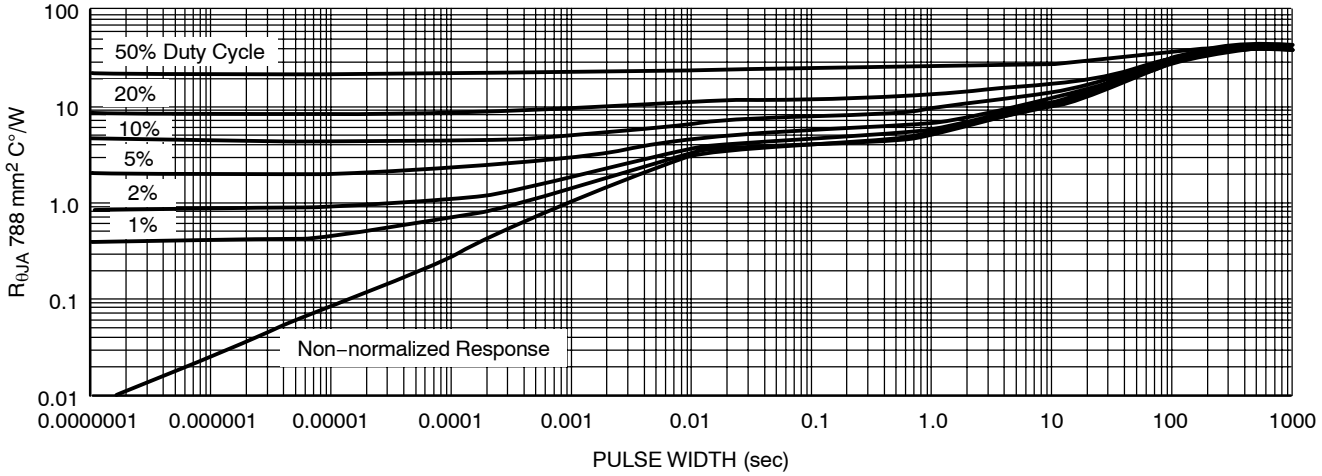
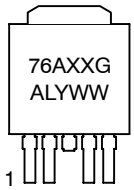


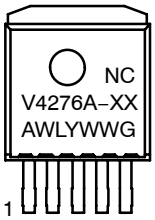

**Figure 56. Duty Cycle for 1″ Spreader Boards, D²PAK 5−Lead**

## MARKING DIAGRAMS



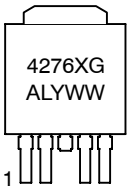

NCV4276A

**DPAK**
**5−PIN**
**DT SUFFIX**
**CASE 175AA**



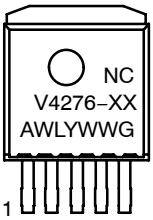

NCV4276A

**D²PAK**
**5−PIN**
**DS SUFFIX**
**CASE 936A**




NCV4276

**DPAK**
**5−PIN**
**DT SUFFIX**
**CASE 175AA**




NCV4276

**D²PAK**
**5−PIN**
**DS SUFFIX**
**CASE 936A**

*Tab is connected to Pin 3 on all packages.

| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Device |
| x, xx | = Voltage Ratings as indicated below |

A−Version

DPAK
XX = AJ (Adj. Voltage)
XX = 50 (5.0 V)

D²PAK
XX = AJ (Adj. Voltage)
XX = 50 (5.0 V)

Non−A−Version

DPAK
X = V (Adj. Voltage)
X = 5 (5.0 V)
X = 3 (3.3 V)

D²PAK
XX = AJ (Adj. Voltage)
XX = 50 (5.0 V)
XX = 33 (3.3 V)
XX = 25 (2.5 V)
XX = 18 (1.8 V)

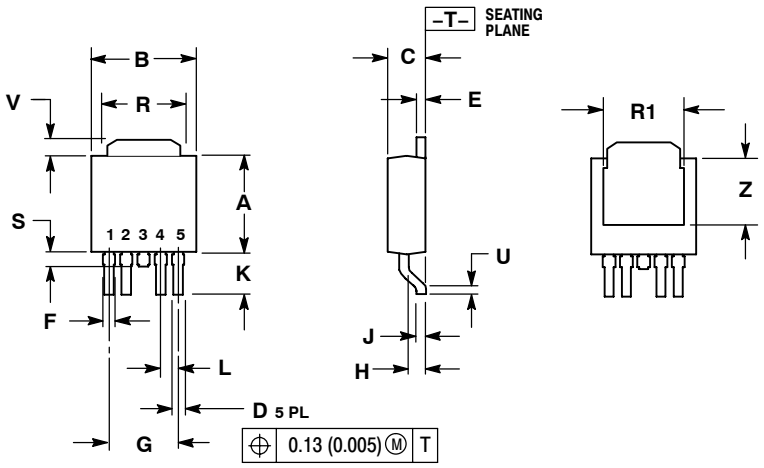
## ORDERING INFORMATION

| Device | Output Voltage Accuracy | Output Voltage | Package | Shipping† |
|---|---|---|---|---|
| NCV4276DT50RK | 4% | 5.0 V | DPAK, 5−Pin | 2500 / Tape & Reel |
| NCV4276DT50RKG | | | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |
| NCV4276DS50 | | | D$^2$PAK, 5−Pin | 50 Units / Rail |
| NCV4276DS50G | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276DS50R4 | | | D$^2$PAK, 5−Pin | 800 / Tape & Reel |
| NCV4276DS50R4G | | | D$^2$PAK, 5−Pin (Pb−Free) | 800 / Tape & Reel |
| NCV4276DT33RK | | 3.3 V | DPAK, 5−Pin | 2500 / Tape & Reel |
| NCV4276DT33RKG | | | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |
| NCV4276DS33 | | | D$^2$PAK, 5−Pin | 50 Units / Rail |
| NCV4276DS33G | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276DS33R4 | | | D$^2$PAK, 5−Pin | 800 / Tape & Reel |
| NCV4276DS33R4G | | | D$^2$PAK, 5−Pin (Pb−Free) | 800 / Tape & Reel |
| NCV4276DS25 | | 2.5 V | D$^2$PAK, 5−Pin | 50 Units / Rail |
| NCV4276DS25G | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276DS25R4 | | | D$^2$PAK, 5−Pin | 800 / Tape & Reel |
| NCV4276DS25R4G | | | D$^2$PAK, 5−Pin (Pb−Free) | 800 / Tape & Reel |
| NCV4276DS18 | | 1.8 V | D$^2$PAK, 5−Pin | 50 Units / Rail |
| NCV4276DS18G | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276DS18R4 | | | D$^2$PAK, 5−Pin | 800 / Tape & Reel |
| NCV4276DS18R4G | | | D$^2$PAK, 5−Pin (Pb−Free) | 800 / Tape & Reel |
| NCV4276DTADJRKG | | Adjustable | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |
| NCV4276DSADJG | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276DSADJR4G | | | | 800 / Tape & Reel |
| NCV4276ADT33RKG | 2% | 3.3 V | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |
| NCV4276ADT50RKG | | 5.0 V | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |
| NCV4276ADS50G | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276ADS50R4G | | | | 800 / Tape & Reel |
| NCV4276ADTADJRKG | | Adjustable | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |
| NCV4276ADSADJG | | | D$^2$PAK, 5−Pin (Pb−Free) | 50 Units / Rail |
| NCV4276ADSADJR4G | | | | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

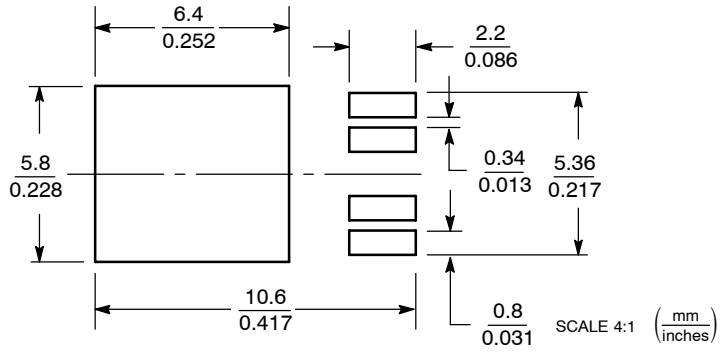
**DPAK 5, CENTER LEAD CROP**
**DT SUFFIX**
CASE 175AA−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.020 | 0.028 | 0.51 | 0.71 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.024 | 0.032 | 0.61 | 0.81 |
| G | 0.180 BSC | | 4.56 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.045 BSC | | 1.14 BSC | |
| R | 0.170 | 0.190 | 4.32 | 4.83 |
| R1 | 0.185 | 0.210 | 4.70 | 5.33 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | −−− | 0.51 | −−− |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | 0.170 | 3.93 | 4.32 |

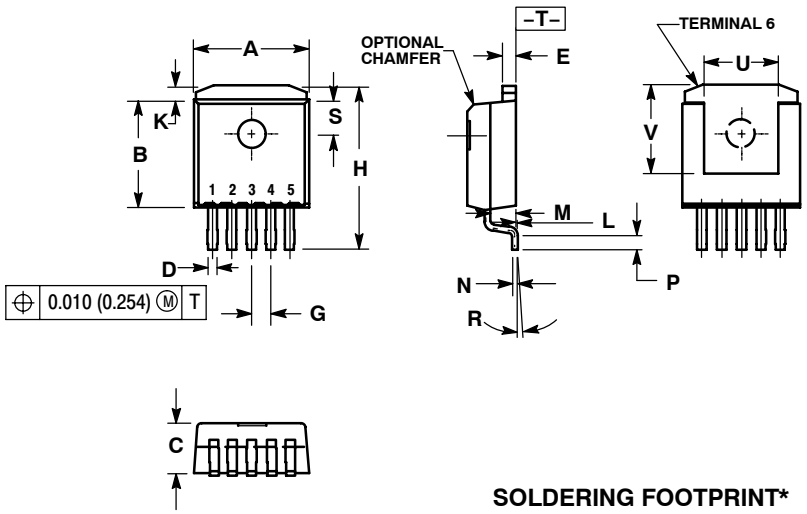
**SOLDERING FOOTPRINT***




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

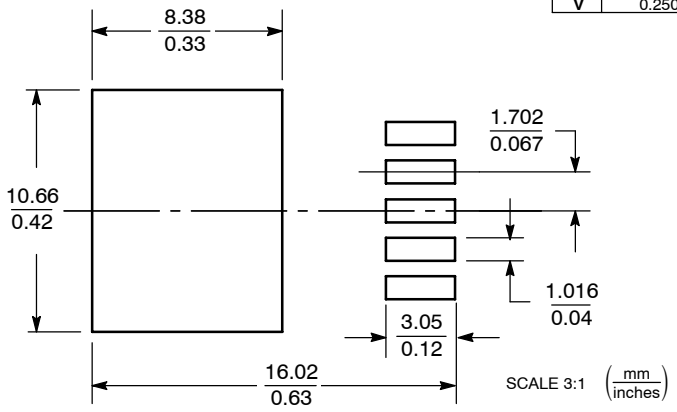
**D²PAK**
**5 LEAD**
**DS SUFFIX**
CASE 936A−02
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 5° REF | | 5° REF | |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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