T-52-33-03

GS62C102
MEMORY/ADDRESS CONTROLLER

1. FEATURES

- Address buffer and latch circuits.
- The I/O address decoder circuit.
- 10 separate hardware or software configurable memory configurations for a flexible memory system design.
- LIM 4.0 EMS controller circuit register circuit.
- DRAM page mode controller circuit.
- Gold mode memory controller circuit. (non-page mode RAM).
- 8237 memory address refresh counter circuit.
- Early RAS and CAS signal generation.
- DMA page mapper circuit.
- 8237 DMA controller (X2).
- Low power CMOS VLSI implementation.
- 160 pins QFP package.

2. DESCRIPTION

Memory Subsystem

The SUNTAC GS62CS102 chip supports both a conventional 0 wait state memory subsystem and a 4-bank 4-way page interleaved memory subsystem. It supports up to 8MB of on-board memory with combinations of 256Kbit and 1Mbit DRAMs. For example, one bank of 1Mbit DRAM plus two banks of 256Kbit DRAM can be used to provide a total of 3MB memory for running the DOS compatible function of OS/2. Special design is incorporated in the memory controller to allow a 10 to 15 percent enhancement in DRAM efficiency. Hidden refresh and minimized precharge time are several features which enhances the memory performance. The processor can run at 20Mhz and 16Mhz with 0.3 wait state using 100ns and 120ns, respectively. In addition, GS62C102 can be configured to run at 16 MHz using conventional DRAM mode. The page mode performance can be further enhanced by using fast page mode DRAMs. The page-interleave feature of the memory subsystem takes the advantages of both the page mode RAM and memory bank interleave. The fast page mode RAM allows for fast 0WS on page accesses during high speed CPU operation. The four page interleaved banks acts as four separate segments of one page size. This feature ideally matches the four segment process model of the

www.DataSheet4U.com

Intel IAPX® architecture for enhanced performance for both protected and real mode.

MEMORY CONTROL

GS62C102 converts the address to MA for local memory for both EMS enabled and EMS disabled. In addition, this chip provides the bank select, RAS and CAS signals to control the DRAM. When the ROM is being accessed, the MXA is also used with the MA to address the content of the ROM.

Several delay lines are connected with DLIN as output and DL15, DL30 and DL45 as input. These signals provide the necessary signals to generate the memory control signals.

ADDRESS CONTROL

GS62C102 provides the address buffering from CPU to MA, LA, SA and XA in CPU cycle, and SA to XA, MA in MASTER cycle. In DMA cycle, the address is generated from internal DMA controller. The bus master accesses are not mapped by the EMS circuit.

Shadow RAM/EMS/Extended Memory

The LIM EMS version 4.0 is fully supported by the EMS registers built into the chip set. Either 640KB or 512KB can be used as the base memory and the remaining DRAMs can be used as extended memory, EMS memory, BIOS shadow RAM or video shadow RAM. For example, when 1MB memory is available with 640KB base memory, 64KB can be used as BIOS shadow RAM and video shadow RAM. The remaining 320 KByte can be configured as conventional extended memory or 20 pages of EMS memory, or as 96 KBytes extended memory plus 14 pages of EMS memory. Each individual EMS page can be disabled or enabled by writing to the configuration registers. GS62CS0102 chip supports EMS without any speed penalty.

The SUNTAC GS62CS102 chip supports both 8- and 16-bit PROM. The 8-bit mode operation not only reduces the board space but also reduces cost and inventory. With the optional BIOS shadow RAM enabled, the 8-bit mode operation is faster than the 16-bit mode operation (without shadow RAM). The chip set also supports single ROM for both system and video BIOS. This further reduces the board space and component cost for all-in-one motherboard designs.

Features of the GS62C102 include:

- Optional shadow RAM for system and video BIOS ROM.
- Fully support EMS 4.0 with 64 EMS registers.
- Two shadow RAM map: window size programmable.
- Two alternate sets of 6 EMS registers. The 6 registers are grouped into 4 contiguous 16KB blocks (total 64K, EMS-3.2) and 2 contiguous 16KB blocks (total 32K, EMS-4.0).
- Extended memory is left over while the space between BASE 0FFFFF is not programed as EMS or SHADOW RAM.

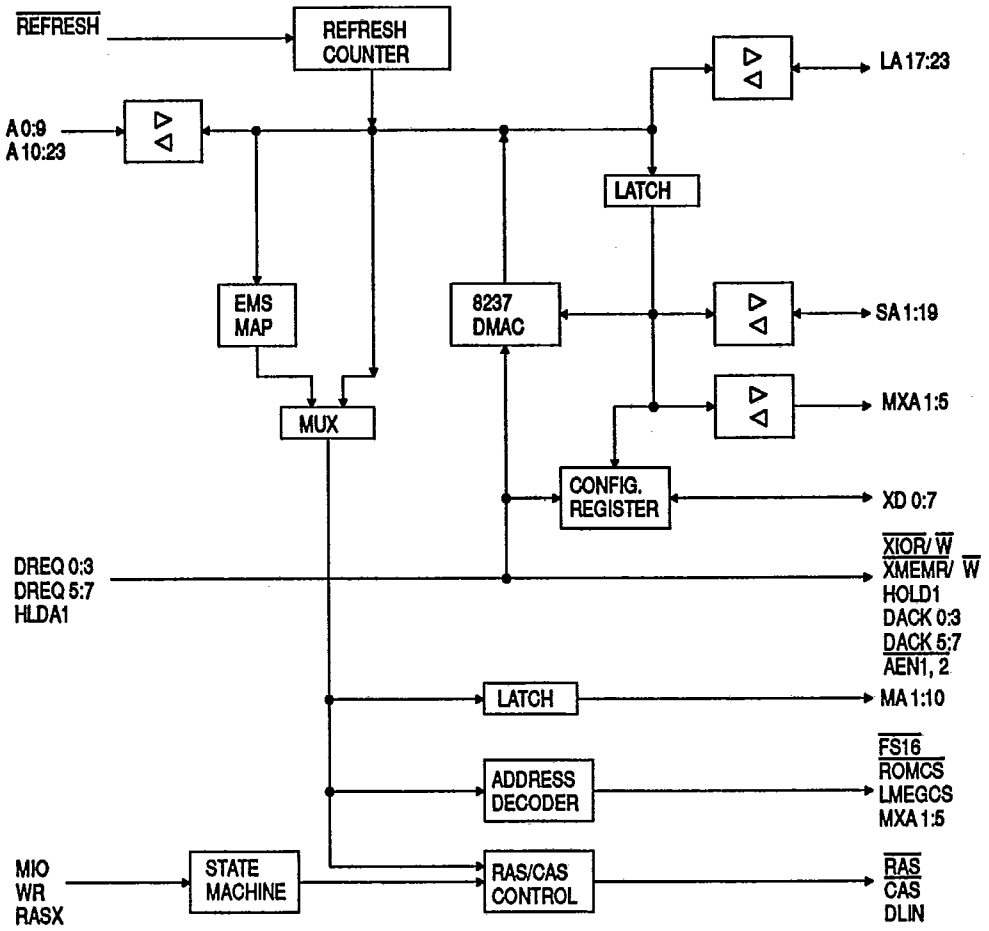
CONFIGURATION REGISTER

The default configuration index port I/O address is defined at 98H after power up. One can program the configuration registers by first writing the correct index register number to the I/O address 98H (Index Address Register) and then, the new data for the index register to the I/O address 99H (Index Data Register).

In case of the I/O address conflict with some other I/O devices, one can program the Index Address Register and the Index Data Register by writting to the new location to the Index register location 00H. In addition, to the above software programmable configuration, the initial power on setup can be read in using the DIP switches. These DIP switch setting is documented in a table at the end of this section.

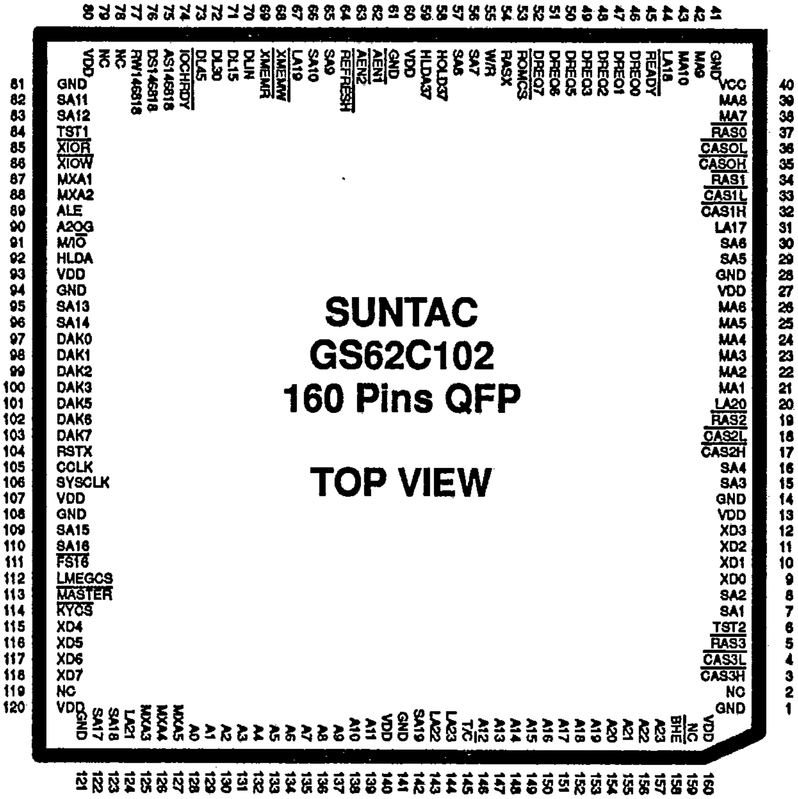
T-52-33-03

GS62C102 FUNCTIONAL BLOCK DIAGRAM



T-52-33-03

GS62C102 PIN DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Number	Type	Description
CPU Interface			
M/$\overline{IO}$	91	I	Memory/IO status from the CPU.
W/R	55	I	W/R status pin from the CPU.
$\overline{BHE}$	158	I/O	CPU byte-high-enable pin, CD8-CD15 to be valid. This pin is logical complement of the A0 pin.
A0:9	128-137	I	CPU address line A0 to A9.
A10:23	138-139 146-157	I	CPU address line A10 to A23.
$\overline{READY}$	45	I/O	Connects to CPU's "READY" pin. READY signal to CPU when cycle other than local memory access is done. This pin serves as output during local memory cycle. For all other cycles, this pin serves as an input pin.
HLDA	92	I	Connects to CPU's "HOLDA" pin. Hold acknowledge from CPU. This pin indicates that AT Bus has been acquired by another bus master.
GS62C101 Interface			
RASX	54	I	The synchronized version of address strobe.
RSTX	104	I	Reset pin from GS62C101. Resets the G62C102 from either power on or keyboard.

Pin Name	Pin Number	Type	Description
CCLK	105	I	CPU clock input from the clock generator on board of the GS62C101. This pin is also connected to the clock input of the CPU. During the Low Power and Sleep Mode, this clock frequency is reduced or stopped.
SYSCLK	106	I	System clock from the GS62C101 is used for the 8237 DMA controller. It is derived by dividing the AT clock by two. This pin is used to generate the DMA clock.
$\overline{FS16}$	111	O	Asserted when local memory is accessed. Active low indicates a 16 bits local memory access.
ALE	89	I	Address-latch-enable from the GS62C101 indicating valid address on SA bus.
LMEGCS	112	O	Low mega memory operation. This pin indicates a memory access under 1MB.
MXA1:5	87-88, 125-127	I/O	X address bus to on-board peripheral and ROM. Also used to address configuration registers. These pins are also used to read in default dip switch setting during power on.
XD0:7	9-12, 115-118	I/O	X data bus. These pins carry the data needed for programming the DMA and the configuration registers. These pins are also used to read in default dip switch setting during power on.
$\overline{XIOR}$	85	I/O	XIO read command. This command is active when one wants to read from an I/O device on the X bus.
$\overline{XIOW}$	86	I/O	XIO write command. This command is active when a write is performed on an X bus I/O device.
$\overline{XMEMR}$	69	I/O	Memory read command that indicates a local memory read operation.

Pin Name	Pin Number	Type	Description
$\overline{\text{XMEMW}}$	68	I/O	Memory write command that indicates a local memory write operation.
HOLD37	58	O	Hold request generated by the internal DMA controller (8237).
HLDA37	59	I	Hold acknowledge from the hold circuit on GS62C101 indicating that the CPU has been put on hold, and the DMA controller has the control of the bus.
$\overline{\text{AEN1,2}}$	62-63	O	AEN1 and AEN2 from the built-in DMA controller. The signal indicates either a 16-bits or 8-bits DMA accesses.
$\overline{\text{REFRESH}}$	64	I	Refresh cycle. Generate by the refresh timer or external master to commence refresh operation.
MEMORY Interface			
$\overline{\text{ROMCS}}$	53	O	ROM chip select. This pin indicates a ROM access cycle to the GS62C101. This pin also enable the ROM.
MA1:10	21-26, 38-39, 42-43	O	Memory address bus. These pins are connected to the address input of the DRAM and ROM chips.
DLIN	70	O	Delay line input. These lines are used to generate address strobe to local memory.
DL15	71	I	Delay line 1st input indicating a delay signal is generated by delaying the DLIN signal 15 ns.
DL30	72	I	Delay line 2nd input indicating a delay signal is generated by delaying the DLIN signal 30 ns.
DL45	73	I	Delay line 3rd input indicating a delay signal is generated by delaying the DLIN signal 45 ns.

Pin Name	Pin Number	Type	Description
RAS0:3	5, 19, 34, 37	O	Row address control for the 4 banks of memory.
CAS0:3L	4, 18, 33, 36	O	Column address control for low bytes.
CAS0:3H	3, 17, 32, 35	O	Column address control for high bytes.
BUS Interface			
SA1:19	7-8, 15-16, 29-30, 56-57, 65-66, 82-83, 95-96, 109-110, 122-123, 142	I/O	System address line from the A1 to A19. These signals are latched by ALE signal.
LA17:23	31, 44, 67, 20, 124, 143-144	I/O	System LA bus. These lines are not latched, and they come directly from the CPU address bus.
MASTER	113	I	MASTER cycle. Indicates a bus master has taken control of the ISA Bus. This signal comes from the ISA Bus slots.
DREQ0:3	46-49	I	DMA request inputs from the ISA Bus.
DREQ5:7	50-52	I	DMA request inputs from the ISA Bus.
DAK0:3	97-100	O	DMA acknowledge outputs to the devices on the ISA Bus requesting a DMA transfer.

Pin Name	Pin Number	Type	Description
DAK5:7	101-103	O	DMA acknowledge outputs to the devices on the ISA Bus requesting a DMA transfer.
T/C	145	O	Terminal count from DMA controller. This pin is used to indicate the count of byte being transferred.
$\overline{\text{IOCHRDY}}$	74	I	IO channel ready. This signal is used by a slow device on the ISA Bus that requires an access time longer than the 4 wait state normally allocated for the I/O transfers.
SYSTEM Interface			
AS146818	75	I/O	146818 AS. Real Time Clock interface. This pin is connected to the 146818's AS pin which function as address strobe for reading the time and the configuration information. This pin is also used to read in default dip switch setting during power on.
DS146818	76	I/O	146818 DS. RTC interface. This pin is connected to the 146818's DS pin which functions as the data strobe for setting time and writing configuration. This pin is also used to read in the default dip switch setting during power on.
RW146818	77	O	146818 R/W. RTC interface. This pin connects to the R/W pin of the 146818, indicating the read or write command to the RAM.
$\overline{\text{KYCS}}$	114	I/O	Key board controller (8742) chip select. This pin is also used to read in the default dip switch setting during power on.
A20G	90	I	A20GATE signal from keyboard controller. This signal cause a fast reset that allows one to switch from protected mode to real mode. It is an optimization for the OS 2.
TST1 TST2	84 6	I	Enable test mode for GS62C102. Always pull high.

CONFIGURATION DESCRIPTION

MEMORY CONFIGURATION

Table I: Memory configuration

- 4 banks up to 8M byte.

Mode	DRAM type				Total memory
	0	1	3	4	
1	256K				512K
2	256K	256K			1M
3	1M				2M
4	256K	1M			2.5M
5	256K	256K	256K	256K	2M
6	256K	256K	1M		3M
7	1M	1M			4M
8	256K	256K	1M	1M	5M
9	1M	1M	1M		6M
10	1M	1M	1M	1M	8M

Table II: DRAM WAIT STATE

Mode	Wait state			Corresponding DRAM (Mhz/ns)
NON-PAGE	0			16/60
(GOLD MODE)	0.5			16/60
	1			16/80
	1.5			16/100
PAGE MODE	START	ON	OFF	
REG-PAGE:	2	0	3	16/120, 20/100, 25/80
FAST-PAGE:	1.5	0	2.5	16/100, 20/80, 25/60
SUPER-PAGE:	1	0	2	16/80, 25/60
Each read after write cycle will have 1 wait state. ROM: 1 or 3 wait state.				

Table 3: System Configuration Register

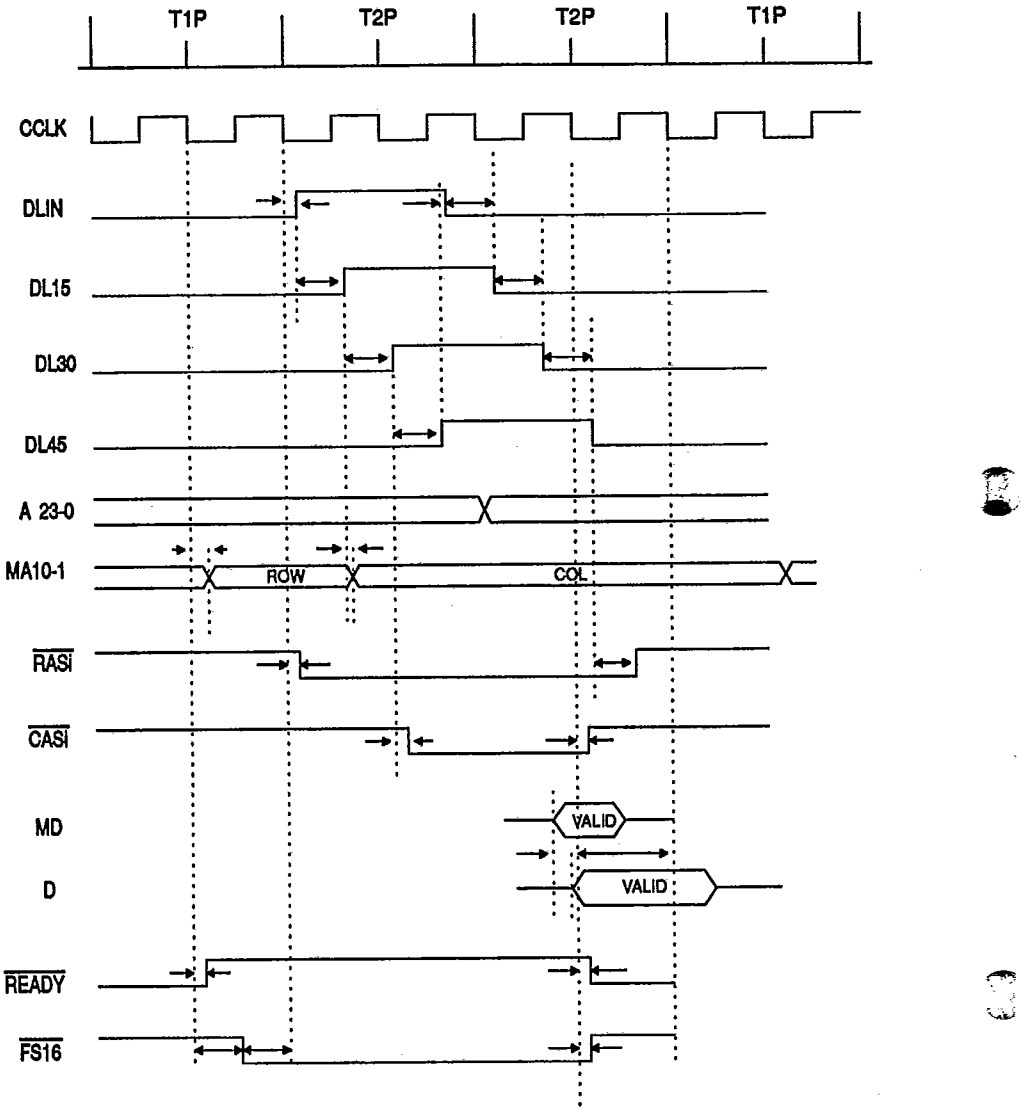
Index Register #0	
This register contains the I/O address of the index address register and the index data register. The default I/O address for index address register is 98H, and the default index data register is 99H. (See below for the index registers configuration)	
Index Register #30	
bit 0	Reserved. Always pull low.
bit 1	0=8-bits ROM 1=16-bits ROM
bit 2	AT Bus clock select: 0=ATCLK, 1=CLK2/2
bit 3	Rom Accesses Wait State: 0=3WS, 1=1WS
bit 4	0=Page Interleave Mode, 1=Gold Mode
bit 5	0=Fast Page Mode, 1=Normal Page Mode
bit 6	Gold Mode Wait State: 0=0WS, 1=1WS
bit 7	Enable Setup ROM: 0=disabled(use FFFFF0), 1=enabled(remap to setup ROM)
Index Register #31	
bit 0,1,2,3	Memory Bank Configuration (see TABLE 1)
bit 4,5	00=disable EMS, disable shadow RAM. 01=enable shadow RAM only. 10=enable EMS and shadow RAM. 11=reserved.
Index Register #32	
bit 0	RAS time out: 0=disable 1=enable
Index Register #33	
bit 0	Video BIOS relocate to allow for single ROM for all BIOS: 0=disable, 1=enable
Index Register #38:	
bit 0	base memory ceiliing: 0=640K, 1=512K
bit 1	enable EMS alternate set (0=A 1=B)

Table 3: System Configuration Register Continued

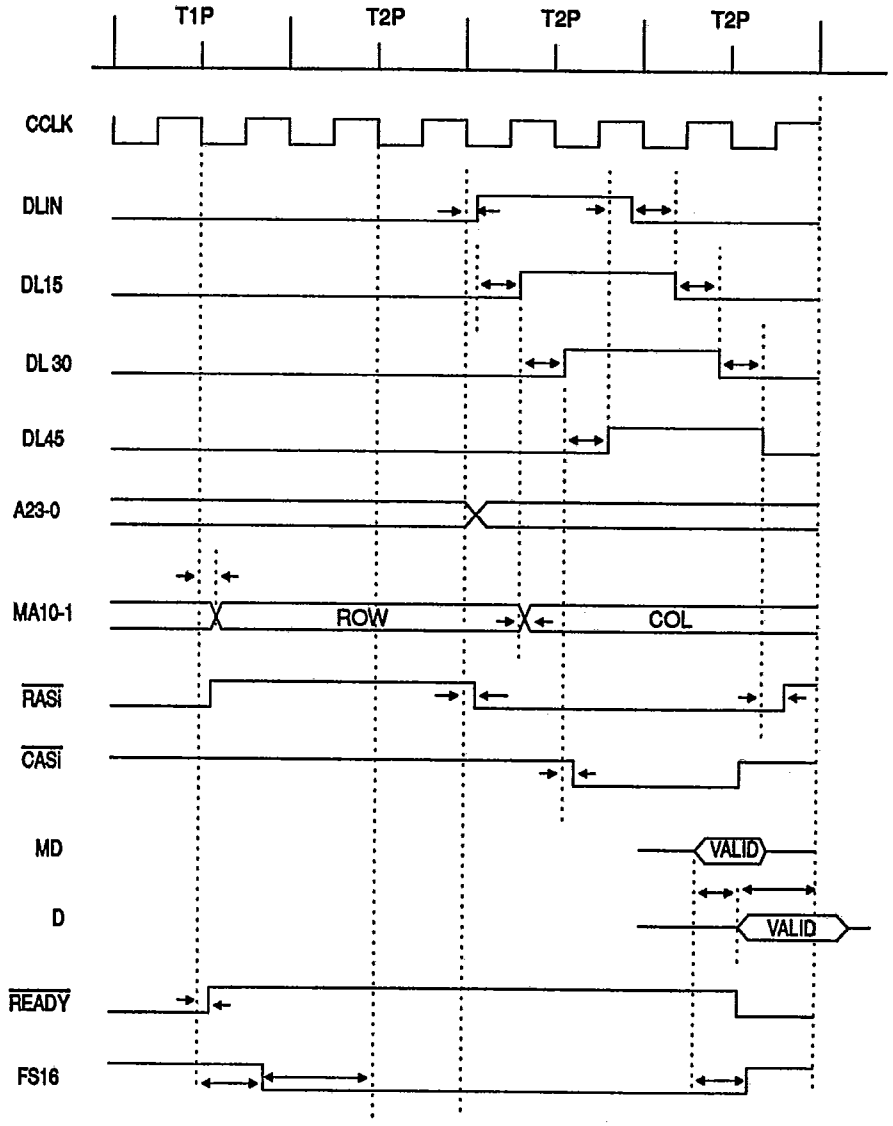
Index Register #39: extended memory ceiling	
bit 0	memory address bit 23
bit 1	memory address bit 22
bit 2	memory address bit 21
bit 3	memory address bit 20
bit 4	memory address bit 19
bit 5	memory address bit 18
Index Register #3A	
bit 0	read enable the shadow RAM
Index Register #3B	
bit 0	write enable the shadow RAM
Index Register #3C-3F:	
Enable/disable bit pattern for individual EMS pages. Each bit corresponds to each of the currently enabled 32 EMS registers.	
Index Register #40-7F:	
EMS Look up table content each of the 64 index registers contains the 9 bits address mapping information.	

MEMORY CYCLE TIMING DIAGRAM

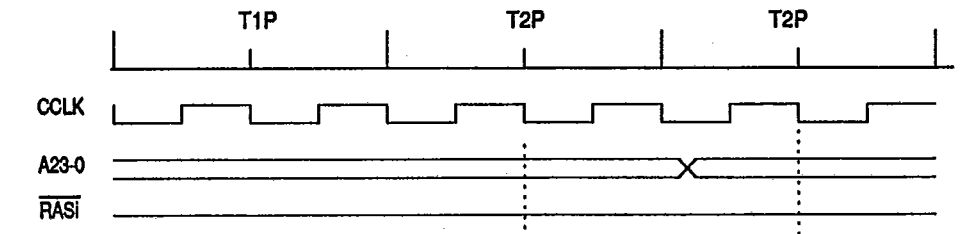
I. Start Cycle of the Page Mode Operation



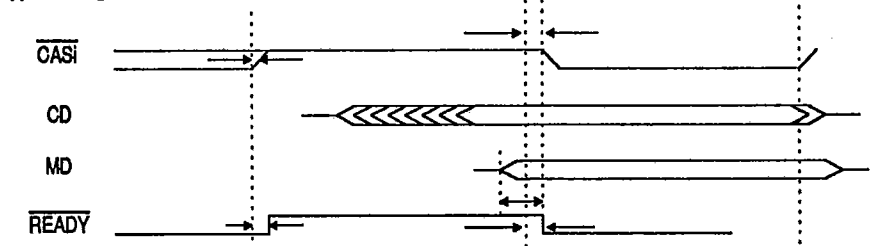
II. Off Page Access Cycle



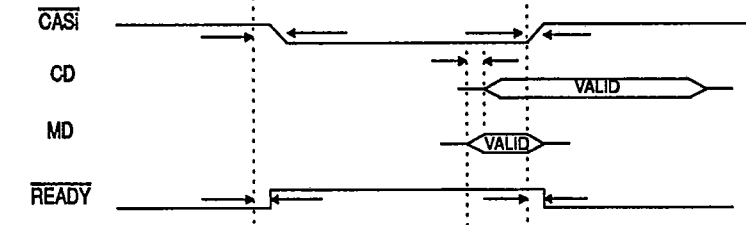
III. On Page Accesses



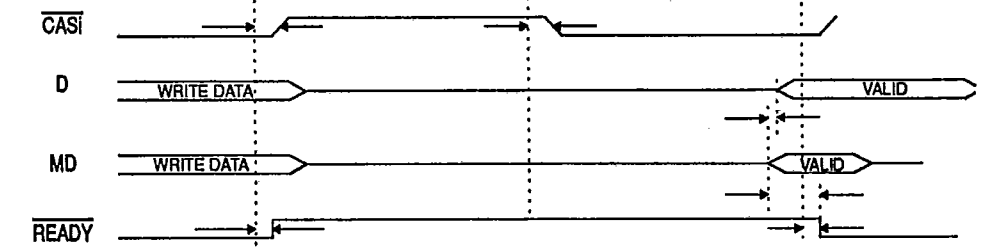
(I) On Page Write



(II) On Page Read



(III) On Page, Same Bank, Read after Write (Normal Page Mode) - One Wait State



IV. Gold Mode© 1 Wait State Access