19-2010; Rev 0; 4/01

MAXIM

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

General Description

The MAX1813 step-down controller is intended for core CPU DC-DC converters in notebook computers. The controller features a dynamically adjustable output (5-bit DAC), ultra-fast transient response, high DC accuracy, and high efficiency necessary for leading-edge CPU core power supplies. Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The MAX1813 is designed specifically for CPU core applications requiring a voltage-positioned supply. The voltage-positioning input (VPCS), combined with a high-DC-accuracy control loop, is used to implement a power supply that modifies its output set point in response to the load current. This arrangement decreases full-load power dissipation and reduces the required number of output capacitors.

The output voltage can be dynamically adjusted through the 5-bit digital-to-analog converter (DAC) inputs over a 0.600V to 2V range. The MAX1813 includes an internal multiplexer that selects between three different DAC code settings. The first two inputs are controlled by five digital input pins (D0–D4). The third input is used for the suspend mode and controlled by two 4-level input pins (S0, S1). Output voltage transitions are accomplished with a proprietary precision slew-rate control that minimizes surge currents to and from the battery while guaranteeing "just-in-time" arrival at the new DAC setting.

The MAX1813's 28V input range enables single-stage buck conversion from high-voltage batteries for the maximum possible efficiency. Alternatively, the controller's high-frequency capability combined with two-stage conversion (stepping down the +5V system supply instead of the battery) allows the smallest possible physical size.

The MAX1813 is available in a 28-pin QSOP package.

Applications

Notebook Computers

(Intel IMVP–II™/Coppermine™)

Docking Stations

CPU Core Supply

Single-Stage (BATT to V_{CORE}) Converters

Two-Stage (+5V to V_{CORE}) Converters

Typical Operating Circuit appears at end of data sheet.

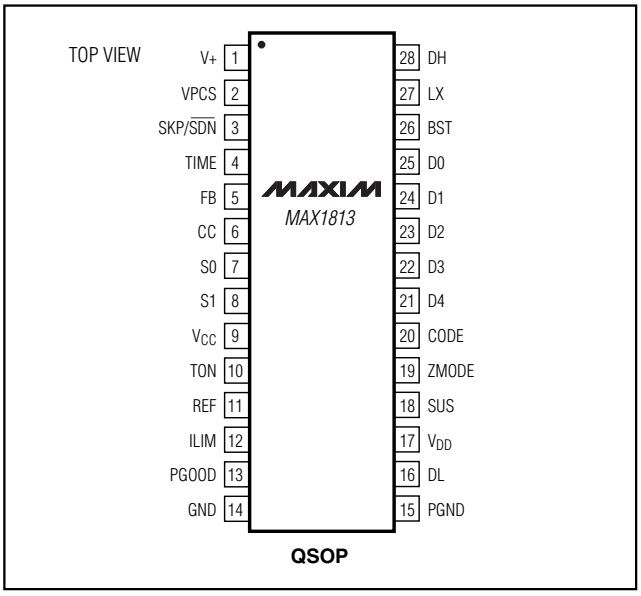
Features

- ♦ **High-Efficiency Voltage Positioning**
- ♦ **Quick-PWM Architecture**
- ♦ **±1% V_{OUT} Accuracy Over Line**
- ♦ **Adjustable Output Slew Rate**
- ♦ **0.600V to 2V Adjustable Output Range (5-Bit DAC)**
- ♦ **2V to 28V Battery Input Range**
- ♦ **200/300/600/1000kHz Switching Frequency**
- ♦ **Output Undervoltage and Overvoltage Protection**
- ♦ **Drives Large Synchronous-Rectifier MOSFETs**
- ♦ **±20% Accurate Current-Limit**
- ♦ **10µA Shutdown Supply Current**
- ♦ **2V ±1% Reference Output**
- ♦ **Power-Good (PGOOD) Indicator**
- ♦ **Small 28-Pin QSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1813EEI	-40°C to +85°C	28 QSOP

Pin Configuration



Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Coppermine and IMVP-II are trademarks of Intel Corp.

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
V_{CC}, V_{DD} to GND .....-0.3V to +6V
PGND to GND.....±0.3V
D0–D4, CODE, ZMODE, SUS, PGOOD to GND .....-0.3V to +6V
SKP/$\overline{SDN}$ to GND (Note 1) .....-0.3V to +16V
ILIM, FB, CC, REF,
TON, TIME, S0, S1 to GND.....-0.3V to (V_{CC} + 0.3V)
VPCS to GND .....-2V to +30V
DL to PGND.....-0.3V to (V_{DD} + 0.3V)
BST to PGND.....-0.3V to +36V
DH to LX.....-0.3V to (V_{BST} + 0.3V)
LX to BST.....-6V to +0.3V
REF Short Circuit to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C).....860mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: SKP/$\overline{SDN}$ may be forced to 12V, temporarily exceeding the absolute maximum rating, for the purpose of debugging prototype breadboards, using the no-fault test mode.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery voltage, V+		2		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy (Notes 2, 3)		V+ = 4.5V to 28V, VPCS = GND, DAC codes from 0.925V to 2.0V		-1		+1	%
		V+ = 4.5V to 28V, VPCS = GND, DAC codes from 0.700V to 0.900V		-1.5		+1.5	
		V+ = 4.5V to 28V, VPCS = GND, DAC codes from 0.600V to 0.675V		-1.83		+1.83	
VPCS Input Bias Current	I_{VPS}	V_{VPCS} = 0 or 28V		-1		+1	µA
VPCS Transconductance	G_m	V_{VPCS} = 0 to -100mV		18	20	22	µS
VPCS Linear Input Range					±100		mV
FB Input Resistance	R_{FB}			115	180	265	kΩ
TIME Frequency Accuracy		38kHz nominal, R_{TIME} = 470kΩ		-12		+12	%
		150kHz nominal, R_{TIME} = 120kΩ		-8		+8	
		380kHz nominal, R_{TIME} = 47kΩ		-12		+12	
ILIM Input Leakage Current	I_{ILIM}	V_{ILIM} = 0 or 5.0V			0.01	100	nA
On-Time (Note 4)	t_{ON}	V+ = 5.0V, V_{FB} = 1.2V	TON = GND	250	270	290	ns
		V+ = 12V, V_{FB} = 1.2V	TON = REF	165	190	215	
			TON = open	320	355	390	
			TON = V_{CC}	465	515	563	
Minimum Off-Time (Note 4)	$t_{OFF(MIN)}$	TON = REF, open, or V_{CC}			400	500	ns
		TON = GND			300	375	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point			1.4	2.5	mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			<1	5	µA
Quiescent Supply Current (V+)	I+	Measured at V+			25	40	µA
Shutdown Supply Current (V_{CC})		SKP/$\overline{SDN}$ = GND			2	5	µA
Shutdown Supply Current (V_{DD})		SKP/$\overline{SDN}$ = GND			<1	5	µA
Shutdown Supply Current (V+)		SKP/$\overline{SDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, -40µA ≤ I_{REF} ≤ +40µA		1.98	2	2.02	V
REF Fault Lockout Voltage		Falling edge, 1% hysteresis		1.5	1.6	1.7	V
FAULT PROTECTION							
Output Overvoltage Fault Preset Threshold	V_{OVP}	Measured at FB	CODE = GND	2.20	2.25	2.30	V
			CODE = V_{CC}	1.95	2.00	2.05	
Output Overvoltage Fault Propagation Delay	t_{OVP}	FB forced to 2% above trip threshold			1.5		µs
Output Undervoltage Fault Threshold		With respect to unloaded output voltage		60	70	80	%
Output Undervoltage Fault Propagation Delay		FB forced to 2% below trip threshold			10		µs
Output Undervoltage Fault-Blanking Time		From SKP/$\overline{SDN}$ signal going high, clock speed set by R_{TIME}			256		clks
Current-Limit Threshold (Positive, Default)	V_{ITH}	V_{GND} - V_{VPCS}, ILIM = V_{CC}		40	50	60	mV
Current-Limit Threshold (Positive, Adjustable)	V_{ITH}	V_{GND} - V_{VPCS}	V_{ILIM} = 0.5V	40	50	60	mV
			V_{ILIM} = 2V (REF)	143	200	265	
Negative Current-Limit Threshold		V_{GND} - V_{VPCS}, with respect to V_{ITH}, ILIM = V_{CC}		-72	-56	-40	mV
Zero-Crossing Current-Limit Threshold		V_{GND} - V_{VPCS}			5		mV
Thermal Shutdown Threshold		Rising temperature, hysteresis = 15°C			160		°C
V_{CC} Undervoltage Lockout Threshold		Rising edge, hysteresis = 20mV, switching disabled below this level		4.05		4.45	V
PGOOD Lower Trip Threshold		Measured at FB with respect to unloaded output voltage, falling edge		-15	-12.5	-10.5	%
PGOOD Upper Trip Threshold		Measured at FB with respect to unloaded output voltage, rising edge		8	10	12	%
PGOOD Propagation Delay		Falling edge, FB forced 2% below or above PGOOD trip threshold			1.5		µs
PGOOD Output Low Voltage		I_{SINK} = 1mA				0.4	V
PGOOD Leakage Current		High state, forced to 5.5V				1	µA

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH Gate Driver On-Resistance	$R_{ON(DH)}$	V_{BST} - V_{LX} forced to 5V			1.2	3.5	Ω
DL Gate Driver On-Resistance	$R_{ON(DL)}$	High state (pull up)			1.3	3.5	Ω
		Low state (pull down)			0.4	1.0	
DH Gate Driver Source/Sink Current	I_{DH}	DH forced to 2.5V, V_{BST} - V_{LX} forced to 5V			2.0		A
DL Gate Driver Sink Current	I_{DL}	DL forced to 5V			4.0		A
DL Gate Driver Source Current	I_{DL}	DL forced to 2.5V			1.3		A
Dead Time		DL rising			35		ns
		DH rising			26		
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	D0–D4, CODE, SUS, ZMODE; V_{CC} = 4.5V to 5.5V		2.4			V
Logic Input Low Voltage	V_{IL}	D0–D4, CODE, SUS, ZMODE; V_{CC} = 4.5V to 5.5V				0.8	V
DAC Z-Mode Programming Resistor, Low		D0–D4, 0 to 0.4V or 2.6V to 5.5V applied to the resistor, ZMODE = CODE = GND or ZMODE = CODE = V_{CC}				1.05	kΩ
DAC Z-Mode Programming Resistor, High		D0–D4, 0 to 0.4V or 2.6V to 5.5V applied to the resistor, ZMODE = CODE = GND or ZMODE = CODE = V_{CC}		95			kΩ
D0–D4, CODE Pull Up/Down		Entering impedance mode	Pull up		40		kΩ
			Pull down		8		
Logic Input Current		D0–D4, CODE = V_{CC}		-1		+1	µA
		SUS, ZMODE = GND or V_{CC}		-1		+1	
4-Level Logic Input High (V_{CC})		TON (200kHz operation), S0, S1		V_{CC} - 0.4			V
4-Level Logic Input Upper-Middle (Float)		TON (300kHz operation), S0, S1		2.8		3.85	V
4-Level Logic Input Lower-Middle (REF)		TON (600kHz operation), S0, S1		1.65		2.35	V
4-Level Logic Low (GND)		TON (1000kHz operation), S0, S1				0.5	V
SKP/$\overline{SDN}$ High Input Level (Skip Mode)				2.8		6.0	V
SKP/$\overline{SDN}$ Float Input Level (Forced-PWM Mode)				1.4		2.2	V
SKP/$\overline{SDN}$ Low Input Level (Shutdown Mode)						0.5	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SKP/$\overline{SDN}$ NO FAULT Input Level			12		15	V
SKP/$\overline{SDN}$, 4-Level Logic Input Current		SKP/$\overline{SDN}$, TON, S0, S1 = GND or V_{CC}	-3		3	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range		Battery voltage, V+		2	28	V
		V_{CC}, V_{DD}		4.5	5.5	
DC Output Voltage Accuracy (Notes 2, 3)		V+ = 4.5V to 28V, VPCS = GND, DAC codes from 0.925V to 2.0V		-1	+1	%
		V+ = 4.5V to 28V, VPCS = GND, DAC codes from 0.700V to 0.900V		-1.5	+1.5	
		V+ = 4.5V to 28V, VPCS = GND, DAC codes from 0.600V to 0.675V		-1.83	+1.83	
VPCS Input Bias Current	I_{VPS}	V_{VPCS} = 0 or 28V		-1	+1	µA
VPCS Transconductance	G_m	V_{VPS} = 0 to -40mV		18	22	µS
		V_{VPS} = 0 to -100mV		16.5	22	
FB Input Resistance	R_{FB}			115	265	kΩ
TIME Frequency Accuracy		380kHz nominal, R_{TIME} = 47kΩ		-12	+12	%
		150kHz nominal, R_{TIME} = 120kΩ		-8	+8	
		38kHz nominal, R_{TIME} = 470kΩ		-12	+12	
ILIM Input Leakage Current	I_{ILIM}	V_{ILIM} = 0 or 5.0V			100	nA
On-Time (Note 4)	t_{ON}	V+ = 5.0V, V_{FB} = 1.2V	TON = GND	250	290	ns
		V+ = 12V, V_{FB} = 1.2V	TON = REF	165	215	
			TON = open	320	390	
			TON = V_{CC}	465	563	
Minimum Off-Time (Note 4)	$t_{OFF(MIN)}$	TON = REF, open, or V_{CC}			500	ns
		TON = GND			375	
BIAS AND REFERENCE						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point			2.5	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			5	µA
Quiescent Supply Current (V+)	I+	Measured at V+			40	µA
Shutdown Supply Current (V_{CC})		SKP/$\overline{SDN}$ = GND			5	µA
Shutdown Supply Current (V_{DD})		SKP/$\overline{SDN}$ = GND			5	µA

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Shutdown Supply Current (V+)		SKP/$\overline{SDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V			5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, -40µA ≤ I_{REF} ≤ +40µA		1.98	2.02	V
REF Fault Lockout Voltage		Falling edge, 1% hysteresis		1.5	1.7	V
FAULT PROTECTION						
Output Overvoltage Fault Preset Threshold	V_{OVP}	Measured at FB	CODE = GND	2.20	2.30	V
			CODE = V_{CC}	1.95	2.05	
Output Undervoltage Fault Threshhold		With respect to unloaded output voltage		60	80	%
Current-Limit Threshold (Positive, Default)	V_{ITH}	V_{GND} - V_{VPCS}, ILIM = V_{CC}		40	60	mV
Current-Limit Threshold (Positive, Adjustable)	V_{ITH}	V_{GND} - V_{VPCS}	V_{ILIM} = 0.5V	40	60	mV
			V_{ILIM} = 2V (REF)	143	265	
Negative Current-Limit Threshold		V_{GND} - V_{VPCS}, with respect to V_{ITH}, ILIM = V_{CC}		-75	-35	mV
V_{CC} Undervoltage Lockout Threshold		Rising edge, hysteresis = 20mV, switching disabled below this level		4.05	4.45	V
PGOOD Lower Trip Threshold		Measured at FB with respect to unloaded output voltage, falling edge		-15	-10.5	%
PGOOD Upper Trip Threshold		Measured at FB with respect to unloaded output voltage, rising edge		8	12	%
PGOOD Output Low Voltage		I_{SINK} = 1mA			0.4	V
PGOOD Leakage Current		High state, forced to 5.5V			1	µA
GATE DRIVERS						
DH Gate Driver On-Resistance	$R_{ON(DH)}$	V_{BST} - V_{LX} forced to 5V			3.5	Ω
DL Gate Driver On-Resistance	$R_{ON(DL)}$	High state (pull up)			3.5	Ω
		Low state (pull down)			1.0	
LOGIC AND I/O						
Logic Input High Voltage	V_{IH}	D0–D4, CODE, SUS, ZMODE; V_{CC} = 4.5V to 5.5V		2.4		V
Logic Input Low Voltage	V_{IL}	D0–D4, CODE, SUS, ZMODE; V_{CC} = 4.5V to 5.5V			0.8	V
DAC Z-Mode Programming Resistor, Low		D0–D4, 0 to 0.4V or 2.6V to 5.5V applied to the resistor, ZMODE = CODE = GND or ZMODE = CODE = V_{CC}			1.05	kΩ
DAC Z-Mode Programming Resistor, High		D0–D4, 0 to 0.4V or 2.6V to 5.5V applied to the resistor, ZMODE = CODE = GND or ZMODE = CODE = V_{CC}		95		kΩ
Logic Input Current		D0–D4, CODE = V_{CC}		-1	+1	µA
		SUS, ZMODE = GND or V_{CC}		-1	+1	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, VPCS = ZMODE = GND = PGND, SKP/$\overline{SDN}$ = CODE = V_{CC}, V_{OUT} set to 1.5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
4-Level Logic Input High (V_{CC})		TON (200kHz operation), S0, S1	V_{CC} - 0.4		V
4-Level Logic Input Upper-Middle (Float)		TON (300kHz operation), S0, S1	2.8	3.85	V
4-Level Logic Input Lower-Middle (REF)		TON (600kHz operation), S0, S1	1.65	2.35	V
4-Level Logic Low (GND)		TON (1000kHz operation), S0, S1		0.5	V
SKP/$\overline{SDN}$ High Input Level (Skip Mode)			2.8	6.0	V
SKP/$\overline{SDN}$ Float Input Level (Forced-PWM Mode)			1.4	2.2	V
SKP/$\overline{SDN}$ Low Input Level (Shutdown Mode)				0.5	V
SKP/$\overline{SDN}$ NO FAULT Input Level			12	15	V
SKP/$\overline{SDN}$, 4-Level Logic Input Current		SKP/$\overline{SDN}$, TON, S0, S1 = GND or V_{CC}	-3	+3	µA

Note 2: Output voltage accuracy specifications apply to DAC voltages from 0.6V to 2.0V.

Note 3: When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple. In discontinuous conduction (SKP/$\overline{SDN}$ = V_{CC}, light load), the output voltage will have a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

Note 4: On-time and off-time specifications are measured from 50% to 50% at the DH pin, with LX forced to 0, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

Note 5: Specifications to -40°C are guaranteed by design, not production tested.

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

Typical Operating Characteristics

(Circuit from Figure 1, components from Table 2, T_A = +25°C, unless otherwise noted.)

EFFICIENCY CURVE LEGEND

SKIP MODE ($\overline{SKIP}$ = GND)

A1: V+ = 4.5V

B1: V+ = 7V

C1: V+ = 15V

D1: V+ = 24V

PWM MODE ($\overline{SKIP}$ = V_{CC})

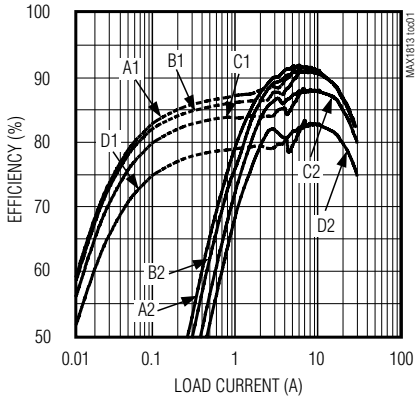
A2: V+ = 4.5V

B2: V+ = 7V

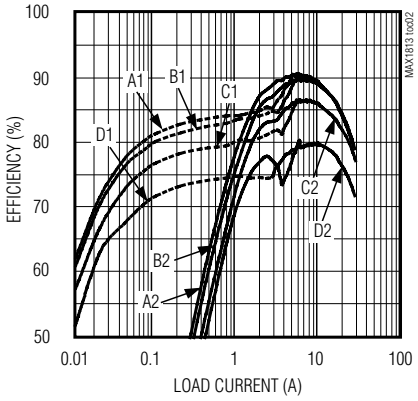
C2: V+ = 15V

D2: V+ = 24V

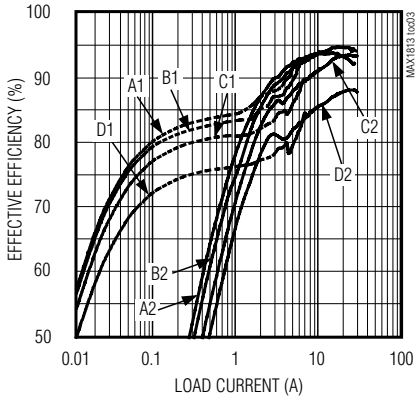
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.4V)



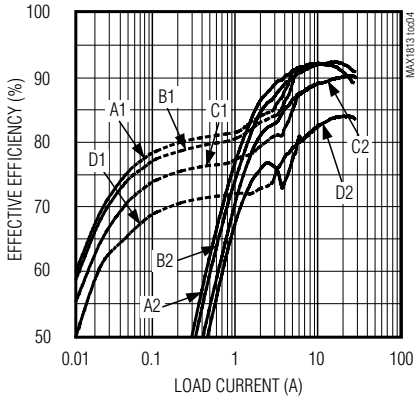
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.1V)



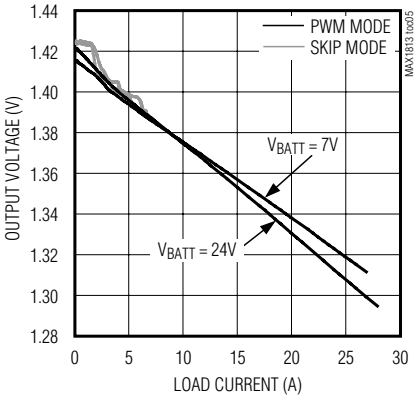
EFFECTIVE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.4V)



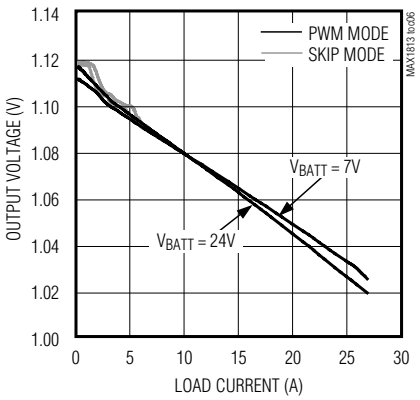
EFFECTIVE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.1V)



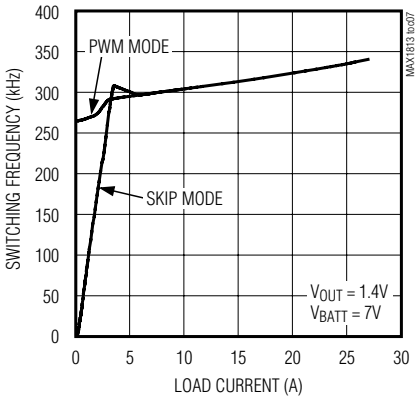
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.4V)



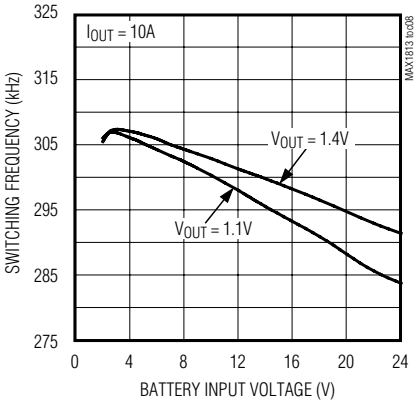
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.1V)



SWITCHING FREQUENCY vs. LOAD CURRENT



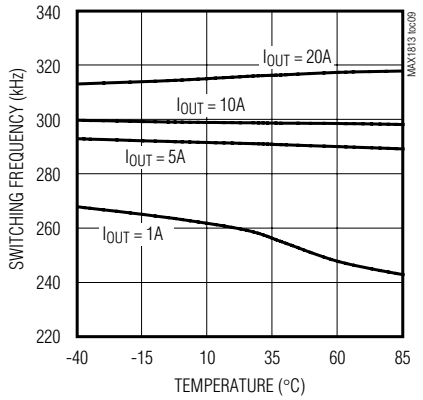
SWITCHING FREQUENCY vs. BATTERY INPUT VOLTAGE



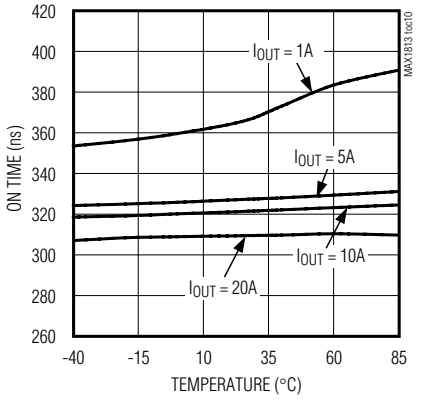
Typical Operating Characteristics (continued)

(Circuit from Figure 1, components from Table 2, T_A = +25°C, unless otherwise noted.)

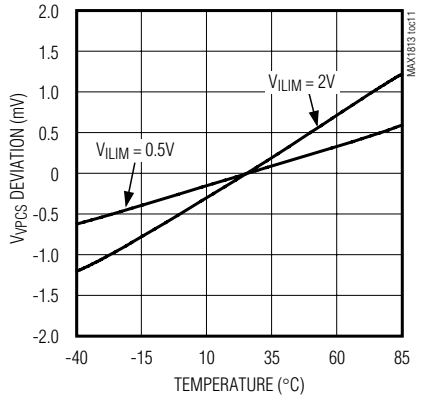
SWITCHING FREQUENCY vs. TEMPERATURE



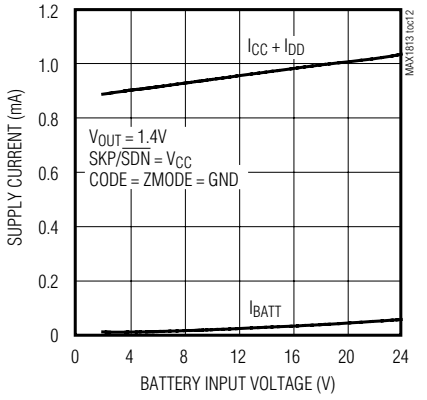
ON TIME vs. TEMPERATURE



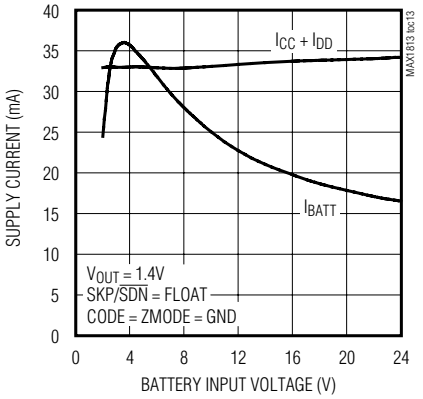
CURRENT-LIMIT DEVIATION vs. TEMPERATURE



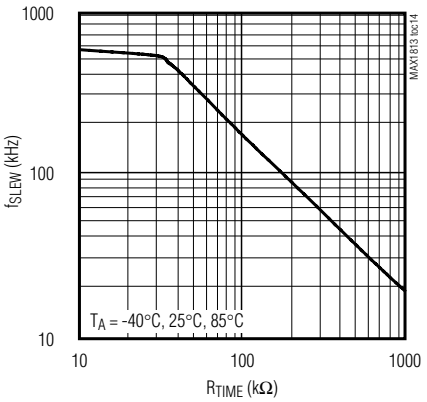
NO-LOAD SUPPLY CURRENT vs. BATTERY INPUT VOLTAGE (SKIP MODE)



NO-LOAD SUPPLY CURRENT vs. BATTERY INPUT VOLTAGE (PWM MODE)



TRANSITION FREQUENCY vs. RTIME

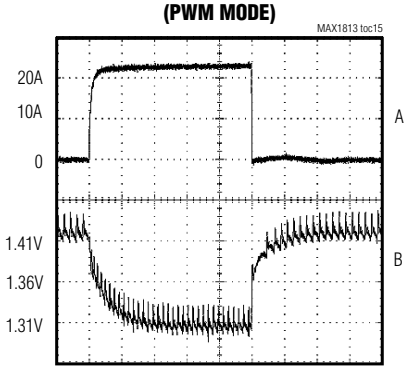


Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

Typical Operating Characteristics (continued)

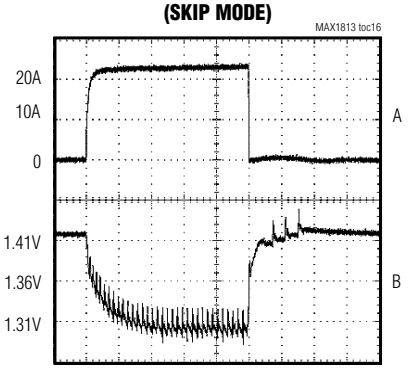
(Circuit from Figure 1, components from Table 2, T_A = +25°C, unless otherwise noted.)

LOAD TRANSIENT (PWM MODE)



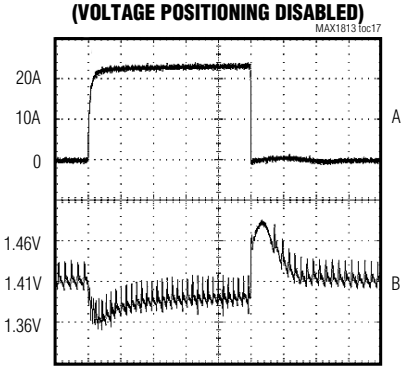
20µs/div
A. I_{OUT} = 0.3A TO 22A, 10A/div
B. V_{OUT} = 1.4V, 50mV/div
SKP/SDN = FLOAT

LOAD TRANSIENT (SKIP MODE)



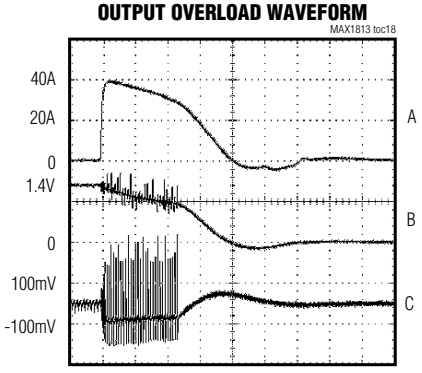
20µs/div
A. I_{OUT} = 0.3A TO 22A, 10A/div
B. V_{OUT} = 1.4V, 50mV/div
SKP/SDN = V_{CC}

LOAD TRANSIENT (VOLTAGE POSITIONING DISABLED)



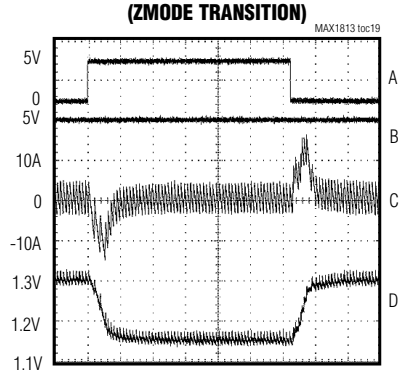
20µs/div
A. I_{OUT} = 0.3A to 22A, 10A/div
B. V_{OUT} = 1.4V, 50mV/div
SKP/SDN = FLOAT

OUTPUT OVERLOAD WAVEFORM



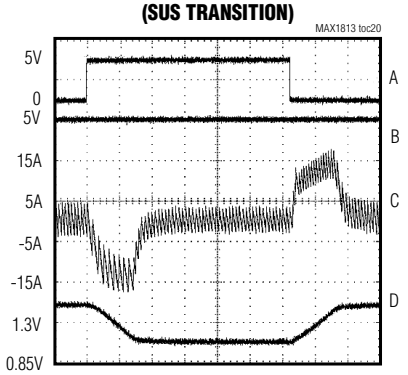
40µs/div
A. I_{OUT} = 0 TO 40A, (0 to 35mΩ), 20A/div
B. V_{OUT} = 1.4V, 1V/div
C. VPCS, 200mV/div
ILIM = V_{CC}

DYNAMIC TRANSITION (ZMODE TRANSITION)



40µs/div
A. V_{ZMODE} = 0 TO 5V, 5V/div
B. PGOOD, 5V/div
C. INDUCTOR CURRENT, 10A/div
D. V_{OUT} = 1.3V TO 1.15V, I_{OUT} = 1A, 100mV/div
CODE = V_{CC}

DYNAMIC TRANSITION (SUS TRANSITION)



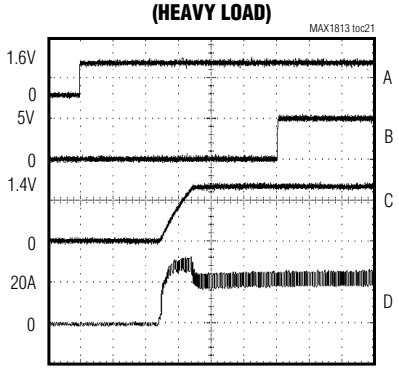
40µs/div
A. V_{SUS} = 0 TO 5V, 5V/div
B. PGOOD, 5V/div
C. INDUCTOR CURRENT, 10A/div
D. V_{OUT} = 1.3V TO 0.85V, I_{OUT} = 1A, 500mV/div
CODE = V_{CC}

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

Typical Operating Characteristics (continued)

(Circuit from Figure 1, components from Table 2, T_A = +25°C, unless otherwise noted.)

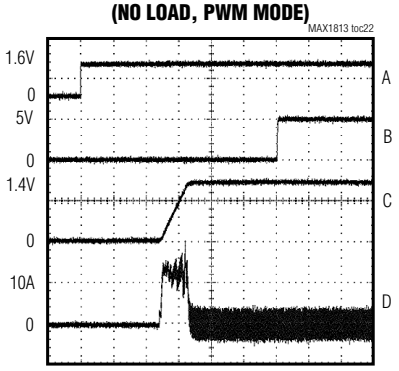
STARTUP WAVEFORM (HEAVY LOAD)



200µs/div

A. $V_{SKP/\overline{SDN}}$ = 0 TO 1.6V, 2V/div
B. PGOOD, 5V/div
C. V_{OUT} = 1.4V, R_{OUT} = 63mΩ, 1V/div
D. INDUCTOR CURRENT, 20A/div

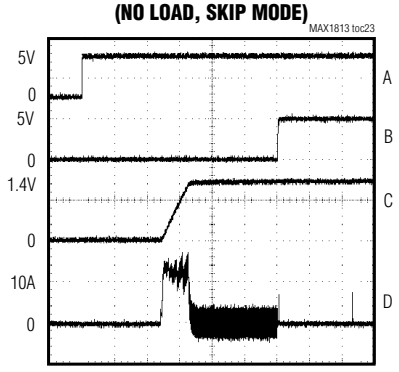
STARTUP WAVEFORM (NO LOAD, PWM MODE)



200µs/div

A. $V_{SKP/\overline{SDN}}$ = 0 TO 1.6V, 2V/div
B. PGOOD, 5V/div
C. V_{OUT} = 1.4V, NO LOAD, 1V/div
D. INDUCTOR CURRENT, 10A/div

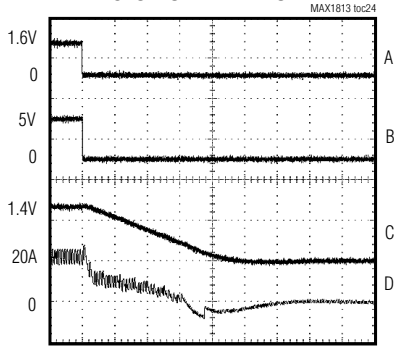
STARTUP WAVEFORM (NO LOAD, SKIP MODE)



200µs/div

A. $V_{SKP/\overline{SDN}}$ = 0 TO 5V
B. PGOOD, 5V/div
C. V_{OUT} = 1.4V, NO LOAD, 1V/div
D. INDUCTOR CURRENT, 10A/div

SHUTDOWN WAVEFORM



40µs/div

A. $V_{SKP/\overline{SDN}}$ = 0 TO 1.6V, 2V/div
B. PGOOD, 5V/div
C. V_{OUT} = 1.4V, R_{OUT} = 63mΩ, 1V/div
D. INDUCTOR CURRENT, 20A/div

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

Pin Description

PIN	NAME	FUNCTION
1	V+	Battery Voltage Sense Connection. Connect V+ to the input power source. V+ is used only for PWM one-shot timing. DH on-time is inversely proportional to the input voltage over a 2V to 28V range.
2	VPCS	Current-Sense Input. Connect a current-sense resistor (R_{SENSE}) between VPCS and PGND. The voltage on VPCS controls both the voltage-positioning and current-limit circuits. The slope of the voltage-positioned output is controlled with the current-sense resistor and the gain resistor connected between CC and REF. See *Setting Voltage Positioning*. The current-limit threshold is set by ILIM. If the current-sense signal (inductor current × R_{SENSE}) exceeds the current-limit threshold, the MAX1813 will not initiate a new cycle. VPCS can also be connected to LX to reduce component count, but CC must be connected to REF to disable the voltage positioning.
3	SKP/$\overline{SDN}$	Combined Shutdown and Skip-Mode Control. Drive SKP/$\overline{SDN}$ to GND for shutdown, leave SKP/$\overline{SDN}$ open for low-noise forced-PWM mode, or drive to V_{CC} for normal pulse-skipping operation: **Shutdown mode:** SKP/$\overline{SDN}$ = GND **Low-noise forced-PWM mode:** SKP/$\overline{SDN}$ = open **Normal pulse-skipping operation:** SKP/$\overline{SDN}$ = V_{CC} Low-noise forced PWM mode causes inductor current recirculation at light loads and suppresses pulse-skipping operation. Forcing SKP/$\overline{SDN}$ with 12V to 15V clears the fault latch and disables undervoltage protection, overvoltage protection, and thermal shutdown with otherwise normal pulse-skipping operation. Exiting shutdown clears the fault latch. **Do not connect SKP/$\overline{SDN}$ to voltages over 15V.**
4	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 470kΩ to 47kΩ resistor sets the clock from 38kHz to 380kHz, respectively: f_{SLEW} = 150kHz x 120kΩ / R_{TIME}.
5	FB	Feedback Input. Connect FB to the junction of the external inductor and output capacitor (Figure 1).
6	CC	Compensation Capacitor and Voltage-Positioning Gain Adjustment. Connect a 47pF to 1000pF (47pF typ) capacitor from CC to GND to adjust the loop's response time. Connect a resistor (R_{AVPS}) from CC to REF to set the gain of the voltage positioning amplifier. $$V_{OUT} = V_{OUT(PROG)} \left[1 + \left(\frac{G_m R_{AVPS} V_{VPCS}}{V_{REF}} \right) \right]$$ where the voltage-positioning amplifer's transconductance (G_m) is typically 20µS.
7, 8	S0, S1	Suspend-Mode Voltage Select Inputs. S0 and S1 are 4-level logic inputs that select the suspend-mode VID code for for the suspend-mode multiplexer inputs. If SUS is high, the suspend-mode VID code is delivered to the DAC. See *Suspend-Mode Internal Mux*.
9	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) through a series 20Ω resistor. Bypass to GND with a 0.22µF or greater capacitor as close to the MAX1813 as possible.
10	TON	On-Time Selection-Control Input. This is a 4-level input used to determine DH on-time. Connect to GND, REF, or V_{CC}, or leave TON unconnected to set the following switching frequencies: GND = 1000kHz, REF = 600kHz, floating = 300kHz, and V_{CC} = 200kHz.

Pin Description (continued)

PIN	NAME	FUNCTION
11	REF	+2.0V Reference Voltage Output. Bypass to GND with a 0.22µF or greater capacitor. The reference can sink and source ±40µA (min) for external loads. Loading REF degrades FB accuracy according to the REF load regulation error.
12	ILIM	Current-Limit Adjustment. The PGND - VPCS current-limit threshold defaults to 50mV if ILIM is tied to V_{CC}. In adjustable mode, the current-limit threshold voltage is 1/10th the voltage seen at ILIM over a 500mV to 2.0V range. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V. Connect ILIM to REF for a fixed 200mV threshold.
13	PGOOD	Open-Drain Power-Good Output. PGOOD is normally high when the output is in regulation. If V_{FB} is not within a +10%/-12.5% window of the DAC setting, PGOOD is asserted low. During DAC code transitions, PGOOD is forced high until 1 clock period after the slew-rate controller finishes the transition. PGOOD is low in shutdown, undervoltage lockout, and during soft-start. Any fault condition forces PGOOD low, and it remains low until the fault is cleared.
14	GND	Analog Ground
15	PGND	Power Ground. PGND is one of the inputs to the current-limit comparator.
16	DL	Low-Side Gate-Driver Output. DL swings from GND to V_{DD}. DL is forced high when a fault occurs, and at the end of the shutdown sequence.
17	V_{DD}	Supply Input for the DL Gate Drive. Connect to the system supply voltage (4.5V to 5.5V). Bypass to PGND with a 1µF or greater capacitor.
18	SUS	Suspend-Mode Control Input. When SUS is high, the suspend-mode VID code, as programmed by S0 and S1, is delivered to the DAC. SUS overrides ZMODE. Connect SUS to GND if the suspend-mode multiplexer is not used. See Table 6.
19	ZMODE	Performance-Mode Mux Contol Input. If SUS is low, ZMODE selects between two different VID codes. If ZMODE = GND with CODE = V_{CC}, or ZMODE = V_{CC} with CODE = GND, the VID code is set by the logic-level voltages on D0–D4. When initially entering impedance mode, the VID code is determined by the impedance at D0–D4. See Tables 5 and 7.
20	CODE	Code Select Input. CODE acts like another VID code input to select between the Intel Mobile Voltage Position II (IMVP-II™) or Coppermine™ VID codes. CODE also determines the polarity of the ZMODE input. See Tables 5 and 7.
21–25	D4–D0	VID Code Inputs. D0 is the LSB and D4 is the MSB of the internal 5-bit DAC (see Tables 5 and 7). If ZMODE = GND with CODE = V_{CC}, or ZMODE = V_{CC} with CODE = GND, D0–D4 are high-impedance digital inputs, and the VID code is set by the logic-level voltages on D0–D4. When initially entering impedance mode, the VID code is determined by the impedance at D0–D4 as follows: Logic Low = source impedance is ≤1kΩ ±5% Logic High = source impedance is ≥100kΩ ±5%.
26	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor and diode according to the standard high-power application circuit (Figure 1). An optional resistor in series with BST allows DH pullup current to be adjusted.
27	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX does not connect to the current-limit comparator.
28	DH	High-Side Gate Driver Output. DH swings from LX to BST.

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

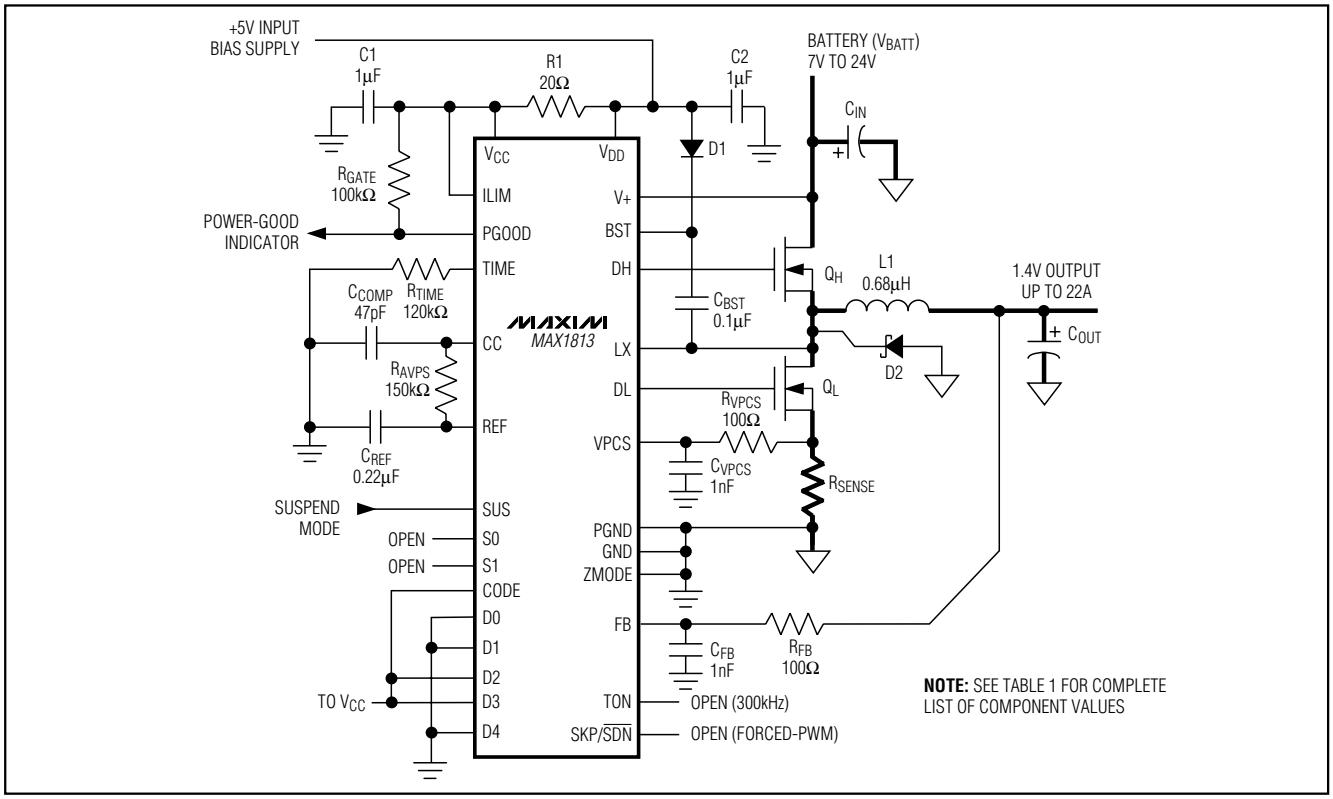


Figure 1. Standard High-Power Application Circuit

Detailed Description

The MAX1813 buck controller is targeted for low-voltage, high-current CPU core power supplies for notebook computers, which typically exhibit 0 to 22A (or greater) load steps. The proprietary Quick-PWM pulse-width modulator in the converter is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PFM schemes.

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1813 requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V supply can be generated with an external linear regulator.

The +5V bias supply powers V_{CC} (PWM controller) and V_{DD} (gate-drive power). The maximum current is:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G1} + Q_{G2}) = 15mA \text{ to } 45mA \text{ (typ)}$$

where I_{CC} is 1.4mA (typ), f_{SW} is the switching frequency, and Q_{G1} and Q_{G2} are the MOSFET total gate-charge specification limits at V_{GS} = 5V.

The battery input (V+) and +5V bias inputs (V_{CC} and V_{DD}) can be connected together if the input source is a fixed 4.5V to 5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal (SKP/$\overline{SDN}$) must be delayed until the battery voltage is present in order to ensure startup.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a constant-on-time, current-mode type with voltage feed-forward

Table 1. Component Selection for Standard Applications

COMPONENT	CIRCUIT 1 (FIGURE 1)
Output Voltage	0.6V to 1.75V
Input Voltage Range	7V to 24V
Maximum Load Current	22A
Inductor	0.68µH Sumida CDEP134H-0R6 or Panasonic ETQP6F0R6BFA
Frequency	300kHz (TON = float)
High-Side MOSFET	International Rectifier (2) IRF7811A
Low-Side MOSFET	Fairchild (3) FDS7764A or International Rectifier (3) IRF7822A
Input Capacitor	(6) 10µF, 25V Taiyo Yuden TMK432BJ106 or TDK C4532X5R1E106M
Output Capacitor	(6) 220µF Panasonic EEFUE0E221R
Current-Sense Resistor	1.5mΩ Dale WSL 2512, plus 0.5mΩ copper PC board trace
ILIM Level	V_{CC} (Default)
Voltage-Positioning Gain Resistor	150kΩ

Table 2. Component Suppliers

MANUFACTURER	PHONE [COUNTRY CODE]	WEBSITE
MOSFETs		
Fairchild Semiconductor	[1] 888-522-5372	www.fairchildsemi.com
International Rectifier	[1] 310-322-3331	www.irf.com
Siliconix	[1] 203-268-6261	www.vishay.com
Capacitors		
Kemet	[1] 408-986-0424	www.kemet.com
Panasonic	[1] 847-468-5624	www.panasonic.com
Sanyo	[65] 281-3226 (Singapore) [1] 408-749-9714	www.secc.co.jp
Taiyo Yuden	[03] 3667-3408 (Japan) [1] 408-573-4150	www.t-yuden.com
Inductors		
Coilcraft	[1] 800-322-2645	www.coilcraft.com
Coiltronics	[1] 561-752-5000	www.coiltronics.com
Sumida	[1] 408-982-9660	www.sumida.com

(Figure 2). This architecture relies on the output ripple voltage to provide the PWM ramp signal. Thus, the output filter capacitor's equivalent series resistance (ESR) acts as a feedback resistor. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage (see *On-Time One-Shot*). Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to the input and output voltages. The high-side switch on-time is inversely proportional to V+ and directly proportional to the output voltage as set by the DAC code. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

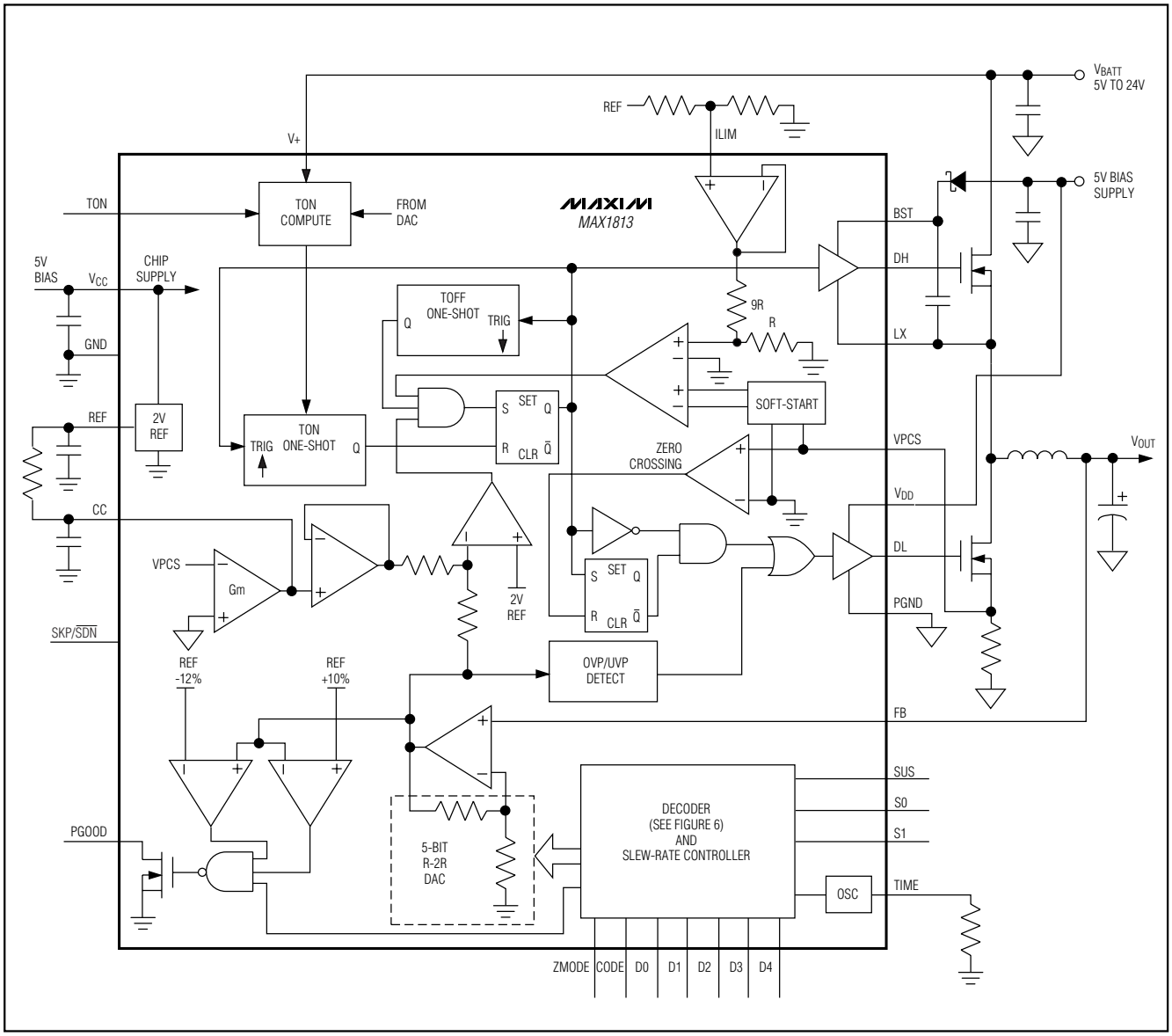


Figure 2. Functional Diagram

easy design methodology and predictable output voltage ripple.

$$t_{ON} = \frac{K(V_{OUT} + 75mV)}{V_{IN}}$$

where K is set by the TON pin-strap connection, and 75mV is an approximation to accommodate for the expected drop across the low-side MOSFET switch and current-sense resistor (Table 3).

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* table. On-times at operating points far removed from the conditions specified can vary over a wide range. For example, the 1000kHz setting will typically run about 10% slower with inputs much greater than +5V, due to the very short on-times required.

Although the on-time is set by TON, the input voltage, and the output voltage, other factors also contribute to the overall switching frequency. The on-time guaranteed in the *Electrical Characteristics* table is influenced by switching delays in the external high-side MOSFET. Resistive losses—including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground—tend to raise the switching frequency at higher output currents. Switch dead-time can increase the effective on-time, reducing the switching frequency. This effect occurs only in PWM mode (SKP/$\overline{SDN}$ = float) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead-time (26ns typ).

When the controller operates in continuous mode, the dead-time is no longer a factor, and the actual switching frequency is:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time calculated by the MAX1813.

Automatic Pulse-Skipping Switchover

In skip mode (SKP/$\overline{SDN}$ = high, Table 4), an inherent automatic switchover to PFM takes place at light loads (Figure 3). This switchover is controlled by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. For a 7V to 24V input voltage range, this threshold is relatively constant, with

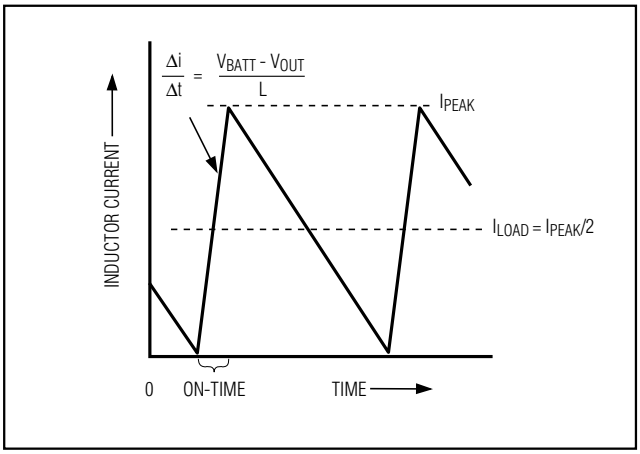


Figure 3. Pulse-Skipping/Discontinuous Crossover Point

Table 3. Approximate K-Factor Errors

TON SETTING (kHz)	K-FACTOR (µs)	APPROXIMATE K-FACTOR ERROR (%)	MINIMUM RECOMMENDED V_{BATT} AT V_{OUT} = 1.4V (V)
200	4.9	±9	1.8
300	3.3	±10	2.0
600	1.8	±13	2.9
1000	1.05	±13	3.5

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Table 4. Operating Mode Truth Table

SKP/$\overline{SDN}$	DL	MODE	COMMENTS
GND	High	Shutdown	Micropower shutdown state (I_{CC} = 2µA typ).
V_{CC}	Switching	Normal Operation	Automatic switchover from PWM mode to pulse-skipping PFM mode at light loads. Prevents inductor current from recirculating into the input.
Float	Switching	Forced PWM	Low-noise forced-PWM mode causes inductor current to reverse at light loads and suppresses pulse-skipping operation.
12V	Switching	NO-FAULT Test Mode	Test mode with overvoltage, undervoltage, and thermal shutdown faults disabled. Otherwise, the converter operates as if SKP/$\overline{SDN}$ = V_{CC}.
V_{CC} or Float	High	FAULT	The fault latch set by the overvoltage protection, output undervoltage protection, or thermal shutdown. The MAX1813 will remain in FAULT mode until V_{CC} power is cycled or SKP/$\overline{SDN}$ is forced low.

only a minor dependence on the input voltage:

$$I_{LOAD(SKIP)} \approx K \left(\frac{V_{OUT}}{2L} \right) \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$

where K is the on-time scale factor (Table 3). The load-current level at which PFM/PWM crossover occurs ($I_{LOAD(SKIP)}$) is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 3). For example, in the standard application circuit with K = 3.3µs (300kHz), V_{IN} = 12V, V_{OUT} = 1.4V, and L = 0.68µH, switchover to pulse-skipping operation occurs at I_{LOAD} = 3.0A or about 1/4 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation; this is a normal operating condition that improves light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Forced-PWM Mode

The low-noise, forced-PWM mode (SKP/$\overline{SDN}$ left floating, Table 4) disables the zero-crossing comparator that controls the low-side switch on-time. The resulting low-side gate-drive waveform is forced to be the complement of the high-side gate-drive waveform. This, in turn, causes the inductor current to reverse at light loads because the PWM loop strives to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency nearly constant, but it results in higher no-load supply current that can be 15mA to 45mA, depending on the external MOSFETs and switching frequency.

The MAX1813 uses forced-PWM mode during all transitions, while the slew-rate controller is active. During downward output voltage transitions, forced-PWM allows the MAX1813 to sink current, thereby rapidly pulling down the output voltage. When a transition uses high negative inductor current, due to voltage positioning, the output voltage may not settle to its intended final value until after the slew-rate controller terminates. For this reason, most applications should use PWM mode exclusively, although skip mode is beneficial in the low-power suspend state (see *Shutdown and Mode Control*).

Shutdown and Mode Control (SKP/$\overline{SDN}$)

When SKP/$\overline{SDN}$ is driven low, the MAX1813 enters the low-current shutdown mode (Table 4). Shutdown forces PGOOD low immediately and ramps down the output voltage in 25mV increments at the clock rate set by R_{TIME}. Once the output voltage ramps down, the MAX1813 pulls DH low, forces DL high, and shuts down the reference, so the total supply current (I_{CC} + I_{DD} + I+) drops to 4µA (typ).

When SKP/$\overline{SDN}$ is left floating or driven high, the MAX1813 begins the startup sequence. First, the reference powers up. After the reference exceeds its 1.6V undervoltage lockout threshold, the DAC determines the target output voltage and starts ramping up the output voltage. The slew-rate controller increases the out-

put voltage in 25mV increments at the clock rate set by R_{TIME} until the MAX1813 reaches the selected output voltage. The MAX1813 does not feature traditional variable current-limit soft-start, so full output current is immediately available. Once the slew-rate controller terminates, output undervoltage fault blanking period ends, and the output voltage is in regulation, PGOOD goes high.

Leave SKP/$\overline{SDN}$ floating for forced-PWM operation, or connect SKP/$\overline{SDN}$ to V_{CC} for normal operation. During all transitions, the MAX1813 uses PWM mode while the slew-rate controller is active. Exiting shutdown clears the fault latch.

Current-Limit Circuit (ILIM)

The current-limit circuit employs a unique "valley" current-sensing algorithm. If the current-sense signal is above the current-limit threshold, the MAX1813 will not initiate a new cycle (Figure 4). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore the exact current-limit characteristic and maximum load capability are a function of the current-limit threshold, inductor value, and input voltage. The reward for this uncertainty is robust, loss-less over-current sensing. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and therefore tracks the positive current limit when ILIM is adjusted.

The MAX1813 measures the current by sensing the voltage between VPCS and PGND. Connect an external sense resistor between the source of the low-side N-channel MOSFET and PGND. The signal provided by this current-sense resistor is also used for voltage positioning (see *Setting Voltage Positioning*). Reducing the sense voltage increases the relative measurement error. However, the configuration eliminates the uncertainty of using the low-side MOSFET on-resistance to measure the current, so the resulting current-limit tolerance is tighter when sensing with a 1% sense resistor.

The voltage at ILIM sets the current-limit threshold. For voltages from 500mV to 2V, the current-limit threshold voltage is precisely 0.1 x V_{ILIM}. Set this voltage with a resistive divider between REF and GND. The current-limit threshold defaults to 50mV when ILIM is tied to V_{CC}. The logic threshold for switchover to this 50mV default value is approximately V_{CC} - 1V.

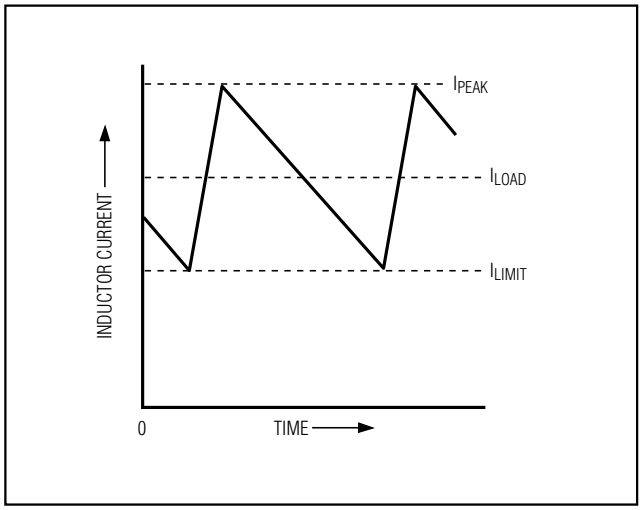

Figure 4. "Valley" Current-Limit Threshold Point

Carefully observe the PC board layout guidelines to ensure that noise and DC errors don't corrupt the current-sense signals seen by VPCS and GND. The IC must be mounted close to the current-sense resistor with short, direct traces making a Kelvin sense connection (see *PC Board Layout Guidelines*).

MOSFET Gate Drivers (DH and DL)

The DH and DL drivers are optimized for driving moderate-sized, high-side and larger, low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1813 will interpret the MOSFET gate as "off" while there is actually charge still left on the gate. Use very short, wide traces (50 to 100 mils wide if the MOSFET is 1 inch from the device). The dead time at the other edge (DH turning off) is determined by a fixed 35ns internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.4Ω (typ) on-resistance. This helps prevent DL from being pulled up during the fast rise-time of the LX node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, some combinations of high- and low-side FETs may cause excessive gate-drain coupling, leading to poor

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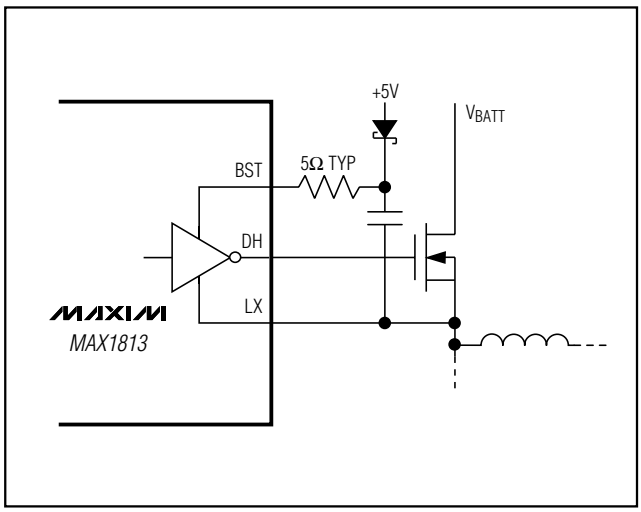

Figure 5. Reducing the Switching-Node Rise Time

efficiency, EMI, and shoot-through currents. This is often remedied by adding a resistor less than 5Ω in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 5).

DAC Converter (D0-D4)

The digital-to-analog converter (DAC) programs the output voltage. It receives a preset digital code from the CPU pins, digital logic, general-purpose I/O, or an external multiplexer. Do not leave D0–D4 floating; use 1MΩ or less pullups if the inputs may float.

The state of DO–D4 can be changed while the switch-mode power supply is active, initiating a transition to a new output voltage level. During this interval, the slew-rate controller is active, so the MAX1813 uses forced-PWM mode. If this mode of DAC control is used, connect ZMODE low. Change D0–D4 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages (Table 5) are compatible with the Coppermine™ and Intel's Mobile Voltage Positioning II (IMVP-II™) specifications.

VID Code Options (CODE)

The MAX1813 contains two separate sets of VID codes. The CODE pin selects between the two output voltage tables (Table 5). Drive CODE low to select the older 0.925V to 2.000V DAC codes, which are compatible with the Coppermine specifications. Drive CODE high to select the new 0.600V to 1.750V DAC codes, which are compatible with the IMVP-II specifications. CODE also determines the polarity of ZMODE (Table 7).

Suspend-Mode Operation (S0, S1)

When the CPU clock stops, the processor enters suspend mode and requires a lower supply voltage to minimize power consumption. The MAX1813 includes suspend-mode output voltages that are selected using two 4-level input pins (S0 and S1, Table 6). When the CPU clock stops, drive SUS high to transition to the suspend-mode output voltage. During the transition, the MAX1813 asserts forced-PWM mode to sink current and pull down the output voltage until PGOOD goes high.

When SUS is driven high, suspend mode overrides the 5-bit DAC setting. When SUS is low, the MAX1813 determines the output voltage from the 5-bit DAC (D0–D4), CODE, and ZMODE settings.

Internal Multiplexers (ZMODE, SUS)

The MAX1813 has a unique internal multiplexer that can select one of three different VID code settings for different processor states. Depending on the logic level at SUS, the suspend (SUS) mode multiplexer selects the VID code settings from either the D0-D4 input decoder or the S0/S1 input decoder. The ZMODE multiplexer selects one of the two D0-D4 input modes, setting the VID code based on either the voltage on D0-D4 (logic mode) or the impedance decoder output (impedance mode) (Figure 6).

When SUS is high, the suspend-mode multiplexer selects the VID code from the S0/S1 input decoder. The decoder outputs are determined by inputs S0 and S1 (Table 6). When SUS is low, the suspend-mode multiplexer selects the D0-D4 input decoder output.

In logic mode (Table 7), the logic-level voltages on D0-D4 set the DAC settings. In this mode, the inputs are continuously active and can be dynamically changed by external logic. The logic-mode VID code setting is typically used for the battery-mode state, and the source of this code is sometimes the VID pins of the CPU with suitable pullup resistors.

Impedance mode (Table 7) is programmed by external resistors in series with D0–D4, using a unique scheme that allows two sets of data bits using only one set of pins. When the MAX1813 initially enters impedance mode, the resistances at D0–D4 are sampled by the impedance decoder to see if there is a large resistance in series with the pin. If the voltage level on a DAC input pin is a logic low, an internal switch connects that pin to

Table 5. Output Voltage vs. DAC Codes

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	
					CODE = 0	CODE = 1
0	0	0	0	0	2.000	1.750
0	0	0	0	1	1.950	1.700
0	0	0	1	0	1.900	1.650
0	0	0	1	1	1.850	1.600
0	0	1	0	0	1.800	1.550
0	0	1	0	1	1.750	1.500
0	0	1	1	0	1.700	1.450
0	0	1	1	1	1.650	1.400
0	1	0	0	0	1.600	1.350
0	1	0	0	1	1.550	1.300
0	1	0	1	0	1.500	1.250
0	1	0	1	1	1.450	1.200
0	1	1	0	0	1.400	1.150
0	1	1	0	1	1.350	1.100
0	1	1	1	0	1.300	1.050
0	1	1	1	1	NO CPU*	1.000
1	0	0	0	0	1.275	0.975
1	0	0	0	1	1.250	0.950
1	0	0	1	0	1.225	0.925
1	0	0	1	1	1.200	0.900
1	0	1	0	0	1.175	0.875
1	0	1	0	1	1.150	0.850
1	0	1	1	0	1.125	0.825
1	0	1	1	1	1.100	0.800
1	1	0	0	0	1.075	0.775
1	1	0	0	1	1.050	0.750
1	1	0	1	0	1.025	0.725
1	1	0	1	1	1.000	0.700
1	1	1	0	0	0.975	0.675
1	1	1	0	1	0.950	0.650
1	1	1	1	0	0.925	0.625
1	1	1	1	1	NO CPU*	0.600

**In the NO CPU State, DH and DL are held low and the slew-rate controller is set for 0.425V.*

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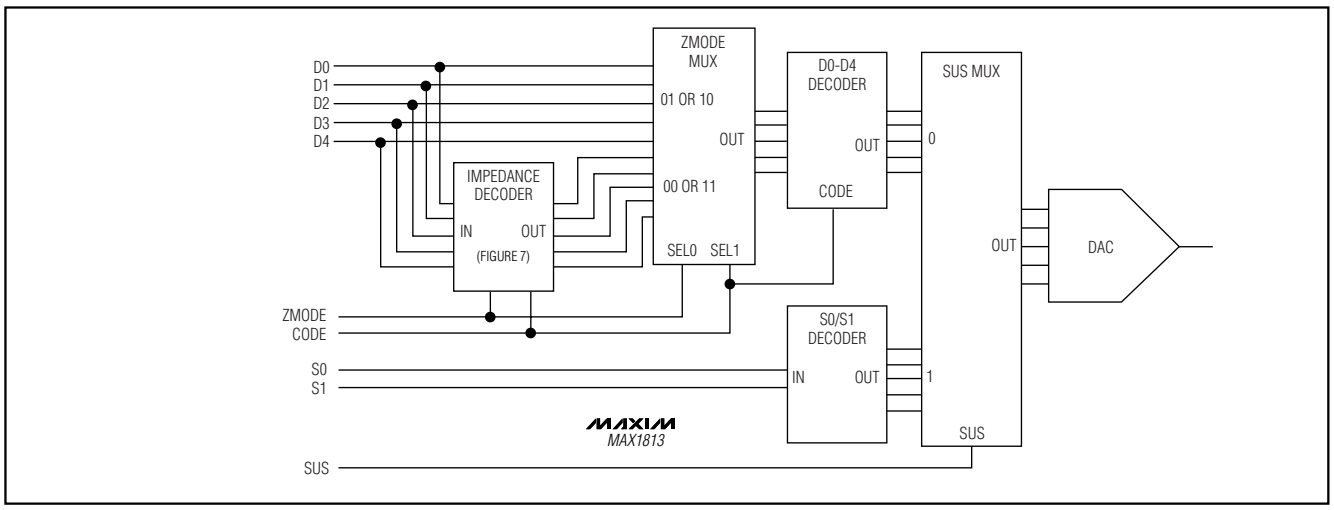

Figure 6. Internal Multiplexers Block Diagram

an internal 40kΩ pullup for about 4µs to see if the pin voltage can be forced high (Figure 7). If the pin voltage cannot be pulled to a logic high, the pin is considered low impedance, and its impedance-mode logic state is low. If the pin can be pulled to a logic high, the impedance is considered high and so is the impedance-mode logic state. Similarly, if the voltage level on the pin is a logic high, an internal switch connects the pin to an internal 8kΩ pulldown to see if the pin voltage can be forced low. If so, the pin is high impedance, and its impedance-mode logic state is high. In either sampling condition, if the pin's logic level does not change, the pin is determined to be low impedance, and the impedance-mode logic state is low.

A high pin impedance (logic high) is 100kΩ or greater, and a low impedance (logic low) is 1kΩ or less. The guaranteed levels for these impedances are 95kΩ and 1.05kΩ to allow the use of standard 100kΩ and 1kΩ resistors with 5% tolerance.

Output Voltage Transition Timing (TIME)

The MAX1813 is designed to perform output voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance. This makes the IC very suitable for IMVP-II CPUs and other CPUs that operate in two or more modes with different core voltage levels.

The IMVP-II CPUs operate at multiple clock frequencies and require multiple core voltages. When transitioning

Table 6. Suspend-Mode Output Voltages

S1	S0	OUTPUT VOLTAGE (V)
GND	GND	0.975
GND	REF	0.950
GND	Float*	0.925
GND	V_{CC}	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float*	0.825
REF	V_{CC}	0.800
Float*	GND	0.775
Float*	REF	0.750
Float*	Float*	0.725
Float*	V_{CC}	0.700
V_{CC}	GND	0.675
V_{CC}	REF	0.650
V_{CC}	Float*	0.625
V_{CC}	V_{CC}	0.600

**Float = no connection*

Table 7. ZMODE Polarity Table

CODE	ZMODE	
0	0	Impedance Mode
0	1	Logic Mode
1	0	Logic Mode
1	1	Impedance Mode

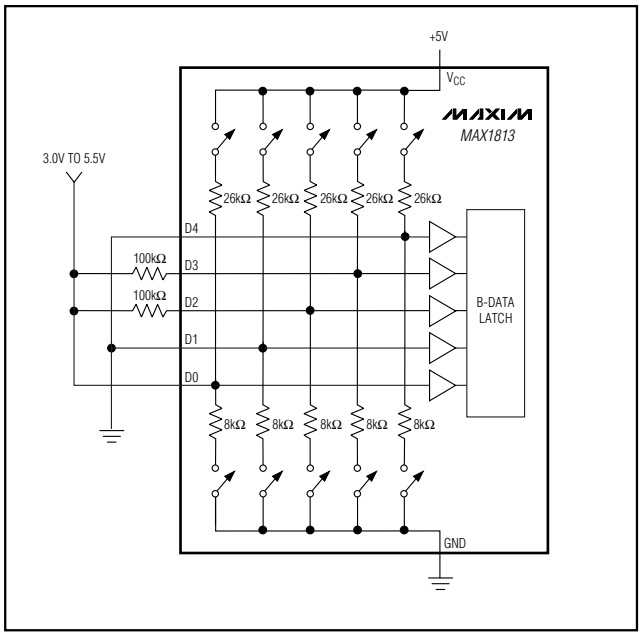

Figure 7. Internal Mux Impedance-Mode Data Test and Latch

from one clock frequency to another, the CPU first goes into a low-power state, then the output voltage and clock frequency are changed. The change must be accomplished in 100µs or the system may halt.

At the beginning of an output voltage transition, the MAX1813 forces the PGOOD output high. PGOOD remains masked high until the slew-rate controller has set the internal DAC to the final value and one additional slew-rate clock period has passed.

The output voltage transition is performed in 25mV increments, preceded by a 4µs delay and followed by one additional clock period after which PGOOD will remain high if the output voltage is in regulation. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX1813's slew-rate clock. The greater the output capacitance, the higher the surge current required for the transition. The MAX1813 will automatically control the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less than the current limit set by ILIM. The transition time is given by:

$$t_{TRAN} \leq 4\mu s + \left[\frac{1}{f_{SLEW}}\left(1+\frac{V_{OLD}-V_{NEW}}{25mV}\right)\right]$$

where f_{SLEW} = 150kHz x 120kΩ/R_{TIME}, V_{OLD} is the original output voltage, and V_{NEW} is the new output voltage. See TIME Frequency Accuracy in *Electrical Characteristics* for f_{SLEW} accuracy.

The practical range of R_{TIME} is 47kΩ to 470kΩ, corresponding to 2.6µs to 26µs per 25mV step. Although the DAC takes discrete 25mV steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times 25mV \times f_{SLEW}$$

Power-On Reset and Undervoltage Lockout

V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching, forces PGOOD low, and forces the DL gate driver high. If the V_{CC} voltage drops below 4.2V, it is assumed that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, DL is forced high in this mode; this will force the output to ground. This results in large negative inductor current and possibly small negative output voltages. If V_{CC} is likely to drop in this fashion, the output can be clamped with a Schottky diode to PGND to reduce the negative excursion.

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V. This resets the fault latch and prepares the PWM for operation. When V_{CC} rises above 4.2V, the DAC inputs are sampled, and the output voltage begins to slew to the DAC setting. To ensure correct startup, V+ should be present before V_{CC}. If the converter attempts to bring the output into regulation without V+ present, the fault latch will trip. For automatic startup, the battery voltage (V+) should be present before V_{CC}. The SKP/$\overline{SDN}$ pin can be forced low or V_{CC} power cycled to reset the fault latch.

Power-Good Output (PGOOD)

PGOOD is the open-drain output of a window comparator. This power-good output remains high impedance as long as the output voltage is within +10%/-12.5% of the regulation voltage. When the output voltage is greater than 10% or less than the -12.5% window limits, the internal MOSFET is activated and pulls the output low. While the slew-rate controller is active (except during startup and shutdown), the MAX1813 forces PGOOD high. PGOOD is low in shutdown, input undervoltage lockout, and during startup. Any fault condition forces PGOOD low until the fault is cleared. For logic-level output voltages, connect an external pullup resistor between PGOOD and V_{CC} (or V_{DD}). A 100kΩ resistor works well in most applications.

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Output Overvoltage Protection

The overvoltage protection circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and activating the battery's protection circuit. The output voltage is continuously monitored for overvoltage. If the output exceeds the overvoltage threshold, the fault protection is triggered and the circuit shuts down. The DL low-side gate-driver output latches high, which turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor, forcing the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery's protection circuit will engage. The MAX1813 is latched off and won't restart until SKP/$\overline{SDN}$ is toggled or V_{CC} power is cycled.

Overvoltage protection can be defeated using the no-fault test mode (see *No-Fault Test Mode*).

Output Undervoltage Protection

The output undervoltage protection (UVP) function is similar to foldback current limiting but employs a timer rather than a variable current limit. If the MAX1813 output voltage is under 70% of the nominal value, the PWM is latched off and won't restart until SKP/$\overline{SDN}$ is toggled or V_{CC} power is cycled. To allow startup, UVP is ignored during the undervoltage fault-blanking time (the first 256 cycles of the slew rate after startup).

UVP can be defeated using the no-fault test mode (see *No-Fault Test Mode*).

Thermal Fault Protection

The MAX1813 features a thermal fault protection circuit. When the temperature rises above +160°C, the DL low-side gate-driver output latches high until SKP/$\overline{SDN}$ is toggled or V_{CC} power is cycled. The threshold has +15°C of thermal hysteresis, which prevents the regulator from restarting until the die cools off.

Thermal shutdown can be defeated using the no-fault test mode (see *No-Fault Test Mode*).

No-Fault Test Mode

The over/undervoltage protection features can complicate the process of debugging prototype breadboards since there are at most a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to disable the overvoltage protection, undervoltage protection, and thermal shutdown features, and clear the fault latch if it has been set. In "no-fault" test mode, the regulator operates as if SKP/$\overline{SDN}$ were high (SKIP mode). Forcing 12V to 15V on SKP/$\overline{SDN}$ activates no-fault test mode.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input voltage range: The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Maximum load current: There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

Switching frequency: This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN2}. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

Inductor operating point: This choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

The MAX1813's pulse-skipping algorithm initiates skip mode at the critical-conduction point. Thus, the inductor operating point also determines the load-current value at which PFM/PWM switchover occurs. The optimum operating point is usually found between 20% and 50% ripple current.

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output fil-

ter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L(I_{LOAD1} - I_{LOAD2})^2 \left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})K}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see *Electrical Characteristics*), and K is from Table 3.

Inductor Selection

The switching frequency and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

Example: $I_{LOAD(MAX)}$ = 22A, V_{IN} = 12V, V_{OUT} = 1.4V, f_{SW} = 300kHz, 30% ripple current, or LIR = 0.3.

$$L = \frac{1.4V \times (12V - 1.4V)}{12V \times 300kHz \times 22A \times 0.3} = 0.62\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}).

$$I_{PEAK} = I_{LOAD(MAX)} + (I_{LOAD(MAX)} \times LIR / 2)$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current; therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)}LIR}{2}\right)$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by R_{SENSE}. For the 50mV default setting, the minimum current-limit threshold is 40mV.

Connect ILIM to V_{CC} for a default 50mV current-limit threshold. In the adjustable mode, the current-limit threshold is precisely 1/10th the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to GND, with ILIM connected to the center tap. The external 0.5V to 2.0V adjustment range corresponds to a 50mV to 200mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a 10µA divider current to prevent a significant increase of errors in the current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} = V_{STEP(MAX)} / I_{LOAD(MAX)}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} equation in the *Design Procedure*). The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{I_{PEAK}^2 L}{2C_{OUT}V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

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$$f_{ESR} = \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors in wide-spread use at the time of publication have typical ESR zero frequencies below 30kHz. In the standard application used for inductor selection, the ESR needed to support a 30mVp-p ripple is 30mV/(22A x 0.3) = 4.5mΩ. Six 220µF/2.5V Panasonic SP capacitors in parallel provide 2.5mΩ (max) ESR. The capacitors' typical ESR results in a zero at 48kHz.

Don't put high-value ceramic capacitors directly across the output without taking precautions to ensure stability. Ceramic capacitors have a high ESR zero frequency and may cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the junction of the inductor and the FB pin.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feed-back loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there isn't enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can cause the output voltage to rise above or fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to monitor simultaneously the inductor current with an AC current probe. Don't allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1813 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>20A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (Q_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of Q_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of Q_H. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two SO-8s, DPAK or D^2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (Q_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\ (Q_H\ Resistive) = \frac{V_{OUT} I_{LOAD}^2 R_{DS(ON)}}{V_{IN}}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation specifications often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in the high-side MOSFET (Q_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on Q1:

$$PD\ (Q_H\ Switching) = \frac{V_{IN(MAX)}^2 C_{RSS} f_{SW} I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q_H, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC-adapter voltages are applied, due to the squared term in the C x V_{IN}^2 x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (Q_L), the worst-case power dissipation always occurs at the maximum input voltage:

$$PD\ (Q_L\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right] I_{LOAD}^2 R_{DS(ON)}$$

The worst case MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D1) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 of the load current. This diode is optional and can be removed if efficiency isn't critical.

Setting Voltage Positioning

Voltage positioning dynamically changes the output voltage set point in response to the load current. When the output is loaded, the signal fed back from the VPCS input adjusts the output voltage set point, thereby decreasing power dissipation. The load-transient response of this control loop is extremely fast yet well controlled, so the amount of voltage change can be accurately confined within the limits stipulated in the microprocessor power-supply guidelines. To understand the benefits of dynamically adjusting the output voltage, see *Voltage Positioning and Effective Efficiency*.

The amount of output voltage change is adjusted by an external gain resistor (R_{AVPS}). Place R_{AVPS} between REF and CC (Figure 8). The voltage developed across the current-sense resistor (V_{VPCS}) relates to the output voltage as follows:

$$V_{OUT} = V_{OUT(PROG)} \left[1 + \left(\frac{G_m R_{AVPS} V_{VPCS}}{V_{REF}}\right)\right]$$

where $V_{OUT(PROG)}$ is the programmed output voltage set by the DAC code (Table 5), and the VPCS transconductance (G_m) is typically 20µS (see *Electrical Characteristics*). The MAX1813 contains internal clamps to limit the voltage positioning between 10% below and 2% above the programmed output voltage.

The MAX1813 determines the load current from the voltage across the current-sense resistor (R_{SENSE}) between the source of the low-side MOSFET and PGND. Therefore, the current-sense voltage present at VPCS is determined by:

$$V_{VPCS} = -I_{LOAD} R_{SENSE} (1-D)$$

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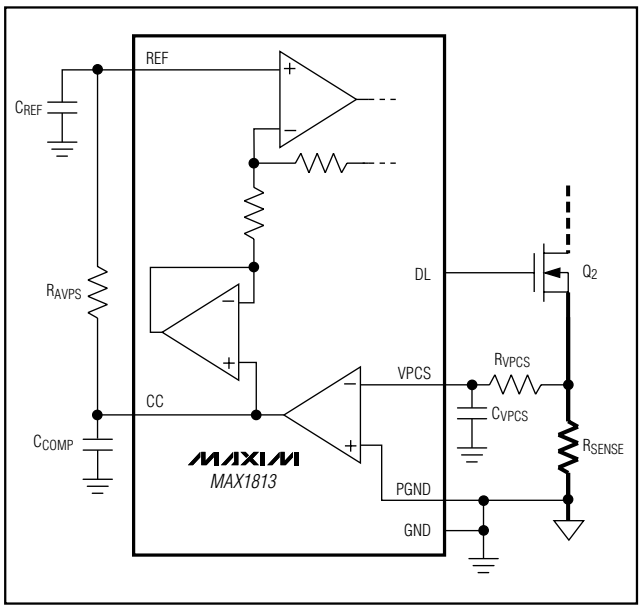

Figure 8. Voltage-Positioning Block Diagram

where D = V_{OUT}/V_{IN} is the regulator's duty cycle. However, since the ratio of the output-to-input voltage is usually relatively large, the effect of the duty cycle on the circuit's performance is not significant. Therefore, the complete expression for the voltage-positioned output depends upon the load current, the value of the voltage-positioning gain resistor, and the value of the current-sense resistor:

$$V_{OUT} \approx V_{OUT(PROG)} \left[1 - \left(\frac{G_m R_{AVPS} R_{SENSE} I_{LOAD}}{V_{REF}} \right) \right]$$

The MAX1813 voltage-positioning circuit has several advantages over older circuits, which added a fixed voltage offset on the sense point and used a low-value resistor in series with the output. The new circuit uses the same current-sense resistor for both voltage positioning and current-limit detection. This simultaneously provides accurate current limiting and voltage positioning. Since the new circuit adjusts the output voltage within the control loop, the voltage-positioning signal may be internally amplified. The additional gain allows the use of low-value current-sense resistors, so the power dissipated in this sense resistor is significantly lower than a single resistor connected directly in series with the output.

The current-sense signal from the sense resistor to the VPCS pin should be filtered to eliminate the effect of switching noise on the voltage-positioned output. A simple low-pass RC filter with a 100ns time constant (100Ω x 1000pF) sufficiently reduces the noise on the current-sense signal (Figure 8).

Voltage-Positioning Compensation (CC)

The voltage-positioning compensation capacitor filters the amplified VPCS signal, allowing the user to adjust the dynamics of the voltage-positioning loop. Since the output impedance of the transconductance amplifier is much greater than R_{AVPS}, the pole provided by this node can be approximated by $1/(2\pi R_{AVPS} C_{COMP})$. The response time is set with a 47pF to 1000pF capacitor from CC to GND.

Applications Information

Voltage Positioning and Effective Efficiency

Powering new mobile processors requires careful attention to detail to reduce cost, size, and power dissipation. As CPUs became more power hungry, it was recognized that even the fastest DC-DC converters were inadequate to handle the transient power requirements. After a load transient, the output instantly changes by $ESR_{COUT} \times \Delta I_{LOAD}$. Conventional DC-DC converters respond by regulating the output voltage back to its nominal state after the load transient occurs (Figure 9). However, the CPU only requires that the output voltage remains above a specified minimum value. Dynamically positioning the output voltage to this lower limit allows the use of fewer output capacitors and reduces power consumption under load.

For a conventional (nonvoltage-positioned) circuit, the total voltage change is:

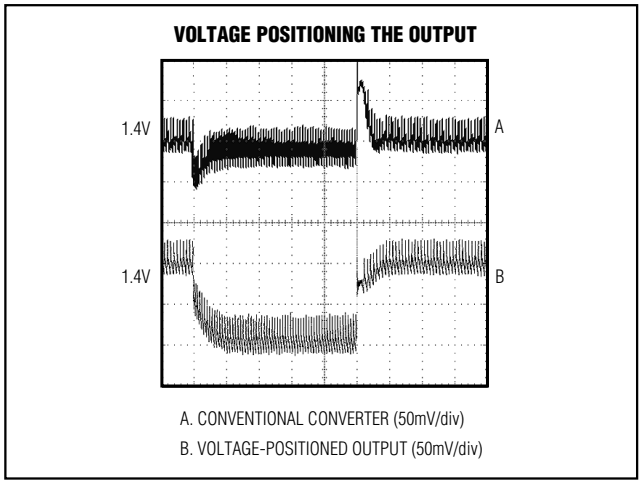

Figure 9. Voltage Positioning the Output

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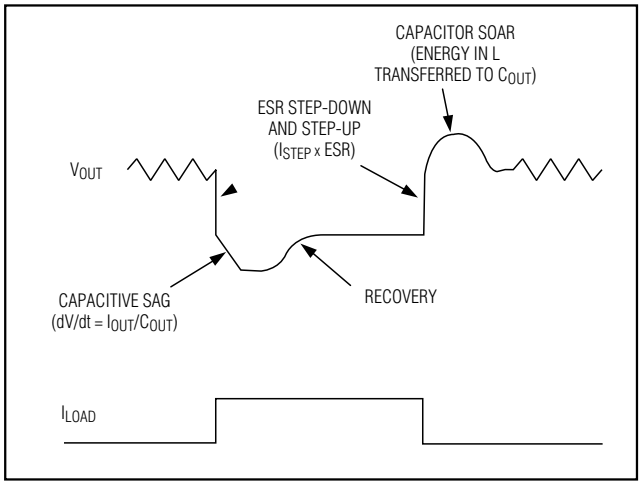

Figure 10. Transient-Response Regions

$$V_{P-P1} = 2 \times (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in Figure 10. Setting the converter to regulate at a lower voltage when under load allows a larger voltage step when the output current suddenly decreases (Figure 9). So the total voltage change for a voltage-positioned circuit is:

$$V_{P-P2} = (ESR_{COUT} \times \Delta_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in the *Design Procedure*. Since the amplitudes are the same for both circuits ($V_{P-P1} = V_{P-P2}$), the voltage-positioned circuit requires only twice the ESR. Since the ESR specification is achieved by paralleling several capacitors, fewer units are needed for the voltage-positioned circuit.

An additional benefit of voltage positioning is reduced power consumption at high load currents. Because the output voltage is lower under load, the CPU draws less current. The result is lower power dissipation in the CPU, although some extra power is dissipated in R_{SENSE}. However, the gain of the voltage positioning block reduces the power dissipation in R_{SENSE}. For a nominal 1.4V, 22A output (R_{LOAD} = 63.6mΩ), reducing the output voltage 6% gives a 1.32V output voltage and a 20.7A output current. Given these values, CPU power consumption is reduced from 30.8W to 27.3W. The additional power consumption of R_{SENSE} is:

$$2.0m\Omega \times (20.7A)^2 = 0.86W$$

and the overall power savings is:

$$30.8W - (27.3W + 0.86W) = 2.62W$$

In effect, 2.62W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial. Effective efficiency is defined as the efficiency required of a non-voltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

Calculate effective efficiency:

1) Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).
2) Model the load resistance for each data point: $R_{LOAD} = V_{OUT} / I_{OUT}$
3) Calculate the output current that would exist for each R_{LOAD} data point in a nonpositioned application:
   $$I_{NP} = V_{NP} / R_{LOAD}$$
   where V_{NP} = 1.4V (in this example).
4) Calculate effective efficiency as: Effective efficiency = ($V_{NP} \times I_{NP}$) / ($V_{IN} \times I_{IN}$) = calculated nonpositioned power output divided by the measured voltage-positioned power input.
5) Plot the efficiency data point at the nonpositioned current, I_{NP}.

The effective efficiency of voltage-positioned circuits is shown in the *Typical Operating Characteristics*.

Dropout Performance

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3). Also, keep in mind that transient-response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure*).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of ability to slew the inductor current higher in response to increased load and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and V_{SAG} greatly increases unless additional output capacitance is used.

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A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{1-\left(\frac{h \times t_{OFF(MIN)}}{K}\right)}\right] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see *On-Time One-Shot*), $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V+_{(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{OUT} = 1.4V

f_{SW} = 600kHz

K = 1.8µs; worst-case K = 1.58µs

$t_{OFF(MIN)}$ = 500ns

$V_{DROP1} = V_{DROP2}$ = 100mV

$$V_{IN(MIN)} = \left[\frac{1.4V + 100mV}{1-(0.5\mu s \times 1.5/1.58\mu s)}\right] + 100mV - 100mV = 2.9V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = \left[\frac{1.4V + 100mV}{1-(0.5\mu s \times 1.0/1.58\mu s)}\right] + 100mV - 100mV = 2.2V$$

Therefore, V_{IN} must be greater than 2.2V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 2.9V.

Using Skip Mode During Suspend

For most active CPU modes, the minimum load currents are too high to benefit from pulse-skipping operation, so PWM mode should be used exclusively. Skip mode can, in fact, be a hindrance to properly executing output voltage transitions (see *Forced PWM Mode*). However, processor suspend currents can be low enough to benefit from low-power pulse skipping.

For processors with three-state outputs, SKP/$\overline{SDN}$ and SUS may be directly controlled. If only digital logic is available, SKP/$\overline{SDN}$ and SUS may be controlled with two digital outputs with the circuit shown in Figure 11. In normal operation, SKP/$\overline{SDN}$ remains biased at 2V by the resistive voltage-divider and the MAX1813's internal circuitry. When the circuit goes into suspend mode (SUS high), the pin remains biased at 2V for approximately 200µs before it goes high. This delay causes the MAX1813 to remain in PWM mode long enough to correctly complete the negative output voltage transition to the suspend-state voltage. Thereafter, the MAX1813 will operate with low-quiescent-current SKIP mode. When the circuit returns to normal operation (SUS low), the delay on the SKP/$\overline{SDN}$ does not affect the transition dynamics because the MAX1813 automatically returns to PWM mode and continues to supply current until the output is in regulation. The ON/$\overline{OFF}$ signal overrides both normal forced-PWM operation and suspend mode.

Using the ZMODE Multiplexer

There are many ways to use the versatile ZMODE multiplexer. The preferred method will depend on when and how the VID DAC codes for the various states are determined. If the output voltage codes are fixed at PC board design time, program both codes with a simple combination of pin-strap connections and series resistors (Figure 12). If the output voltage codes are chosen during PC board assembly, both codes can be independently programmed with resistors (Figure 13). This matrix of 10 resistor-footprints can be programmed to all possible logic-mode and impedance-mode code combinations with only 5 resistors.

Often, the CPU pins provide one set of codes that are typically used with pullup resistors to provide the logic mode VID code, and resistors in series with D0–D4 set the impedance-mode code. Since some of the CPU's VID pins may float, the open-circuit pins can present a problem for the ZMODE multiplexer's impedance mode. For impedance mode to work, any pins intended to be low during this mode must appear to be low impedance at least for the 4µs sampling interval.

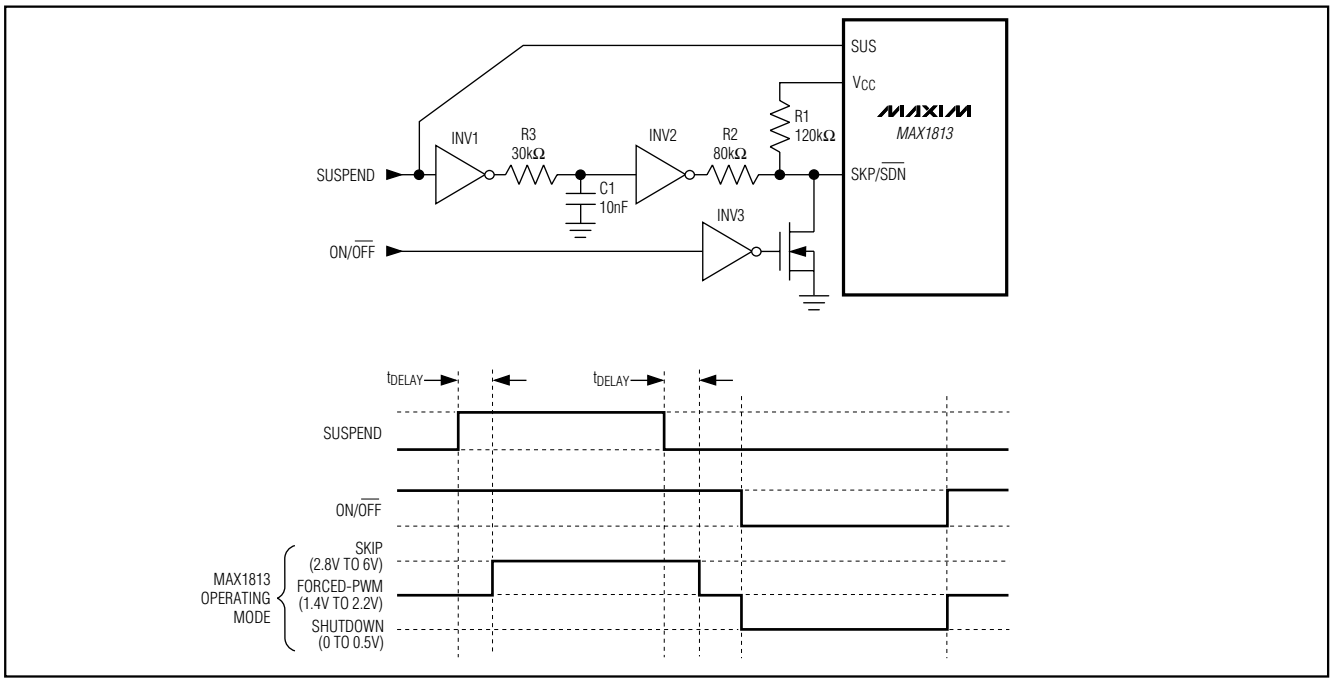

Figure 11. Three-State Operating Mode Control

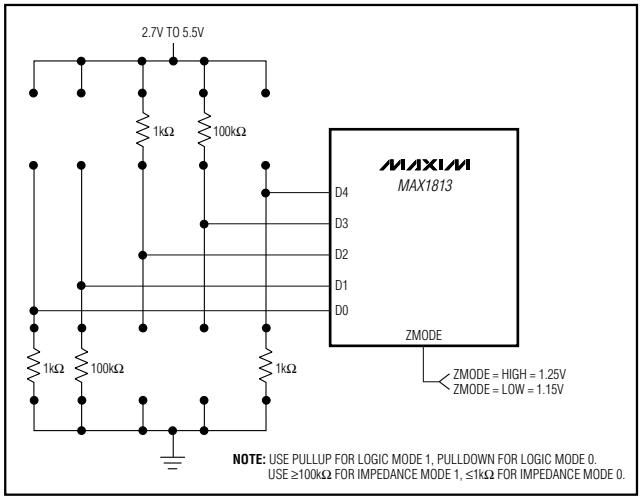

Figure 12. Using the Internal Mux with Hard-Wired Logic-Mode and Impedance-Mode DAC Codes

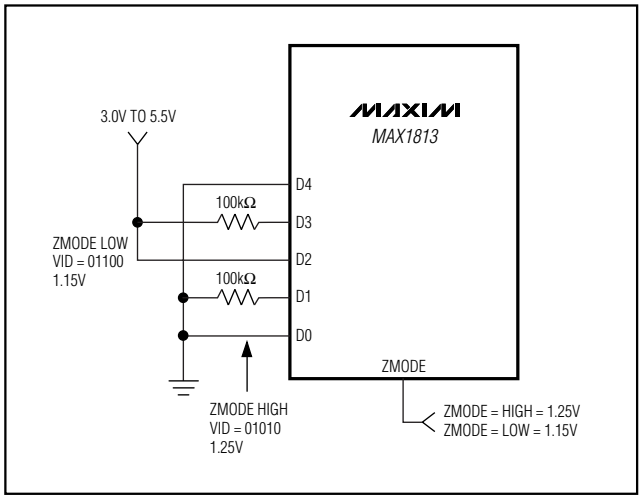

Figure 13. Using the Internal Mux with Both VID Codes Resistor-Programmed

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If the CPU's VID pins float, the open-circuit pins can present a problem for the MAX1813's internal mux. The processor's VID pins can be used for the voltage-mode setting, together with suitable pullup resistors. However, the impedance mode VID code is set with resistors in series with D0–D4, and for the impedance mode to work, any pins intended to be impedance mode logic low must appear to be low impedance, at least for the 4µs sampling interval.

Use one of the two following methods to make the D0-D4 inputs appear low impedance (Figure 14). By using low-impedance pullup resistors with the CPU's VID pins, each pin provides the low impedance needed for the mux to correctly interpret the impedance-mode setting. Unfortunately, the low resistances cause several mA of additional quiescent current for each of the CPU's grounded VID pins. Since D0–D4 need to briefly appear low impedance for sampling, the additional quiescent current may be avoided by using high-impedance pullups that are bypassed with a large enough capacitance to make them appear low impedance for the 4µs sampling interval. As noted in Figure 14, 4.7nF capacitors allow the inputs to appear low impedance even though they are pulled up with 1MΩ resistors.

In some cases, it is desirable to determine the impedance-mode code during system boot so that several processor types can be used without hardware modifications. Figure 15 shows one way to implement this configuration. The desired code is determined by the system BIOS and programmed into one register of the MAX1609 using the SMBus™ serial interface. The MAX1609's other register is left in its power-up state (all outputs high impedance). When $\overline{SMBSUS}$ is low, the outputs are high impedance and do not affect the logic-mode VID code setting. When $\overline{SMBSUS}$ is high, the programmed register is selected, and the MAX1609 forces a low impedance on the appropriate VID input pins. The ZMODE signal is delayed relative to the $\overline{SMBSUS}$ pin because the VID pins that are pulled low by the MAX1609 take significant time to rise when they are released. One additional benefit of using the MAX1609 for this application is that the application uses only five of the MAX1609's high-voltage, open-drain outputs. The other three outputs can be used for other purposes.

Adjusting V_{OUT} with a Resistive-Divider

The output voltage can be adjusted with a resistive-divider rather than the DAC if desired (Figure 16). The drawback is that the on-time doesn't automatically receive correct compensation for changing output voltage levels. This can result in variable switching frequency as the resistor ratio is changed, and/or excessive switching frequency. The equation for adjusting the output voltage is:

$$V_{OUT} = V_{FB}\left(1+\frac{R4}{R5\|R_{INT}}\right)$$

where V_{FB} is the currently selected DAC value, and R_{INT} is the FB input resistance. In resistor-adjusted circuits, the DAC code should be set as close as possible to the actual output voltage to minimize the shift in switching frequency.

Offsetting the Output Voltage

When required, accurate positive and negative output voltage adjustments may be made using external resistors to offset the feedback voltage. Place an offset resistor between the output and FB. The offset voltage may then be controlled by adjusting the current across this offset resistor. For a positive voltage offset, connect a resistor between FB and GND to sink current as shown in Figure 17.

$$V_{OS(POS)} = \left(\frac{R_{FB}}{R\_}\right)V_{OUT(PROG)}$$

For a negative offset voltage, place a resistor between REF and FB to source current as shown in Figure 18.

$$V_{OS(NEG)} = \left(\frac{R_{FB}}{R\_}\right)(V_{OUT(PROG)} - V_{REF})$$

The reference can only support ±40µA of current, so a unity-gain buffer must be used to generate the negative offset reference voltage. Select R_{FB} to be between 50Ω and 500Ω to avoid output voltage regulation error from the FB pin's input current.

Adjusting V_{OUT} Above 2V

The feed-forward circuit that makes the on-time dependent on the input voltage maintains a nearly constant switching frequency as the input voltage (I_{LOAD}) and the DAC code are changed. This works extremely well as long as FB is connected directly to the output. When the output is adjusted with a resistive-divider, the switching frequency is increased by the inverse of the divider ratio.

This change in frequency can be compensated with the addition of a resistive-divider to the battery-sense input (V+). Attach a resistor-divider from the battery voltage

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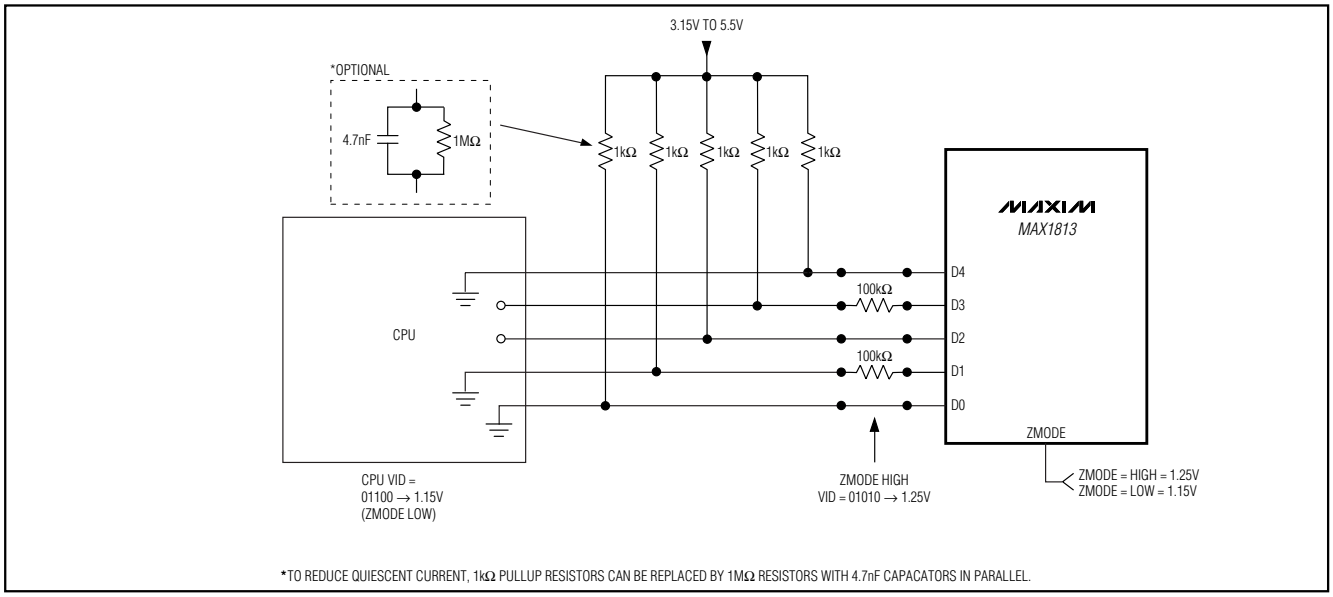

Figure 14. Using the Internal Mux with CPU Driving the Logic-Mode CID Code

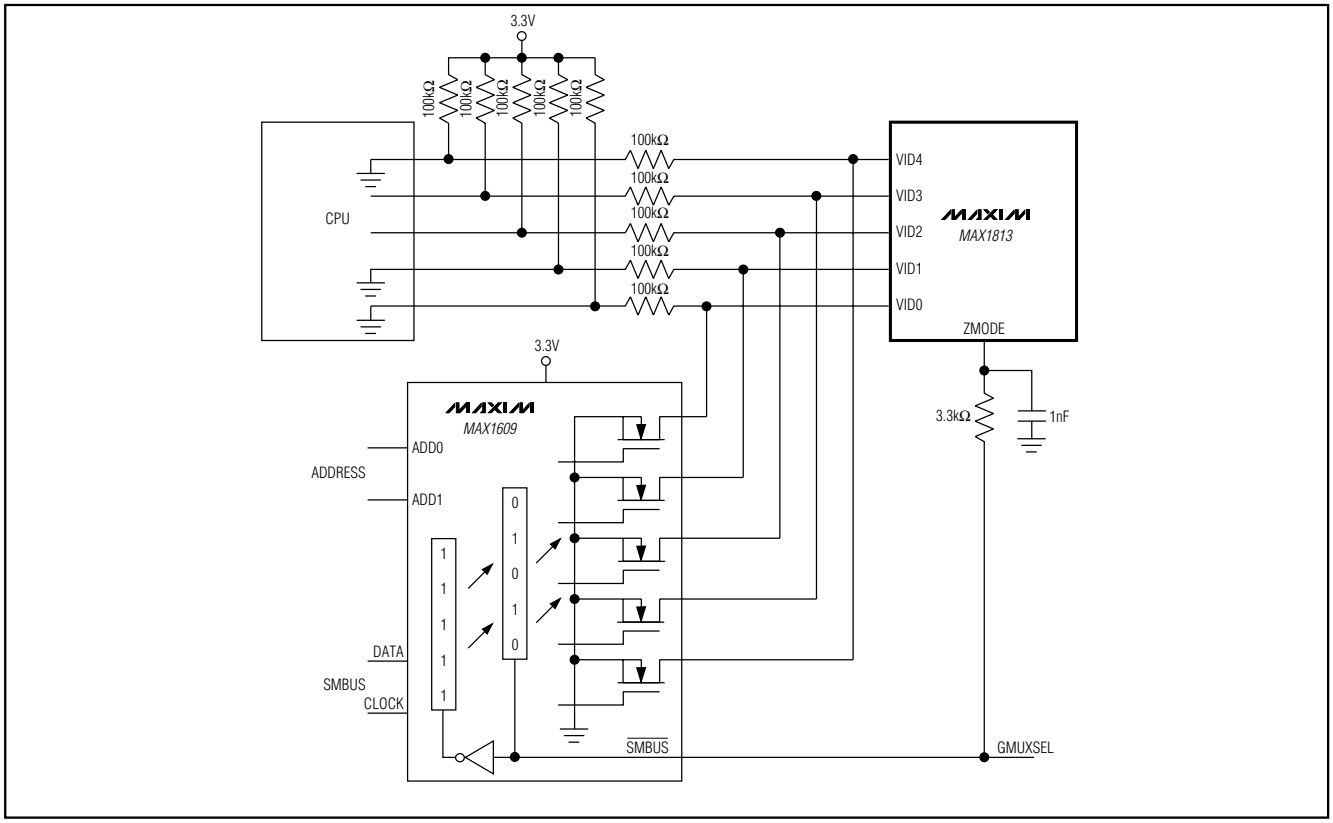

Figure 15. Using the ZMODE Multiplexer

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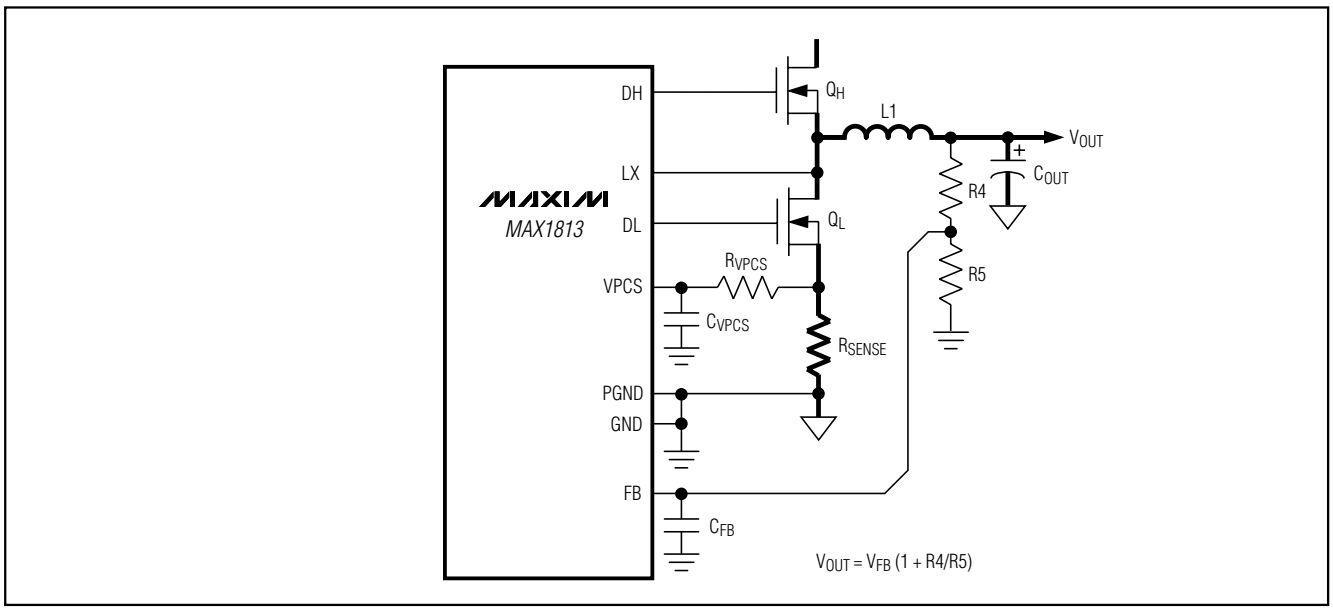


Figure 16. Adjusting V_{OUT} with a Resistive-Divider

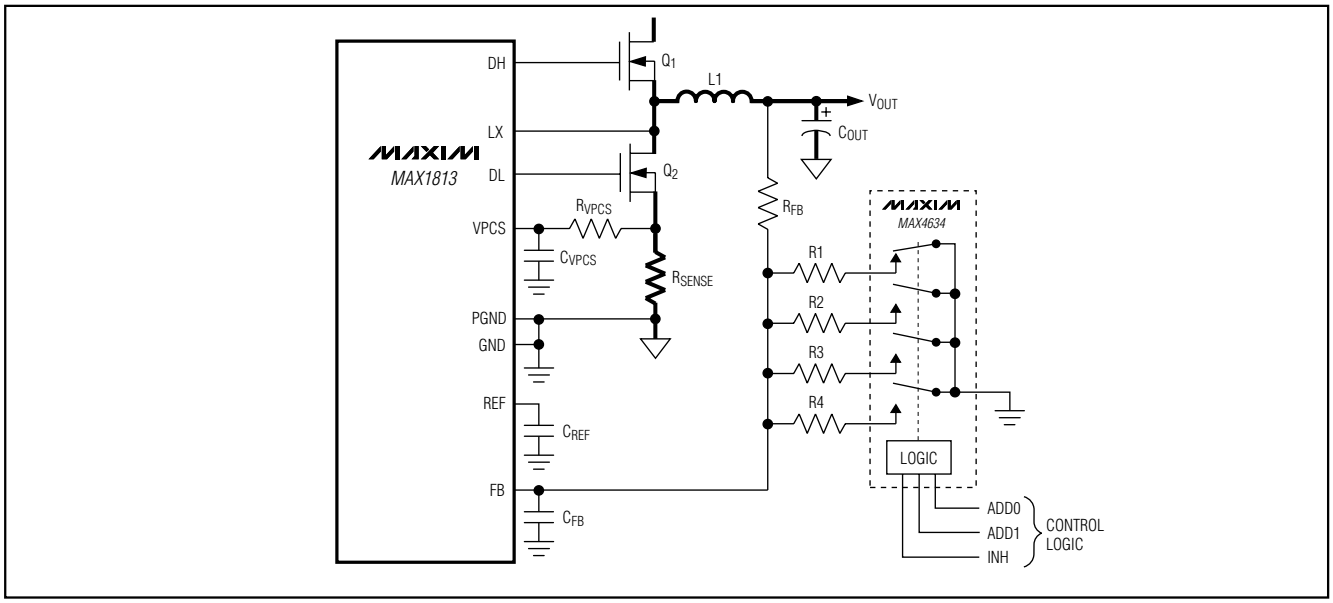


Figure 17. Adding a Positive Offset Voltage

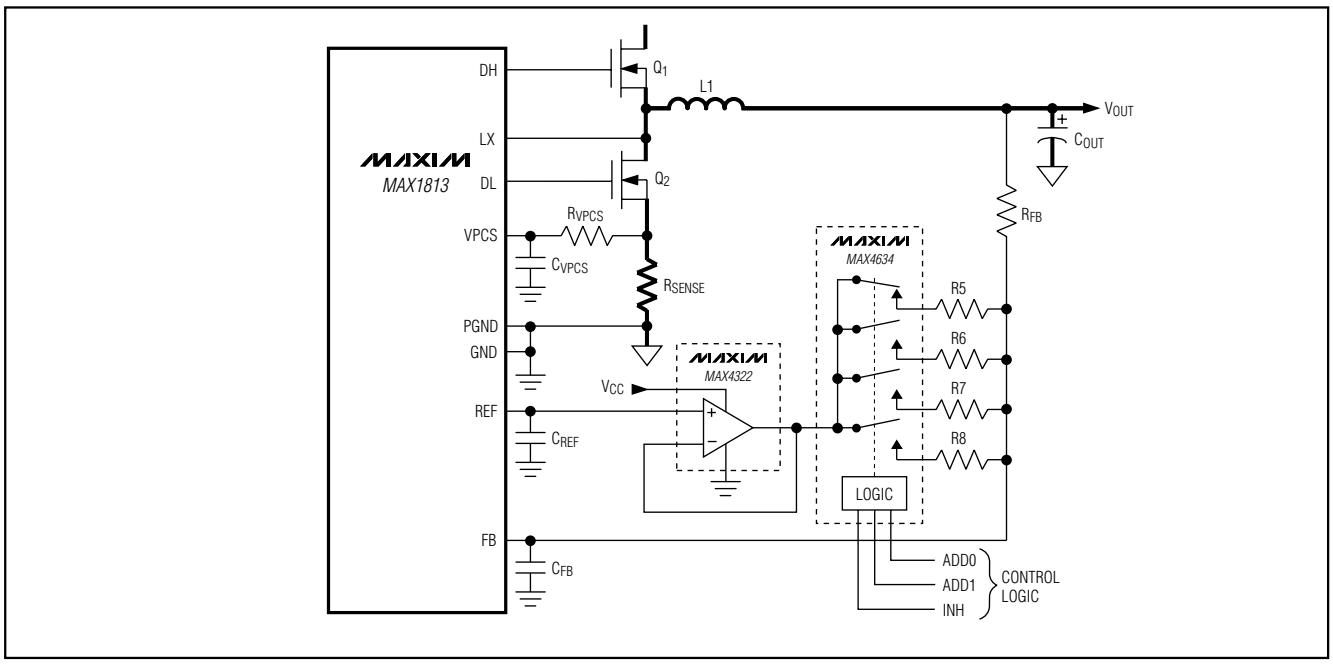


Figure 18. Adding a Negative Offset Voltage

to V+ on the MAX1813, with the same attenuation factor as the output divider. The V+ input has a nominal 600kΩ input impedance, which should be considered when selecting resistor values.

One-Stage (Battery Input) vs. Two-Stage (5V Input) Applications

The MAX1813 can be used with a direct battery connection (one stage) or can obtain power from a regulated 5V supply (two stage). Each approach has advantages, and careful consideration should go into the selection of the final design.

The one-stage approach offers smaller total inductor size and fewer capacitors overall due to the reduced demands on the 5V supply. The transient response of the single stage is better due to the ability to ramp the inductor current faster. The total efficiency of a single stage is better than the two-stage approach.

The two-stage approach allows flexible placement due to smaller circuit size and reduced local power dissipation. The power supply can be placed closer to the CPU for better regulation and lower I^2R losses from PC board traces. Although the two-stage design has slower transient response than the single stage, this can be offset by the use of a voltage-positioned converter.

Ceramic Output Capacitor Applications

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR and are noncombustible, relatively small, and nonpolarized. However, they are also expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies. In addition, their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency) or there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored inductor energy. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The MAX1813 can take advantage of the small size and low ESR of ceramic output capacitors. To ensure stable operation, there must be sufficient resistance in series with the inductor and output capacitor (see "*Output Capacitor Stablility Considerations*").

Output overshoot (V_{SOAR}) determines the minimum output capacitance requirement (see Output Capacitor Selection). Often the switching frequency is increased to 1000kHz or 600kHz, and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 1000kHz is about 5% and

Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

about 2-3% at 600kHz when compared to the 300kHz voltage-positioned circuit, primarily due to the high-side MOSFET switching losses.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 19). If possible, mount all of the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the MAX1813's GND pin. This includes the V_{CC}, REF, and CC capacitors, as well as the resistive-dividers connected to FB and ILIM.
3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) VPCS and GND connections for current limiting and voltage positioning must be made using Kelvin sensed connections to guarantee the current-sense accuracy.
5) When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
6) Ensure the FB connection to the output is short and direct.
7) Route high-speed switching nodes away from sensitive analog areas (CC, REF, ILIM). Make all pin-strap control input connections (SKP/SDN, ILIM, CODE, SUS, ZMODE, etc.) to analog ground or V_{CC} rather than power ground (PGND) or V_{DD}.

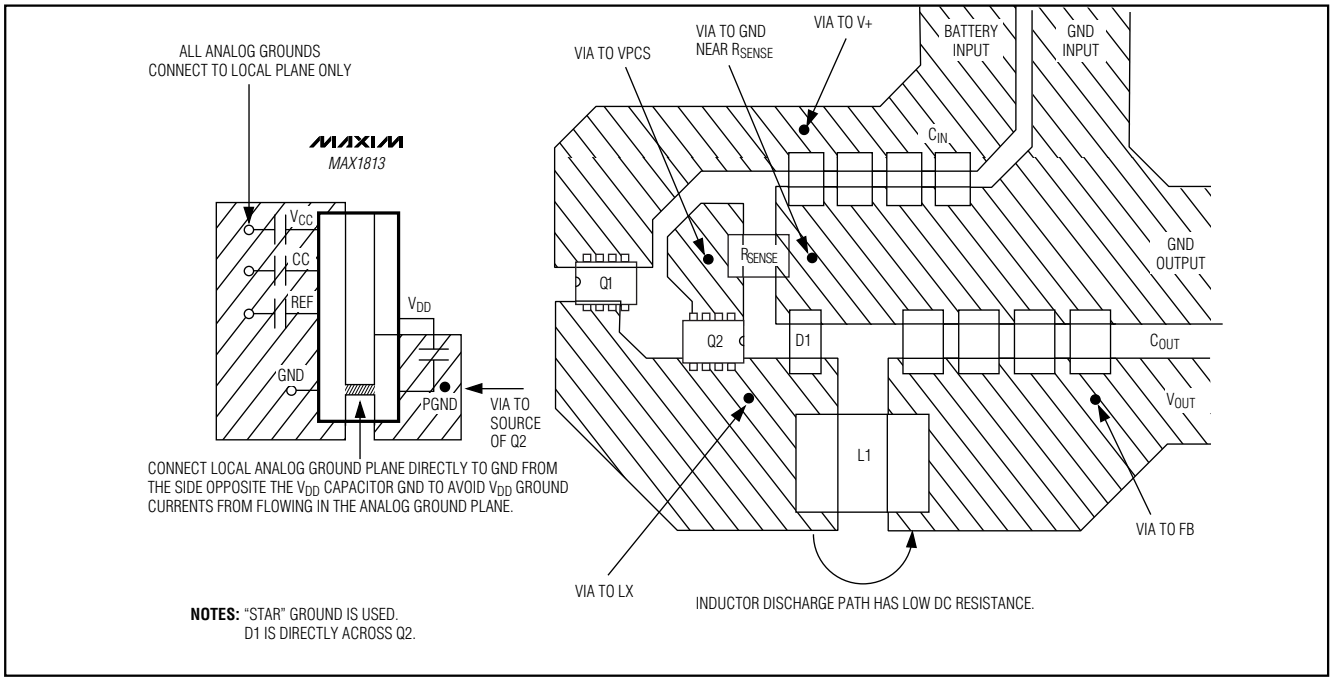


Figure 19. Power-Stage PC Board Layout Example

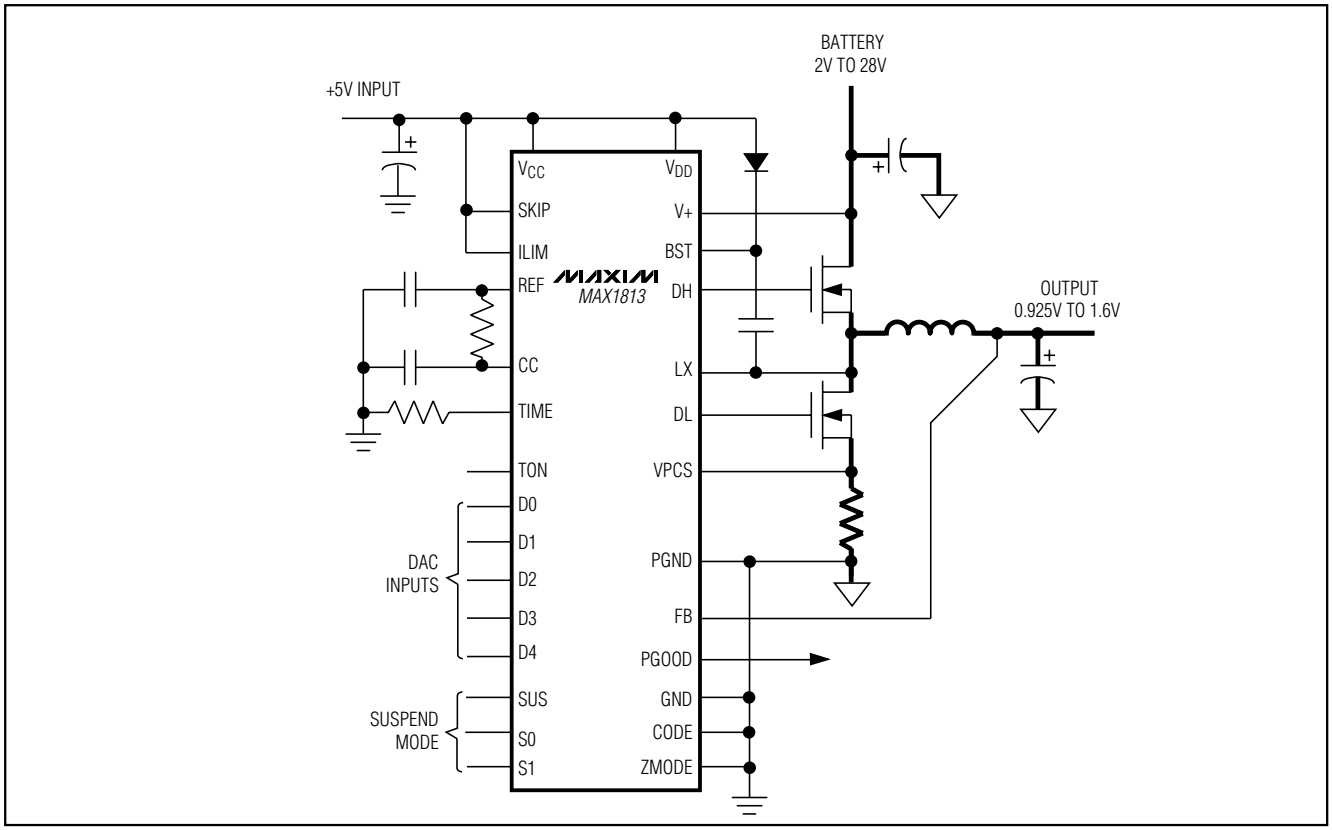
Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate trace must be short and wide (50mils to 100mils wide if the MOSFET is 1 inch from the controller IC).
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 19. This diagram can be viewed as having three separate ground planes: output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; and an analog ground plane where sensitive analog components, the GND pin, and V_{CC} bypass capacitor go. The GND plane and PGND plane must meet only at a single point directly beneath the IC. These two planes are then connected to the high-power output ground with a short connection from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

TRANSISTOR COUNT: 8757

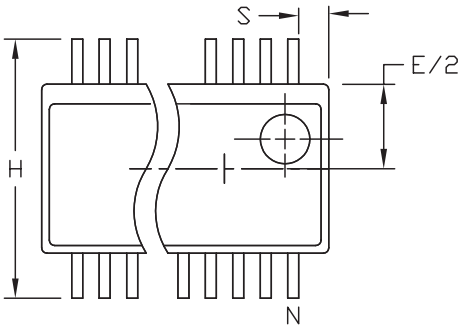
Typical Operating Circuit



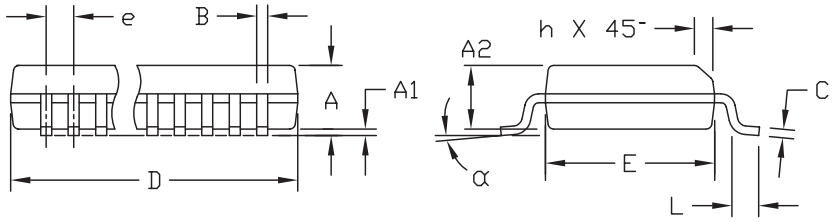
Dynamically-Adjustable, Synchronous Step-Down Controller with Integrated Voltage Positioning

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	D	1/1