# BCM8702
## PRODUCT Brief

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# SERIAL 10-GIGABIT ETHERNET TRANSCEIVER WITH XAUI INTERFACE

## FEATURES

- **IEEE 802.3ae compliant**
- **Support for XENPAK and XGP Standards**
  - Xenpak support optimized for Xenpak/XGP layout and thermal
- **Fully integrated CMU, CDR, and SerDes**
- **PMD interface with serial 10.3125 Gbps CML**
- **PSC 64B/66B scrambler/descrambler**
- **XGXS 8B/10B error detection ENDEC**
- **XAUI link synchronization/deskew**
- **Four-lane, 3.125-Gbps XAUI interface**
- **Loss-of-signal detection**
- **Loopback modes**
- **802.3 clause 45 management interface extended indirect address access**
- **Built-In Self-Test (BIST)**
  - Built-in jitter tests for XAUI and PMD
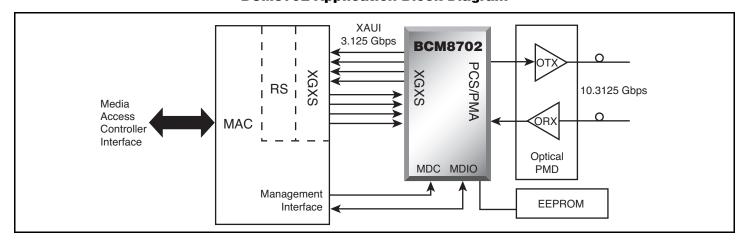- **EEPROM interface support**

## SUMMARY OF BENEFITS

- **Power supplies: core, LVPECL, CML, and XAUI at 1.8V, MDIO at 1.2V, and CMOS at 1.8 or 3.3V.**
- **Low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.**
- **Reduces design cycle and time to market.**
- **Uses the most effective silicon economy of scale for CMOS-based devices.**
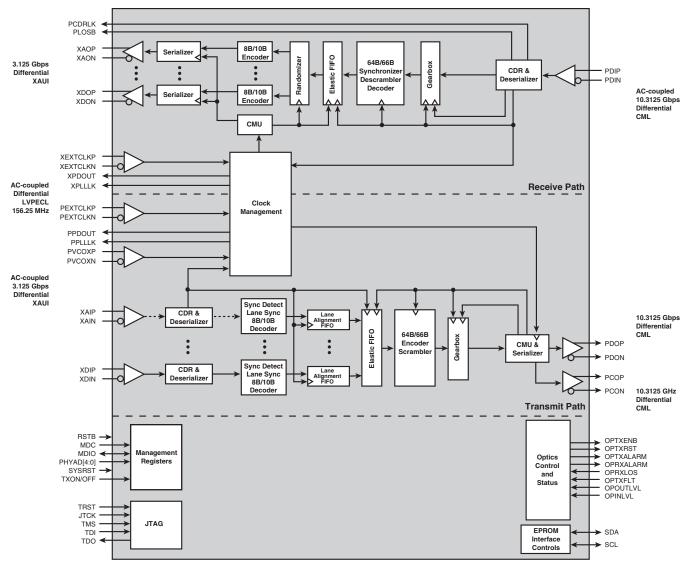
## APPLICATIONS

- **LAN/WAN switches**
- **Switch/router backbones**
- **Hubs and repeaters**
- **Network Interface Cards (NICs)**
- **Test equipment**

## BCM8702 Application Block Diagram

The **BCM8702** Ethernet LAN PHY is a fully integrated serialization/deserialization (10.3125 Gbps) interface device performing the extension functions for a 10.3125 Gbps Serial Ethernet Reconciliation Sublayer (RS) interface. The XGXS, PCS, and PMA functions include 8B/10B coding, 64B/66B coding, SerDes, Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR).

On-chip clock synthesis is performed by the high-frequency, low-jitter, phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing the on-chip VCOs directly to their respective incoming data streams. Elastic buffers allow the XAUI and PMD interfaces to operate in either a synchronous or asynchronous configuration. An external 156.25- MHz VCXO is required for synchronous mode operation or for asynchronous mode with clock cleanup.

The **BCM8702** is packaged in a 19 x 19 x 1.86 mm BGA with a 1-mm ball pitch.

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