TCB8000A

LCD Module Controller Board User Manual

Shenzhen TOPWAY Technology Co., Ltd.

Rev.	Descriptions	Release Date
0.1	Preliminary	2006-07-25
0.2	Typing Correction in 1.1 Product Highlight	2006-11-20

Table of Content

1. Basic Specifications

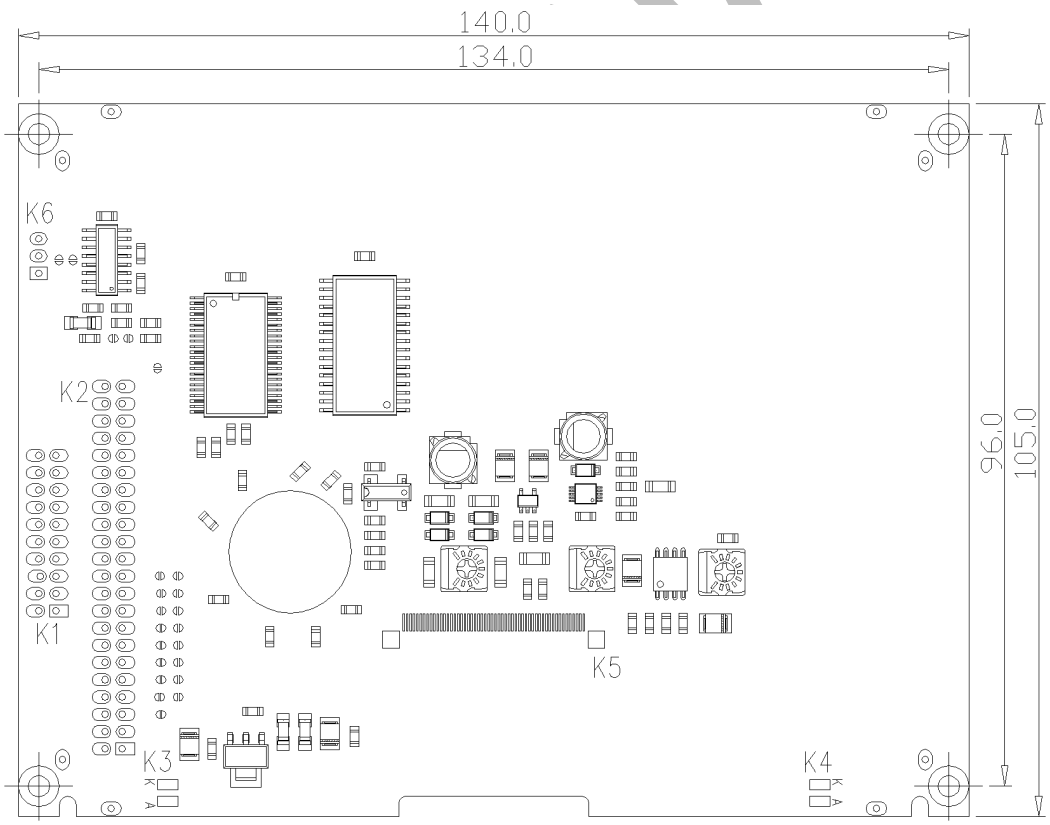
1.1 Product Highlight

1) TCB8000A is a LCD Module Controller Board
2) It could speed up the development of TFT display module
3) Direct interface with LMT057DNAFWU and LMT035DNAFWU TFT LCD module
4) Direct MCU interface, generic 8bit interface or 16bit bus interface
5) With 2D draw function, it could provide fast response even connected with a slow MCU
6) Built in DC-DC converter for LCD supply
7) Built in backlight supply, with software control
8) On board display memory 64k x 16 SRAM
9) Optional RS232 interface of quick start and evaluation
10) Optional font ROM for Chinese Char (GB2123)

1.2 Power and Interface Highlight

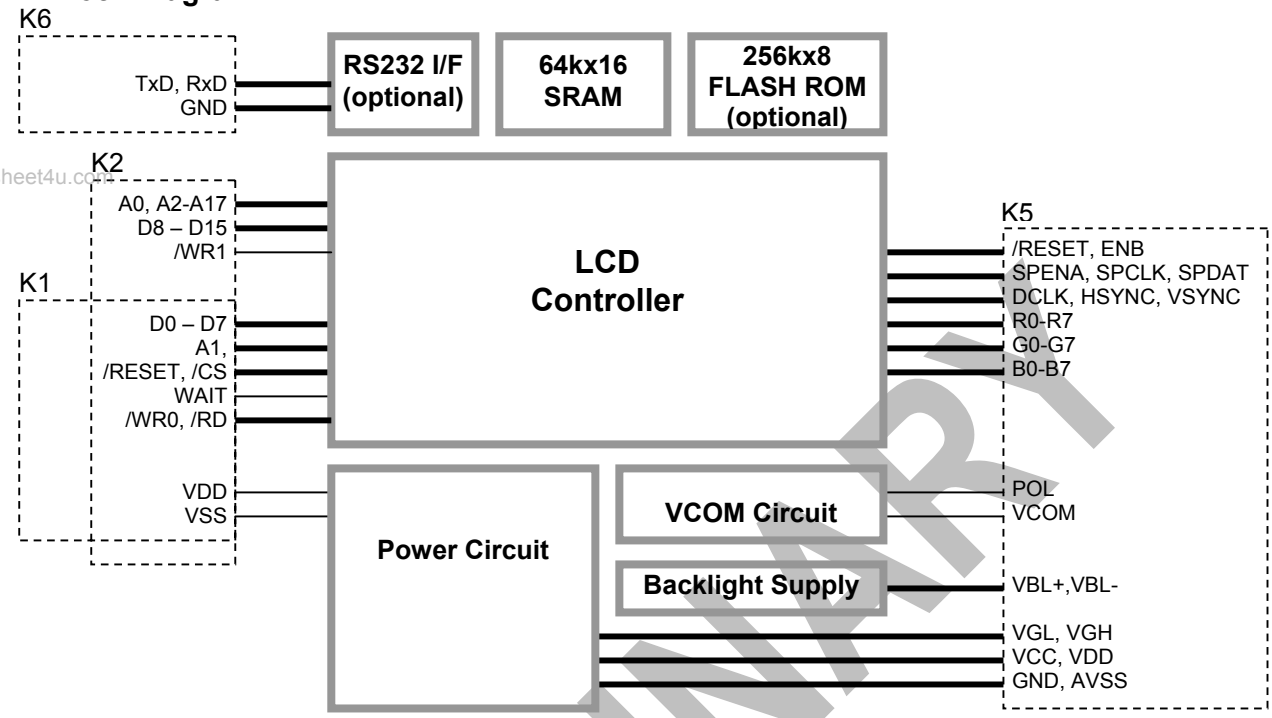
- 5.0V power supply (VDD-VSS)
- 3.3V MCU interface / logic I/O (tolerate to 5.0V logic input)

1.3 Mechanical Specifications



K1 : 20pin IDC connector (P2.54mm) <8bit-data, 1bit-address generic interface, default>
K2 : 44pin IDC connector (P2.54mm) <8/16bit-data, 17bit-address bus interface>
K3,K4: soldering pads <Backlight terminals>
K5 : 54pin FPC connector (P0.5mm) <LCD terminal>
K6: 3pin SIL (P2.54mm) <RS232C terminal>

1.4 Block Diagram



1.5 Terminal Functions

1.5.1 MCU Terminal (K1, 8bit-Data, 1bit-Add)

Pin No.	Pin Name	I/O	Descriptions
1	VSS	Power Input	Power Supply GND (0V)
2			
3	VDD	Power Input	Positive Power Supply
4			
5	A1	Input	Register Select A1=LOW: Accessing Address F004 (command package port) A1=High: Accessing Address F006 (data and status port)
6	/CS	Input	Chip Select Inputs /CS=LOW: Data IO is enabled
7	/RESET	Input	Reset Signal Input /RESET=LOW: Reset /RESET=HIGH: Normal
8	D0	Bi-directional I/O	8-bit bi-directional data bus
:	:		
15	D7		
16	WAIT	Output	Wait Signal
17	/RD	Input	Read enable input, active LOW
18	/WR0	Input	Write enable input, active LOW
19	NC	-	No connection, leave open
20	NC	-	No connection, leave open

Note:
Only one of the MCU Terminal could be used at a time.

1.5.2 MCU Terminal (K2, 8/16bit-Data, 17bit-Add)

Pin No.	Pin Name	I/O	Descriptions
1	VSS	Power Input	Power Supply GND (0V)
2			
3	VDD	Power Input	Positive Power Supply
4			
5	A0	Input	18bit address bus
:	:		
22	A17		
23	/CS	Input	Chip Select Inputs /CS=LOW: Data IO is enabled
24	/RESET	Input	Reset Signal Input /RESET=LOW: Reset /RESET=HIGH: Normal
25	D0	Bi-directional I/O	8-bit or 16-bit bi-directional data bus
:	:		
32	D7		
33	D8		
:	:		
40	D15		
41	WAIT	Output	Wait Signal
42	/RD	Input	Read enable input, active LOW
43	/WR0	Input	Write enable input (for Low byte), active LOW
44	/WR1	Input	Write enable input (for High byte), active LOW

Note:
Only one of the MCU Terminal could be used at a time.

1.5.3 Backlight Terminal (K3, K4)

Pin No.	Pin Name	I/O	Descriptions
-	A	Power Output	Positive backlight driving output
-	K	Power Output	Negative backlight driving output

1.5.4 RS232 Terminal (K6)

Pin No.	Pin Name	I/O	Descriptions
1	Tx	Output	Data Output (to pin2 of PC RS232C<9pin D-connector>)
2	Rx	Input	Data Input (to pin3 of PC RS232C<9pin D-connector>)
3	GND	Power	Power and Signal ground (to pin5 of PC RS232C<9pin D-connector>)

1.5.5 LCD Module Interface (K5, for LMT057DNAFWU or LMT035DNAFWU)

Pin No.	Pin Name	I/O	Descriptions
1	VBL-	Power	Positive Backlight Power Output
2			
3	BVL+	Power	Negative Backlight Power Output
4			
5	NC	-	No connection
6			
7	POL	Input	Signal input for generating VCOM signal
8	/RESET	Output	Reset signal
9	SPENA	Output	Serial enable signal
10	SPCLK	Output	Serial clock signal
11	SPDAT	Output	Serial data signal
12	B0	Output	Blue data signal
:	:		
19	B7		
20	G0	Output	Green data signal
:	:		
27	G7		
28	R0	Output	Red data signal
:	:		
35	R7		
36	HSYNC	Output	Horizontal Sync signal
37	VSYNC	Output	Vertical Sync signal
38	DCLK	Output	Data Clock signal
39	VDD	Power	5.0V power supply
40			
41	VCC	Power	3.3V power supply
42			
43	NC	-	No connection
44			
45	VGL	Power	-10V power supply
46	NC	-	No connection
47	VGH	Power	+16V power supply
48	NC	-	No connection
:			
50			
51	VCOM	Output	VCOM signal output
52	ENB	Output	Enable output
53	GND	Power	GND, 0V, supply
54	AVSS	Power	GND, 0V, supply

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	5.5	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	5.5	V	V_{SS} = 0V
Operating Temperature	T_{OP}	0	50	°C	No Condensation
Storage Temperature	T_{ST}	-10	60	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics (MCU terminal)

V_{SS}=0V, V_{DD} =5.0V, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	4.8	5.0	5.2	V	VDD
Input High Voltage	V_{IH}	3.0	-	VDD	V	Input pins, Bi-direction pins
Input Low Voltage	V_{IL}	VSS	-	0.6	V	Input pins, Bi-direction pins
Output High Voltage	V_{OH}	2.6	-	-	V	Bi-direction pins (*1)
Output Low Voltage	V_{OL}	-	-	0.6	V	Bi-direction pins (*2)
Operating Current	I_{DD}	-	TBD	TBD	mA	VDD

Note:
*1. I_{OH}=-3.0mA
*2. I_{OL}= 3.0mA

3.2 AC Characteristics

Please refer to LCD controller datasheet for details.

4. Function Specifications

4.1 Hard-wired Setting

The following is the list of Jumpers on TCB8000A:

Note: Never try to change the reserved jumper. It may damage the system

Interface Mode	interface terminal	JP1	JP2	JP3	JP4, JP5	JP7~ JP23	JP24	JP25	Note
8bit-data 1bit-address	K1	OPEN	CLOSE	CLOSE	OPEN	CLOSE	OPEN	OPEN	Default setting
8bit-data 17bit-address	K2	OPEN	OPEN	CLOSE	OPEN	OPEN	CLOSE	OPEN	
16bit-data 17bit-address	K2	OPEN	OPEN	CLOSE	OPEN	OPEN	CLOSE	OPEN	
RS232C interface	K6	CLOSE	CLOSE	OPEN	OPEN	CLOSE	OPEN	CLOSE	

4.2 VR setting

P1, P2 adjust the VCOM signal on K5 (LCD terminal).
Check point: C12-positive terminal to GND

P3 adjust the VGL, –10V, output on K5 (LCD terminal).
Check-point: C15-negative terminal to GND

Note.

- It should adjust the VGL output before connect the LCD module.
- As VCOM signal generated by POL signal form LCD module, it must connect the LCD module for the adjustment.

4.3 Command Packet Format

All commands are organized in packet with a 1 byte “Opcode” followed by optional parameters / data up to 64 bytes.

4.3.1 Command Packet Format

Opcode (1 byte)	Parameters / Data (up to 64 bytes)

4.3.2 Opcode Group

00 - 0F Reserved for Serial Communication
10 - 1F 2D Hardware-acceleration: Fonts Drawing Operations
20 - 2F 2D Hardware-acceleration: Geometric Drawing Operations
30 - 3F Audio Operations
40 - 4F Reserved
50 - 5F Reserved
60 - 6F Communication
70 - 7F Reserved
80 - 8F System Control
F0 – FF Reserved for serial mode synchronization

4.3.3 Opcode Description

Opcode (HEX)	Operations	Parameters / Data
00	Set “Control & Status Port” of the Command Interpreter	The value of this data (one byte) will be directly written to the Control & Status register.
10	charset_config	Character Set (1 byte): 00: Built in 8x8 ASCII 01: 8x8 CGRAM (Embedded RAM) 02: 8x16 CGRAM (Embedded RAM) 03: 16x16 CGRAM (Embedded RAM) 04: 16x16 GB2312-80 (External ROM) 05: 16x16 BIG5 (External ROM) 06: 8x8 Custom 8-bit encoding (External ROM) 07: 8x8 Custom 16-bit encoding (External ROM)
12	set_print_coord	Character Print Coordinates (4 bytes) - x (2 bytes) - y (2 bytes) For Mono LCD, x = (multiple of 8) – 1 For Color LCD, no restriction on the value of x coordinate
14	set_font_fgcolor	Character Foreground Color (2 bytes) (same as td_fgcolor, with opcode = (20 HEX)) Mono LCD: 1bpp, 2bpp, 4bpp Color LCD: 16-bit TFT (5R:6G:5B) 12-bit STN (4R:4G:4B)
15	set_font_bgcolor	Character Background Color (2 bytes) Mono LCD: 1bpp, 2bpp, 4bpp Color LCD: 16-bit TFT (5R:6G:5B) 12-bit STN (4R:4G:4B)
16	show_char	Display Character (1 or 2 bytes)
17	show_string	Display String - Character count (1 byte) (0 ≤ character count ≤ 63) - String (≤ 63 bytes)

Opcode (HEX)	Operations	Parameters / Data
20	td_fgcolor	Set Foreground Color (2 bytes) Mono LCD: 1bpp, 2bpp, 4bpp Color LCD: 16-bit TFT (5R:6G:5B) 12-bit STN (4R:4G:4B)
23	draw_pixel	Draw Pixel - x (2 bytes) - y (2 bytes)
24	draw_line	Draw Line - x_start (2 bytes) - y_start (2 bytes) - x_end (2 bytes) - y_end (2 bytes)
26	draw_rect	Draw Hollow Rectangle (Box) - x_start (2 bytes) - y_start (2 bytes) - x_end (2 bytes) - y_end (2 bytes)
27	fill_rect	Fill Rectangle (Box) - x_start (2 bytes) - y_start (2 bytes) - x_end (2 bytes) - y_end (2 bytes)
28	draw_circle	Draw Circle - x_center (2 bytes) - y_center (2 bytes) - radius (1 byte)
29	fill_circle	Fill Circle - x_center (2 bytes) - y_center (2 bytes) - radius (1 byte)
60	set_baud	Set baud rate - divisor (lower byte) (1 byte) - divisor (upper byte) (1 byte)
80	refresh_setting	N/A
81	set_mem_ptr	Set memory pointer - address (3 bytes)
82	read_reg	Read register - address (2 bytes) ONLY used in RS232 serial host mode
83	write_reg	Write register - address (2 bytes) - data (1 byte)
84	write_mem	Write memory - count (1 byte) - data (up to 63 bytes)
8F	mem_clk_en	Enable memory clock “69 45 61 67 6C 65” (6 bytes in HEX)

4.3.4 Registers Table

Register (HEX)	R/W	Reset Value	Descriptions
F000	Read Write	1000 0000	Chip ID Port Always read back 80 (HEX) Write “DE FC 0B” (HEX) to enable memory clock, same as command with OPCODE “8F”.
F001	Read only	0000 0000	Chip Revision Port Always read back 00 (HEX) for iEM8000
F004	Write only	-	Command Packet Port - Writing of Command Packets.
F006	 Write Read	 Don’t Care Bit[4] = 1 Don’t Care Bit[0] = 0 Don’t Care Bit[0] = 0	Port for writing control or reading status Bit[7:5]: Reserved Bit[4] : DISPLAY ON / OFF 0 : DISPLAY ON 1 : DISPLAY OFF Bit[3:1] : Reserved Bit[0] : End of Command Write “1” after each command packet Bit[7:1] : Reserved Bit[0] : FIFO full Read “1” if Command FIFO is full. Hosts must read this bit = “0” before writing to Command Packet Port.
F080	Read / Write	0000 0000	Bit[7:6] : External SRAM Select Bit[7:6] = 11: Required setting - 64Kx16 external SRAM connected Bit[5] : Horizontal TFT Pulse Polarity 0: Active low 1: Active high Bit[4] : Vertical TFT Pulse Polarity 0: Active low 1: Active high Bit[3] : STN Panel I/F Data Width 0: 4-bit single 1: 8-bit single Bit[2] : Color Mode Select 0: Monochrome 1: Color Bit[1:0] : Color Depth Select If Monochrome (Bit[2] = 0) 00: 1 bit-per-pixel 01: 2 bit-per-pixel 10: 4 bit-per-pixel 11: Reserved If Color (Bit[2] = 1) 00: 16 bit-per-pixel (TFT panel) 01: 12 bit-per-pixel (CSTN panel) 10: Reserved 11: Reserved
F081	Read / Write	000 0000	Bit[7] : Reserved Bit[6:0] : Panel Horizontal Character Count – 1, Panel Horizontal Character Count[8:0] supports horizontal panel size up to 128 characters or 1024 pixels.
F082	Read / Write	0000 0000	Bit[7:0] : Panel Line Count - 1 bit[7:0]
F083	Read / Write	0	Bit[7:1] : Reserved Bit[0] : Panel Line Count – 1 bit[8], Panel Line Count[8:0] supports vertical panel size up to 512 lines.
F084	Read / Write	0000 0000	Bit[7:0] : Display Start Position X Coordinate – 1 bit[7:0]
F085	Read / Write	00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position X Coordinate – 1 bit[9:8]

Register (HEX)	R/W	Reset Value	Descriptions
F086	Read / Write	0000 0000	Bit[7:0] Display Start Position Y Coordinate – 1 bit[7:0]
F087	Read / Write	00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position Y Coordinate – 1 bit[9:8] Display Start Position (X,Y) is for panning of the view port on a virtual display.
F088	Read / Write	0000 0000	LCD_LUT1 Bit[7:4] : for Gray level 3 Bit[3:0] : for Gray level 2
F089	Read / Write	0000 0000	LCD_LUT0 Bit[7:4] : for Gray level 1 Bit[3:0] : for Gray level 0
F08A	Read / Write	000 0000	Bit[7] : Reserved Bit[6:0] : Virtual Display Character count – 1 It supports horizontal virtual size up to 128 characters or 1024 pixels.
F08B	Read / Write	00 0000	Bit[7:6] : Reserved Bit[5:0] : WF count for STN panels 000000: WF pin toggles every frame 000001: WF pin toggles every 2 LP pulses 000010: WF pin toggles every 3 LP pulses …… …… 111111: WF pin toggles every 64 LP pulses
F08C	Read / Write	0000	Bit[7:4] : Reserved Bit[3:0] : Horizontal non-display period 0000: 2 characters (16 pixels) 0001: 3 characters (24 pixels) …… …….. 1111: 17 characters (136 pixels)
F08D	Read / Write	0000	Bit[7:4] : Reserved Bit[3:0] : Vertical non-display period 0000: 1 line 0001: 2 lines ……... …… 1111: 16 lines
F08E	Read / Write	0000 000	Bit[7:4] : Pixel Clock Divider 0000: 24 MHz (divided by 1) 0001: 12 MHz (divided by 2) 0010: 8 MHz (divided by 3) 0011: 6MHz (divided by 4) …… …… 1111: 1.5MHz (divided by 16) Bit[3] : Display Blank 0: Normal 1: Blank Bit[2] : Display Invert 0: Normal 1: Invert Bit[1] : LCD_ON Polarity 0: LCD_ON pin active low 1: LCD_ON pin active high Bit[0] : Reserved

Register (HEX)	R/W	Reset Value	Descriptions
F08F	Read / Write	000 0000	Bit[7] : Reserved Bit[6:0] : Number of frames to start – 1 Maximum 128 frames (see section 2.15.1 for detail)
F090	Read / Write	00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Front Porch for TFT panels 000000: 1 pixel 000001: 2 pixels ……... …….. 111111: 64 pixels
F091	Read / Write	00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Back Porch for TFT panels 000000: 1 pixel 000001: 2 pixels ……... …….. 111111: 64 pixels
F092	Read / Write	0 0000	Bit[7:5] : Reserved Bit[4:0] : Horizontal Pulse Width for TFT panels 00000: 1 pixel 00001: 2 pixels ……... …….. 11111: 32 pixels
F093	Read / Write	0000 0000	Bit[7:0] : Scratch Pad register
F094	Read / Write	00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Front Porch for TFT panels 000000: 1 line 000001: 2 lines ……... …….. 111111: 64 lines
F095	Read / Write	00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Back Porch for TFT panels 000000: 1 line 000001: 2 lines ……... …….. 111111: 64 lines
F096	Read / Write	0 0000	Bit[7:5] : Reserved Bit[4:0] : Vertical Pulse Width for TFT panels 00000: 1 line 00001: 2 lines ……... …….. 11111: 32 lines

Register (HEX)	R/W	Reset Value	Descriptions
F100	Read / Write	Bit[7:6] = 00 Bit[1:0] = 00	Bit[7] – Enable / Disable 0: Disable Sprite 1: Enable Sprite Bit[6] – Transparency 0: Transparency disable 1: Transparency enable When enabled: Sprite data = 00 becomes transparent and LCD background will be displayed instead. Bit[5:2] – Reserved Bit[1:0] – Sprite Modes Select 01: Sprite with 2 bit-per-pixel 00, 10, 11: Reserved
F102	Read / Write	0000 0000	Bit[7:0] - SP_LUT0L[7:0]
F103	Read / Write	0000 0000	Bit[7:0] - SP_LUT0H[7:0]
F104	Read / Write	0000 0000	Bit[7:0] - SP_LUT1L[7:0]
F105	Read / Write	0000 0000	Bit[7:0] - SP_LUT1H[7:0]
F106	Read / Write	0000 0000	Bit[7:0] - SP_LUT2L[7:0]
F107	Read / Write	0000 0000	Bit[7:0] - SP_LUT2H[7:0]
F108	Read / Write	0000 0000	Bit[7:0] - SP_LUT3L[7:0]
F109	Read / Write	0000 0000	Bit[7:0] - SP_LUT3H[7:0]
F10A	Read / Write	0000 0000	Bit[7:0] – Sprite Horizontal Pixel Count – 1 Maximum 256 pixels
F10B	Read / Write	0000 0000	Bit[7:0] – Sprite Vertical Line Count – 1 Maximum 256 lines
F10C	Read / Write	0000 0000	Bit[7:0] – Sprite Horizontal Start Position bit[7:0]
F10D	Read / Write	00	Bit[7:2] – Reserved Bit[1:0] - Sprite Horizontal Start Position bit[9:8] Sprite Horizontal Start Position bit[9:0] is measured in pixels and counted from left to right of the edge of the panel display (i.e. not virtual display).
F10E	Read / Write	0000 0000	Bit[7:0] – Sprite Vertical Start Position bit[7:0]
F10F	Read / Write	0	Bit[7:1] – Reserved Bit[0] - Sprite Vertical Start Position bit[8] Sprite Vertical Start Position bit[8:0] is measured in lines and counted from top to bottom of the edge of the panel display (i.e. not virtual display).
F142	Write Only	0000 0000	Bit[7:0] – Sprite / overlay storage starting address bit[7:0]
F143	Write Only	0000 0000	Bit[7:0] – Sprite / overlay storage starting address bit[15:8]
F144	Write Only	0000 0000	Bit[7:2] – Reserved Bit[1:0] – Sprite / overlay storage starting address bit[17:16] This is the starting address to put the sprite/overlay image
F180	Read Only	0000 0000	Bit[7:0] – Background Color bit[7:0]
F181	Read Only	0000 0000	Bit[7:0] –Background Color bit[15:8]
F182	Read Only	0000 0000	Bit[7:0] – Foreground Color bit[7:0]
F183	Read Only	0000 0000	Bit[7:0] –Foreground Color bit[15:8]

Register (HEX)	R/W	Reset Value	Descriptions
F500	Read / Write	Bit[7:4] = 1110 Bit[3:0] = 1110	CS0 Configuration Port – Pulse Width Bit[7:4] : Write Cycle Pulse Width 0000: 1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks ……. 1110:15 memory clocks 1111: Reserved Bit[3:0] : Read Cycle Pulse Width 0000: 1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks ……. 1110:15 memory clocks 1111: Reserved
F501	Read / Write	0000 0000	CS0 Configuration Port – Control Bit[7] : Enable bit 0:Disable CS0 1:Enable CS0 Bit[6] : Memory data bus width 0: 8-bit memory data bus width 1: 16-bit memory data bus width Bit[5] : 16-bit SRAM option 0:two 8-bit SRAMs 1:one 16-bit SRAM Bit[4] : Reserved Bit[3] : CS0 assertion time relative to address assertion. 0:CS0 and address assert at the same time 1:CS0 lags address by 1 memory clock. Bit[2] : CS0 Negation Timing 0:CS0 and Address negate at the same time 1:CS0 leads Address by 1 memory clock in write access. Bit[1] : Write Enable Assertion Time 0: Write Enable and Address Assert at the same time. 1: Write Enable lags Address by 1 memory clock. Bit[0] : Write Enable Negation Time 0: Write Enable and Address negate at the same time. 1: Write Enable leads Address by 1 memory clock.
F504	Read / Write	Bit[3:0] = 1110	CS1 Configuration Port – Pulse Width Bit[7:4] : Reserved Bit[3:0] : Read Cycle Pulse Width 0000: 1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks 0001: 3 memory clocks …… 1101:14 memory clocks 1110:15 memory clocks 1111: Reserved
F505	Read / Write	0000 0000	CS1 Configuration Port – Control Bit[7] : Enable bit 0:Disable CS1 1:Enable CS1 Bit[6] : Memory data bus width 0: 8-bit memory data bus width 1: 16-bit memory data bus width Bit[5] : Reserved Bit[4] : Reserved Bit[3] : CS1 assertion time relative to address assertion. 0:CS1 and Address assert at the same time 1:CS1 lags Address by 1 memory clock. Bit[2] : CS1 Negation Timing 0:CS1 and Address negate at the same time 1:CS1 leads Address by 1 memory clock in write access. Bit[1:0] : Reserved
F6C4	Read / Write	Bit[5:0] = 11 0011	Set Memory Clock Divide Bit[7:6] = Reserved Bit[5:0] = 010000 to set 24MHz memory clock for proper operations

5. Design and Handling Precaution

1. Any mechanical shock (eg. dropping form high place) will damage the device.
2. Do not add excessive force on the device.
3. Never attempt to disassemble or rework the device.
4. When mounting the device, make sure that it is free form twisting, warping and distortion.
5. Only hold the device by its side.
6. Never add force to component of the device. It may cause invisible damage or degrade of the reliability.
7. This could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect it.
8. Take care and prevent get hurt by the device sharp edge.
9. Never operate the device exceed the absolute maximum ratings.
10. Keep the signal line as short as possible to prevent noisy signal applying to the device.
11. Never apply signal to the device without power supply.
12. Device reliability may be reduced by temperature shock.
13. When storing the device, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature.