Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC

Getting high efficiency from low-power off-line power supplies has always posed difficulties for the design engineer. Power hungry control circuits require either line frequency transformers for bias or bleeder circuits for start-up. The problem with the bleeder approach is that, to date, no provisions have been made in PWM ICs to turn off the bleeder; so several watts of power get consumed during normal operation — serving no purpose but to heat the bleed resistor. While solutions are available, they all require additional parts, which increase costs and use precious circuit board real estate.

The Si9120 from Siliconix was designed to address these problems. This current-mode control, pulse-width modulator IC is implemented with combined BiC/DMOS technology. All logic functions are implemented in CMOS to reduce the typical quiescent power requirements to 0.85 mA while driving a 500-pF load at 50 kHz. Included on chip is a 450-V DMOS, depletion-mode transistor configured as a linear voltage regulator to supply operating power to the chip directly from the rectified 115-V mains. The chip contains MOS capacitors for the clock circuit, so the only external timing component required is a resistor to set the operating frequency. Other features include a temperature-compensated buried Zener reference for less than 0.2 mV/$^\circ$C drift; a latchable shutdown feature; and a dual current-limit comparator, which minimizes false tripping due to leading-edge current spikes. A major advantage of CMOS processing is speed—current-limit delays are typically under 100 ns while supply current is kept at less than 1 mA. This allows reliable operation up to 500 kHz.

FUNCTIONAL DESCRIPTION

Pre-regulator

A BiC/DMOS power integrated circuit process is used to integrate a high-voltage (450-V rated) lateral DMOS transistor with the CMOS PWM controller. By using an ion implant to shift the gate threshold to a negative value, as shown in Figure 1, the transistor is made to operate as a depletion-mode device. This eliminates the need for a pull-up voltage above V_{CC} to turn
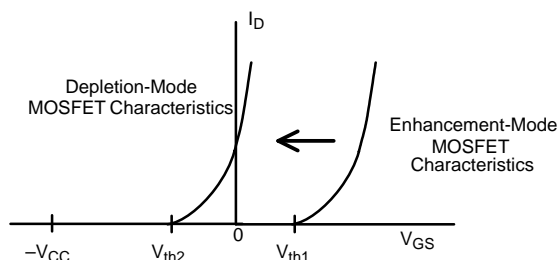
the device on, and an amplifier and voltage reference can be used to implement a linear regulator, as shown in Figure 2. The CMOS circuitry is thus protected from transients which appear on the input power bus.

For some applications it is useful to turn off the pre-regulator after start-up. This is easily accomplished by using an auxiliary winding on the transformer to develop a bootstrap supply voltage. After the converter starts, its own output feeds 10 to 12 V to pin 7 (V_{CC}), and the amplifier pulls the gate of the MOSFET to the $-V_{IN}$ rail. Thus, $V_{GS} = -V_{CC}$, and the device is turned off. For operation of $+V_{IN} > 250$ V, a 10-kΩ, $^1/_4$-W resistor should be placed in series with $+V_{IN}$ (Pin 1). For $+V_{IN} > 380$ V, a 15-kΩ, $^1/_4$-W resistor is recommended. (Reference Figure 10, R13, C22 are also required.)

Oscillator

A ring of inverters and internal MOS capacitors form the oscillator circuit, as shown in Figure 3. This circuit requires only a resistor (no external capacitor) to program the frequency. The internal capacitance is charged towards V_{CC} through R_{OSC}. When the capacitor voltage reaches $V_{CC}/2$ (the CMOS logic threshold), inverter INV1 changes state (from high to low), and the INV2 output goes from a low to a high output. The capacitor, C2, provides positive feedback to ensure stable operation without frequency jitter.

It also causes the "bump" at the end of the ramp until INV2 can turn on the discharge switch, Q1, to terminate the cycle.

Oscillator synchronization is achieved by prematurely terminating each clock cycle using a positive going pulse capacitively coupled onto the oscillator ramp voltage. The pulse forces INV1 to change states, Q1 discharges C = C1 + C2, and the cycle repeats. An internal flip-flop blanks out the output during every other clock cycle, so the switch duty ratio is limited to a maximum of 50%. Therefore, the oscillator frequency and SYNC pulse repetition rate must be set at two times the switching frequency, f_s.
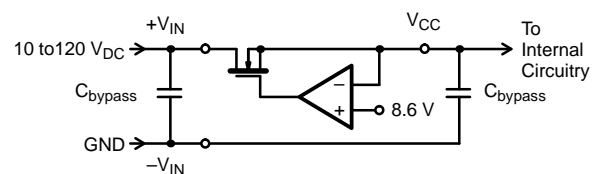

FIGURE 1. Depletion-mode MOSFET Characteristics

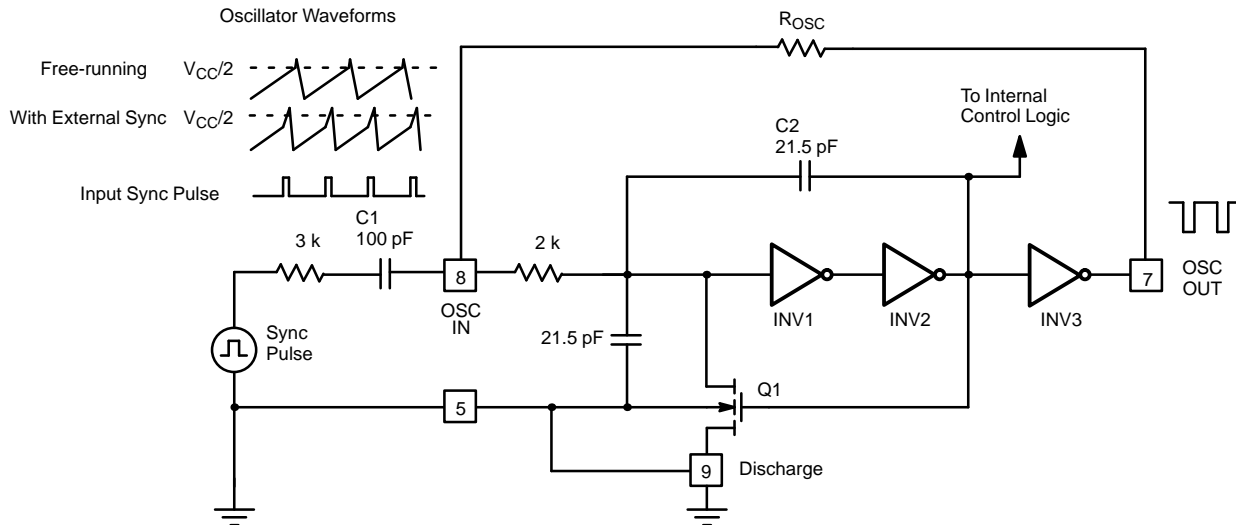**FIGURE 2.** Pre-regulator/Start-up Circuit

FIGURE 3. Si9120 Oscillator Circuit Operation

Error Amplifier

The bias resistor, connected from pin 16 (bias) to pin 6 ($-V_{IN}$), programs the current sources in the analog portion of the current-mode controller — including the error amplifier, the current-mode and current-limit comparators, and the voltage reference. The Si9120 data sheet guarantees the performance of these functions at one value of bias current—15 μA. It is possible to change the performance characteristics of these functions by changing the bias current. (See Siliconix Application Note AN703 for an explanation of how this is accomplished.)
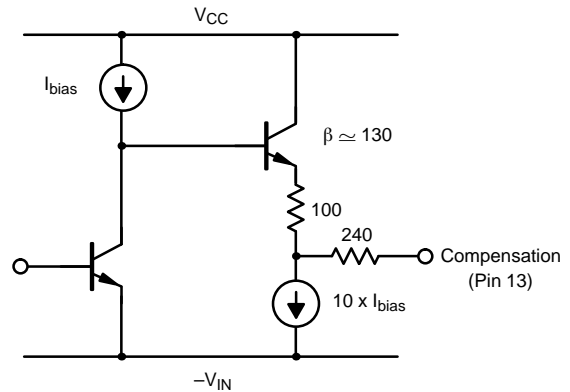
The error amplifier circuit employs PMOS transistors in a differential input stage to achieve a high input impedance of 40 MΩ typically (2-MΩ minimum). This input impedance, combined with a 1-kΩ small-signal output impedance, enables the amplifier to be used with feedback compensation, unlike transconductance error amplifiers. The amplifier can source 2 mA and sink 0.140 mA, as can be seen from the output stage equivalent circuit in Figure 4. Yes, an NPN transistor is used here. Most of the PWM controller is CMOS, but the process allows the flexibility of using bipolar devices where they are advantageous.

FIGURE 4. Error Amplifier Output Stage

The error amplifier is unity gain stable with a typical bandwidth of 1.4 MHz and 70° phase margin. Bias current values from 5 μA to 50 μA have been tested, and the error amplifier does remain stable over this range. Actually, the bandwidth and phase margin increase somewhat as I_{bias} is increased above 15 μA. Higher bias currents may, therefore, be useful when compensating higher frequency converters (above 250 kHz).

Voltage Reference

A buried Zener with merged temperature compensating diode (Patent no. 4766469) is used to achieve stability of 0.2 mV/$^\circ$C.

The Si9120 voltage reference is trimmed to 4 V plus or minus 2% with a bias current of 15 μA. Note that trimming is done with the error amplifier connected for unity gain, so the effect of the offset voltage is removed. The reference voltage varies by about 1% as I_{bias} is varied from 5 to 50 μA. If 2% reference accuracy must be guaranteed, I_{bias} should be set at 15 μA.

Comparators

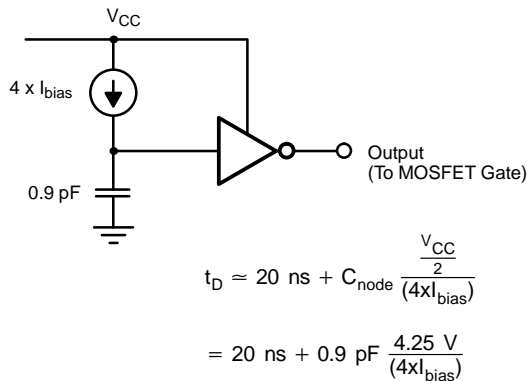The delay time of the current-limit and current-mode comparators can be modeled as a current source charging an internal nodal capacitance, as shown in Figure 5. The current-mode comparator is intentionally made to be four times slower than the current-limit comparator. In many circuits, this permits the elimination of the RC filter in the current-sense circuit, which is used to prevent false trips by the leading edge current spike. After one of the comparator outputs goes high, there is an additional 20 ns of gate propagation delay before the output driver can begin switching. The total current-limit delay to output versus I_{bias} is shown in Figure 6 for V_{CC} equal to 8.5 V. The delay time is 180 ns for I_{bias} = 5 μA, but decreases to 50 ns for I_{bias} = 30 μA. As operating frequency is increased, I_{bias} may be increased to speed up the current limiting and reduce the minimum MOSFET pulse width. As I_{bias} is increased, however, the current-limit trip voltage also increases. Figure 7 shows how the trip voltage is established and how it varies with I_{bias}. The current sense resistor and I_{bias} determine the peak value of switch current. Since this current limiting is very fast, the trip level of current is usually set to be well above the maximum normal operating current (by a factor of 1.5 to 2). This prevents false trips but still protects the MOSFET switch from exceeding its pulse current ratings.

$$t_D \simeq 20 \text{ ns} + C_{node} \frac{\frac{V_{CC}}{2}}{(4 \times I_{bias})}$$

$$= 20 \text{ ns} + 0.9 \text{ pF} \frac{4.25 \text{ V}}{(4 \times I_{bias})}$$

FIGURE 5. Current-limit Comparator Delay (Equivalent Circuit Model)

FIGURE 6. Current-limit Comparator Delay vs. Bias Current

V_{be} has negative temp coefficient.
R has positive temp coefficient.

$$V_{CL} = 0.7 \text{ V} + I_{bias} \times 36 \text{ k}$$
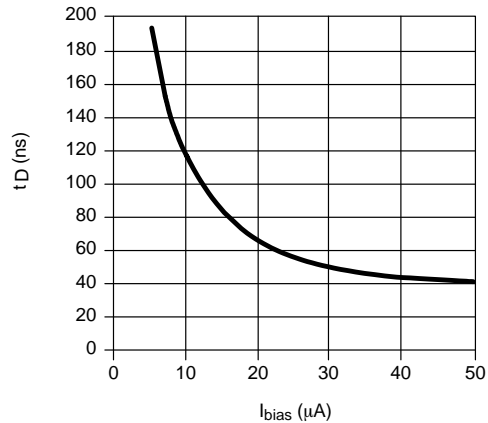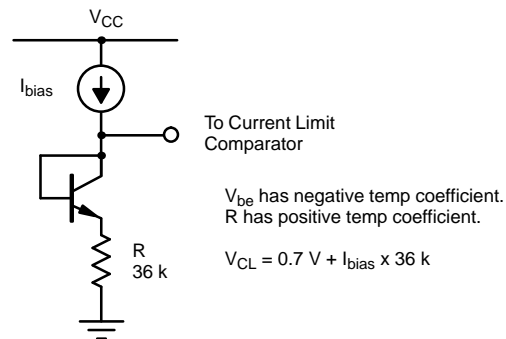
FIGURE 7. Current-Limit Trip Voltage vs. Programmed Bias Current

MOSFET Driver

The driver circuit is a CMOS inverter whose typical characteristics are shown in Figure 8. The n-channel (turn-off) peak drive current is about 20% higher than that of the p-channel (turn-on) device. Although the on-resistance ($r_{DS(on)}$) of the output drive is specified, usually the saturation current (where $\Delta I_D/\Delta V_{DS}$ is very small) determines the switching speed. This is due to the vertical load line of capacitive loads. In other words, the MOSFET gate capacitance appears as a short circuit across the driver's output.

The CMOS driver is fast enough to effectively eliminate cross-conduction current during switching transitions, at least when $V_{CC} \leq 10$ V. Above this level, a small amount of cross conduction occurs. Therefore, the greatest gate drive efficiency (approaching 100%) is achieved by keeping $V_{CC} \leq 10$ V, and the gate drive power is given by

$$P_{gate} = Q_g \times f_s \times V_{CC}$$

where

Qg = MOSFET gate charge
f_s = switching frequency
V_{CC} = supply voltage

Shutdown Logic

The shutdown logic employs an RS flip-flop to disable the output drive. Both the SHUTDOWN and RESET inputs have internal current-source pull-ups (equal to I_{bias}), so they can be left open when unused. As long as the SHUTDOWN input is held low, the output is OFF. If the RESET input is hard wired to $-V_{IN}$ (through a normally closed reset button if desired), any LOW input to SHUTDOWN will latch the output in the "off" state. It will remain off until power is recycled (or the reset button is pushed).

Undervoltage Lockout

During start-up, the depletion transistor charges the capacitance connected to the V_{CC} pin with a typical charging current of 15 to 20 mA. The output is disabled until V_{CC} reaches the undervoltage (UV) lockout voltage (typically 8.1 V). The IC requires less than 0.5 mA of current during this time, since the largest component of supply current is usually for the gate drive. When V_{CC} reaches 8.1 V, the output is enabled and the MOSFET begins switching. The supply current increases by $Q_g \times f_s$, and V_{CC} charges more slowly until it reaches the pre-regulator voltage (8.6 V).

If too much current is drawn from V_{CC} (for instance, to supply other circuitry), it is possible that the converter will be prevented from starting. Or it may oscillate on and off as it starts up, loads down the V_{CC} pin, shuts off, and then repeats this cycle. Consult the factory if a minimum pre-regulator current specification above 5 mA must be guaranteed.
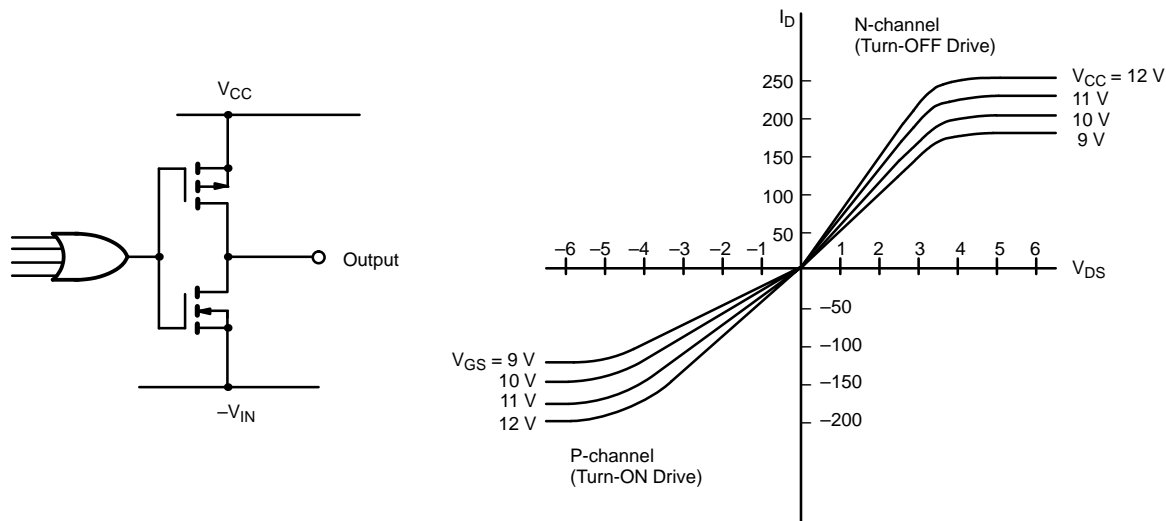

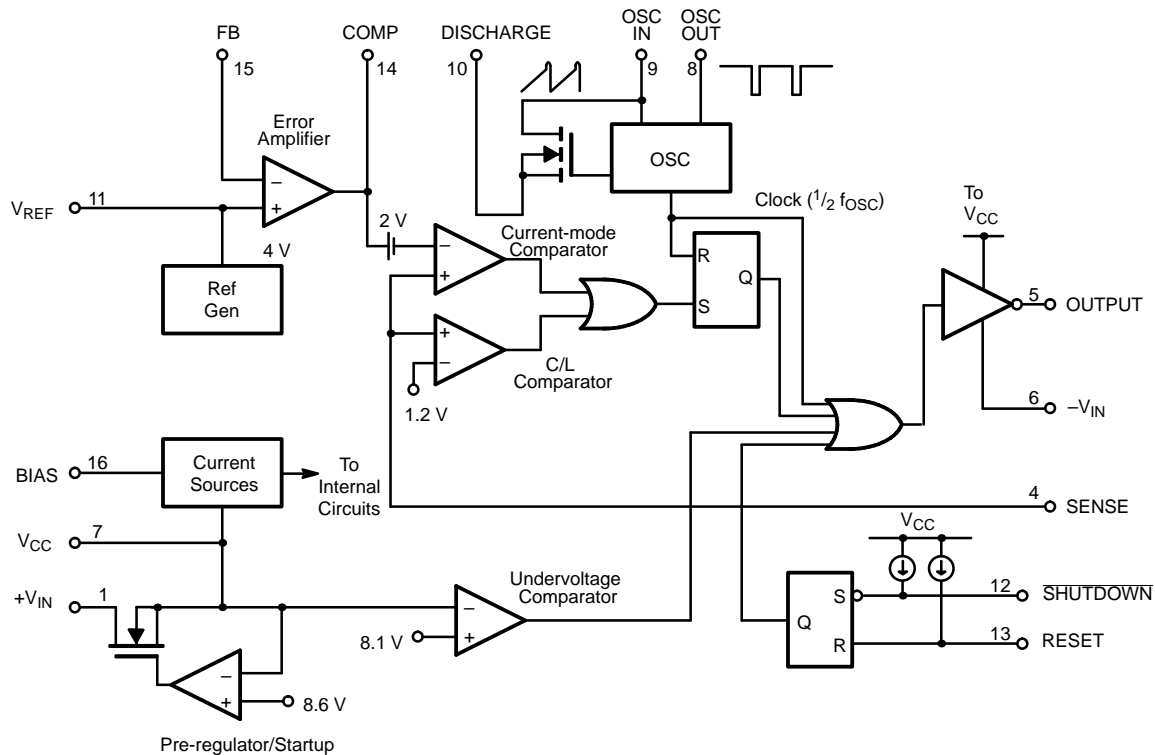**FIGURE 8.** Output Drive Characteristics

FIGURE 9. Si9120 Block Diagram

Flyback Converter Example

To illustrate the design procedure for a low-power off-line SMPS, a typical example should be presented. But what is a "typical" 5- to 10-W supply requirement? Should the output be a single +5 V or +12 V, or should a dual output, ± 5 V or ± 12 V, be used? How about +5 V and ± 12 V? There is no typical requirement, so a multiple-output design was chosen since cross regulation requirements make this the more difficult problem. The specifications for a 5-W supply with four outputs is given below.

Specifications

Input Voltage 90- to 130-V ac, 50 to 60 Hz

TABLE 1.				
Output Voltage (v)	Min Load (mA)	Max Load (mA)	Regulation (%)	Ripple (mV$_{p-p}$)
+30	1	4	± 5	200
+12	80	340	± 5	200
+5$_{(Main)}$	25	110	± 5	50
+5$_{(Aux)}$	20	80	± 5	15

Efficiency >80% Minimum
Switching Frequency 32 kHz

Circuit Description

The flyback converter circuit, shown in Figure 10, was designed for minimum cost and parts count. Since the regulation requirements are fairly loose, it is advantageous to eliminate feedback from primary to secondary. Output voltage is controlled indirectly by regulating a bootstrap auxiliary winding on the primary side. (Strictly speaking, the auxiliary winding is not required, as the chip will run directly from line power; but another feedback scheme would obviously be necessary.) All outputs are isolated from one another. Also, the primary-to-secondary isolation is designed to meet VDE safety requirements.

The power switching transistor (Q1) is an IRF820 rated at 500 V and 2.5 A. On-resistance is specified at 3 Ω. While this device may appear to be overkill for a 5 W output, it is the smallest 500-V die available, and it allows operation without a heatsink.

The flyback inductor (T1) is designed to operate in the discontinuous conduction mode. This makes loop compensation simple since there is no right half plane zero in DCM flyback converters. Also, since the power level is so low, the higher peak currents associated with this mode of operation pose no significant problems. The Si9120 provides all necessary control functions with only a handful of passive components.
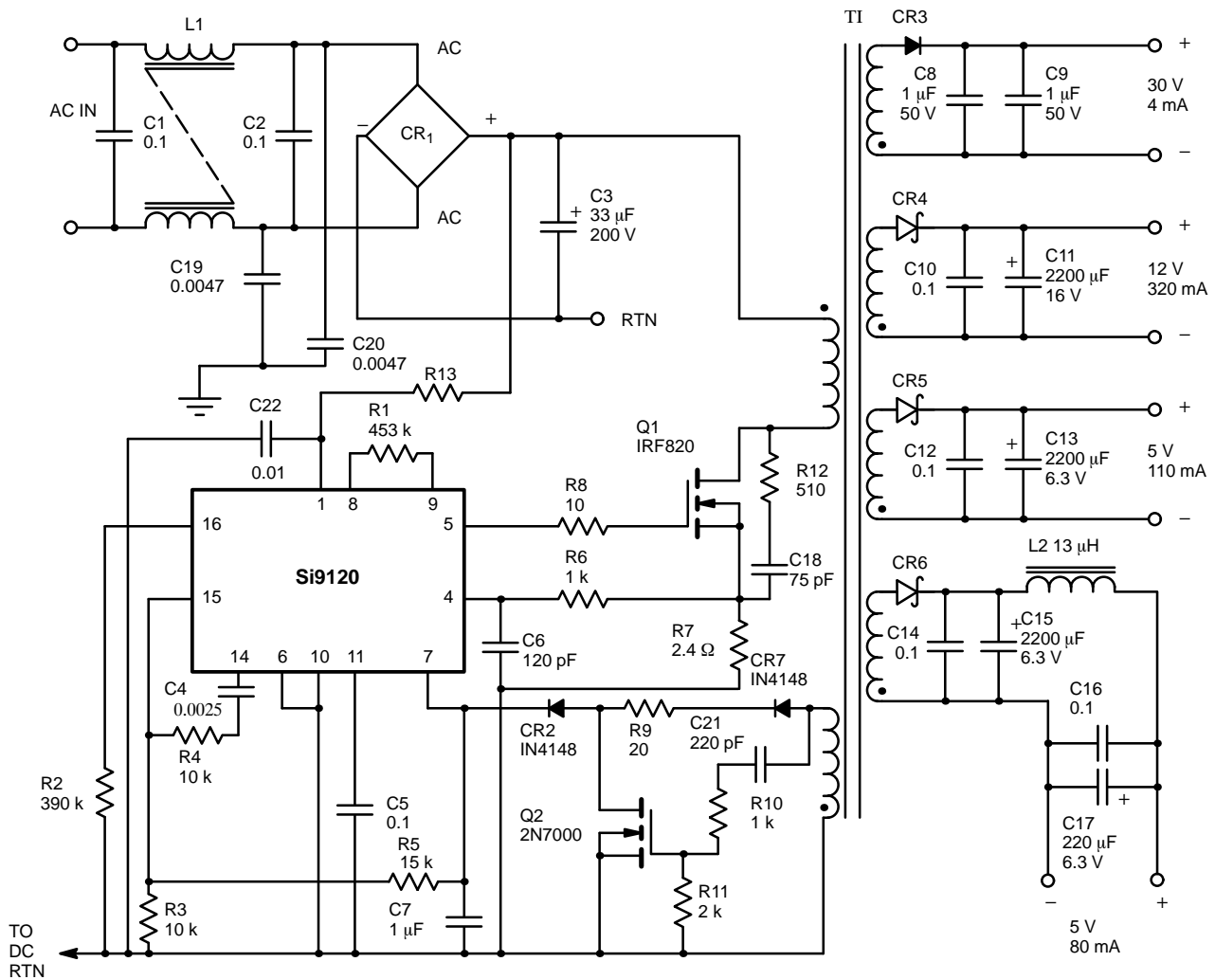
FIGURE 10. 5-W Offline Flyback Converter

Flyback Fundamentals

The flyback circuit works by storing energy in the flyback inductor during the switch's on-time and releasing this energy to the secondary circuits during the switch's off-period. The power transformer, in the case of a flyback converter, is not a transformer at all. Transformers work by coupling energy from primary to secondary, storing as little energy as possible. The flyback, however, stores all the energy for one cycle of operation in what is properly an inductor.

It is widely believed that current in an inductor cannot be changed instantaneously. This is not quite true. Ampere-turns are what cannot change instantaneously. If you could somehow change the turns, you could change the current on demand. This is what happens in the flyback inductor. During the switch-on time, some number of ampere-turns are developed in the primary winding. The power switch is then turned off in essentially zero time, forcing the ampere-turns to appear at the secondary windings. Thus, turns have changed, and amperes scale accordingly. Autotransformer action between the various windings forces the output voltages to track in proportion to the turn ratios of the windings. This forces the output capacitors to peak charge to the respective winding voltages and, thereby, provides regulation between windings. The better the coupling between windings, the better the cross regulation. Hence, all four outputs are wound closely together with no additional insulation between windings. By controlling the peak current through the primary winding during the on-time, the total energy per cycle, hence the total throughput power, can be controlled. By making this current a function of the output voltage error, voltage regulation is achieved.

On initial application of power to the supply, the high-voltage DMOS transistor in the Si9120 begins to charge the V_{CC} supply capacitor, C7. When approximately 8.1 V appears on the bias supply, the Si9120 undervoltage lockout enables the output driver. All internal bias voltages are stable at this point, and clean operation is assured. When V_{CC} reaches 8.6 V, the DMOS linear regulator reduces the charging current to maintain this voltage. Within a few cycles of operation, the bootstrap winding raises V_{CC} beyond the point at which the linear regulator tries to hold the bias supply. The DMOS transistor is forced to cut off. Now the V_{CC} supply is totally independent of the power line and draws no current from it.

A cycle is initiated by the Si9120 clock toggling the output driver on. The driver turns on power switch Q1, causing current to begin ramping up linearly in T1's primary winding. The current is sensed by R7 and filtered by R6 and C6. When the Si9120's current-sense comparator detects that the primary current has reached the control loop's programmed level, the power switch is shut off and energy stored in T1 begins to discharge into the secondary circuits.

To close the regulator loop, the voltage of the V_{CC} supply winding on the primary side is sensed and compared to a reference. The difference is multiplied by a high-gain amplifier. These functions are all performed by the Si9120. R3 and R5 divide the bias voltage down to the 4 V reference level. R4 and C4 provide for loop compensation, and C7 filters V_{CC}.

A major problem exists in any converter with a large input-to-output isolation voltage -- leakage inductance of the flyback inductor. A portion of the energy stored in this inductance will appear as a voltage spike on the feedback winding. The V_{CC} supply tends to charge to the peak of the spike, forcing the control loop to regulate all of the output voltages substantially below the desired values.

Spike suppression and proper operation of the regulator loop are provided by a blanking circuit (consisting of R9, R10, R11, C21, CR7, and Q2). At the instant Q1 turns off, a positive-going voltage appears at the anode of CR7. C21 forms a differentiator with R10 and R11 that produces a positive voltage on the gate of Q2. This turns on Q2 and clamps the anode of CR2 to ground, back-biasing CR2 and preventing the spike from passing through to the V_{CC} supply. A substantial portion of the energy contained in the voltage spike is shunted to ground through CR7 and R9 (the circuit is behaving, to some degree, like an active snubber). When the spike energy has been dissipated, the voltage drops to the nominal level. R11 then pulls Q2's gate voltage back down, turning off Q2 and allowing the remainder of the pulse to pass through to the V_{CC} supply. Figure 11 shows details of the blanking circuit in operation.

Figures 12-15 show details of the power supply operation. The input voltage for all photos was 115 V RMS and all loads are at maximum. Table 1 gives the line and load regulation of the circuit along with output ripple and efficiency data. At 85% efficiency, absolutely no heatsinks are required.
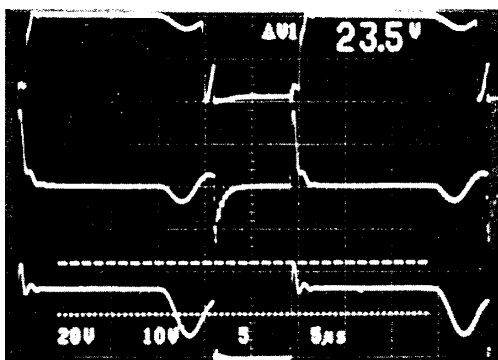

FIGURE 11. Top Trace – Anode of CR2
Center Trace – Gate of Q2
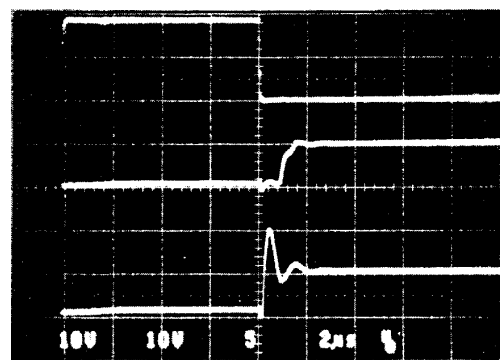Bottom Trace – Anode of CR7
Note spike amplitude of 23.5 V.

FIGURE 12. Top Trace – Gate Drive Q1
Center Trace – Anode of CR2
Bottom Trace – Cathode of CR7
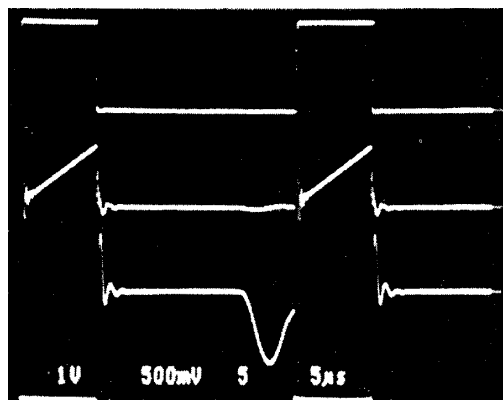
FIGURE 13. Top Trace – Gate Drive Q1
Center Trace – Voltage Across R7
Bottom Trace – Drain Voltage of Q1 (100 V/div)
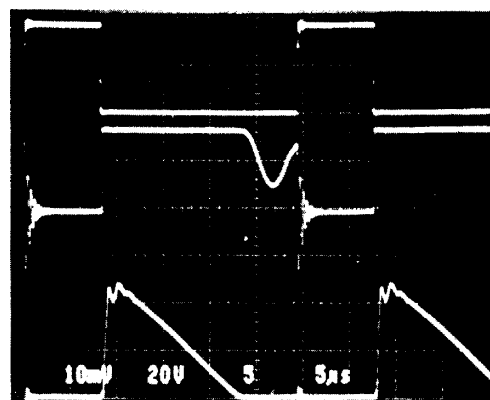
FIGURE 14. Top Trace – Gate Drive Q1
Center Trace – Anode of CR4
Bottom Trace – CR4 Current (500 mA/div)
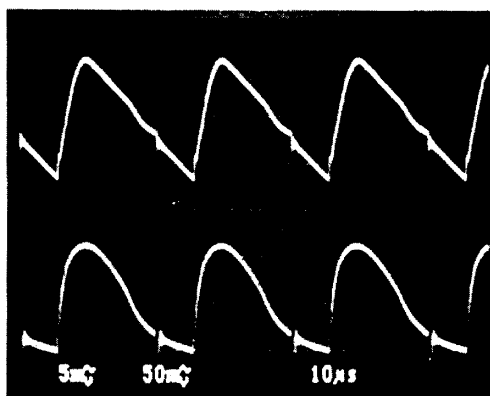
FIGURE 15. Top Trace – 30-V Output Ripple
Bottom Trace – 5-V, 80-mA Ripple

TABLE 2. 5-W OFF-LINE FLYBACK TEST DATA				
Full Load Outputs (V)				
AC Input (V RMS)	**12 V**	**30 V**	$5_{(Main)}$ **V**	$5_{(Aux)}$ **V**
80	11.00	28.50	5.019	5.058
100	11.05	28.60	5.046	5.080
115	11.08	28.70	5.060	5.095
130	11.11	28.77	5.072	5.111
Half Load Outputs (V)				
80	11.26	29.10	5.170	5.214
100	11.32	29.16	5.180	5.223
115	11.33	29.19	5.186	5.230
130	11.34	29.92	5.190	5.234
Half Load Outputs (V)				
80	11.26	29.10	5.170	5.214
100	11.32	29.16	5.180	5.223
115	11.33	29.19	5.186	5.230
130	11.34	29.92	5.190	5.234
Output Ripple (mV Pk–Pk)				
	90	125	23	12

Actual measured outputs tabulated at various line and load conditions ($5_{(Main)}$ = 5 V, 110 mA, $5_{(Aux)}$ = 5 V, 80 mA)
Full Load Drop Out Voltage = 64-V RMS
Efficiency = (P_{out}/P_{in}) 100% = (4.98/5.86) 100 = 85%

CIRCUIT DESIGN DETAILS

Selecting the Input Capacitor

For a 90-V ac input, the bus voltage is

$$90 \sqrt{2} = 127 \text{ V dc}$$

If 20 V of ripple is allowed, the lowest input voltage is 107 V dc. For some margin, use 100 V dc. For a 5-W output with 80% efficiency, $\eta = 0.8$;

$$P_{in} = P_{out}/\eta = 5/0.8 = 6.25 \text{ W}$$
$$I_{in} = P_{in}/V_{IN} = 6.25/100 = 62.5 \text{ mA}$$

Input ripple is assumed to be 20 V_{p-p}. The low frequency limit is 50 Hz; thus, the ripple frequency is 100 Hz.

$$C = I \times \Delta T/\Delta V$$
$$= (0.0625) (0.01)/20$$
$$= 31.25 \text{ } \mu F$$

33 μF is a standard value.

Finding the Peak Switch Current

At 100 V dc in, the maximum duty factor D = 45%.

$$I_{pk} = 2 \times I_{avg}/D_{max}$$
$$= 2 (0.0625)/0.45$$
$$= 0.28 \text{ A}$$

The RMS switch current is

$$I_{RMS} = I_{pk} \sqrt{\frac{D}{3}} = 0.28 \quad 0.45 \sqrt{3} = 0.11 \text{ A}$$

Switch Voltage Rating and Temperature Rise

The transformer primary voltage during the off-time will be independent of input line voltage but must be equal to or greater than the dc input voltage at low line. The maximum switch off-voltage equals the dc input at high line plus the transformer off-voltage. If the transformer off-voltage is assumed to be 125 V (the peak of the rectified sine wave at low line), then

$$V_{off(max)} = V_{in(max)} + 125 \text{ V} = 130 \sqrt{2} + 125 = 308 \text{ V}$$

Allowing approximately 100 V for the leakage inductance spike, $V_{DS(max)} \leq 408$ V. A 500-V FET gives a good safety margin. The IRF820 is rated 500 V, 3 Ω. For $T_J = 100°$C, the $r_{DS(on)}$ scale factor = 1.6, so the worst case on-resistance is

$$r_{DS(on)} = 3 \text{ } \Omega \text{ (1.6)}$$
$$= 4.8 \text{ } \Omega$$

Conduction loss is

$$(0.11 \text{ A})^2 (4.8 \text{ } \Omega) = 0.058 \text{ W}$$

Assuming switching losses are equal to conduction losses, total dissipation in the FET equals 0.116 W. With no heatsink,

$$\Delta T_J = (R_{\Theta JA}) (P_{DISS})$$
$$= (80°\text{C/W}) (0.155 \text{ W})$$
$$= 9.3°\text{C}$$

Primary Inductance

Operating frequency was selected at approximately 32 kHz to permit synchronization to a television horizontal scan if needed. Period $T_S = 31.25$ μs, so

$$t_{on(max)} = (0.45) (31.25)$$
$$= 14 \text{ } \mu s$$

I_{pk} was calculated at 0.28 A and is also invariant with line voltage. At low line,

$$V_{IN(min)} = 100 \text{ V and}$$
$$L_P = \frac{V \Delta t}{\Delta I} = \frac{100(14 \mu s)}{0.28} = 5 \text{ mH}$$

where

L_P = Primary Inductance
$\Delta t = t_{on(max)}$
$\Delta I = I_{pk}$

AN707

Vishay Siliconix

Flyback Inductor Design

Using the area product method,

$$A_c A_e = \frac{(25.32 \, L_P I_{pk} D^2) \, 10^8}{B_{max}} \qquad \text{(REF–2)}$$

where

D	= wire diameter in inches
B_{max}	= maximum flux swing in gauss
A_c	= core cross sectional area in cm^2
A_e	= effective window are in cm^2
$A_c A_e$	= core-window area product in cm^4

Assuming 400 cir/mil/A and 0.11 A RMS, #32 AWG is adequate. Use #31 for cool operation; the diameter of #31 AWG is 0.0108 inches. Allow B_{max} = 2000 gauss.

$$A_c A_e = \frac{(25.32)(5 \, mH)(0.28 \, A)(0.0108)^2 \, (10^8)}{2000}$$

$$= 0.207 \, cm^4$$

PQ 42020 size core has $A_c A_e = 0.238 \, cm^4$, so it should handle the power.

Find the air gap, I_g, as:

$$I_g = \frac{1.26 \, L_P I^2 \, pk \, \times \, 10^8}{A_c B_{max}^2} = \frac{(1.26)(5.0 \, E\text{-}3)(0.28)^2(10)^8}{(0.58) \, (2000)^2}$$

$$= 0.213 \, cm$$
$$= 8.4 \, mils$$

8 mils is a standard air gap.

<u>Calculate primary turns</u>, N_P. For the chosen core with an 8 mil air gap, the inductance factor, $A_L = 363 \, mH/1000$ turns.

$$N_P = 1000 \sqrt{\frac{L_P}{A_L}}$$

$$N_P = 1000 \sqrt{\frac{5.0}{363}} = 117 \, \text{turns}$$

<u>Solve for secondary turns</u>, N_S. Based on the feedback winding,

$$N_S = N_P \, \frac{(V_O + V_f) \, (1 - D_{msc})}{V_{in(min)} \, D_{max}}$$

$$\text{[See REF. 2]}$$

$$= \frac{(117) \, (10.0 + 0.7) \, (1 - 0.45)}{(100 \, V) \, (0.45)} = 15.3 \, \text{turns}$$

where

V_f	= diode forward voltage
V_O	= output voltage
D_{max}	= maximum duty factor
$V_{IN(min)}$	= dc bus voltage at low line

Use 15 turns. This must be less than or equal to the calculated number of turns to ensure current resetting to zero during the off time.

Scaling voltages for other outputs:

10.7 V/15 turns = 0.7133 V/turn

For all outputs:

$$V_{pk} = V_O + V_f$$

where

V_{pk} is transformer secondary voltage.

$$N_S = V_{pk}/0.7133 \, \text{V/turn}$$

After calculating all turn numbers and scaling slightly to optimize output voltage balances, the following turns resulted:

+30 V	43 turns
+12 V	17 turns
+5 V	8 turns
10 V bias	15 turns

<u>Choose Wire Sizes</u>. Core window area $A_e = 0.384 \, cm^2$. Allowing about a 50% fill factor results in a winding area of

0.5 (0.384) = 0.192 cm^2

#31 AWG was assumed for primary. The wire chart lists 1072 turns/cm^2 for #31 AWG.

117/1072 = 0.1091 cm^2
0.192 – 0.1091 = 0.083 cm^2 left for secondaries

Scaling for the percentage of power output and allotting window area accordingly, the following wire gauges result:

30 V, #40 AWG. (This is about the smallest wire gauge one would use for reliable design and ease of manufacture.)
12 V, #25 AWG
5 V, #31 AWG both outputs
Feedback, #40 AWG for same reasons as +30 V output

Calculating Output Currents

To determine the peak and RMS output currents, the following equations apply:
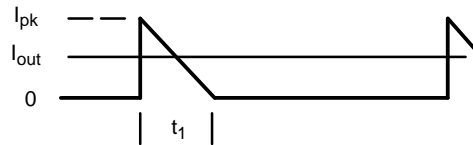
Output Current Waveform

$$t_1 = \left(\frac{2\,(I_{out})\,A_L\,N^2}{f(V_{OUT} + V_f)(10^9)} \right)^{\frac{1}{2}}$$

$$I_{pk} = \frac{2(I_{out})}{t_1 f}$$

$$I_{RMS} = \sqrt{\frac{t_1 f}{3}}$$

Where:

t_1 = current decay time
I_{out} = average load current
A_L = core inductance constant in mH/1000 turns
I_{pk} = peak secondary current
f = operating frequency
N = number of turns

Results are as follows:

TABLE 3.			
	I_{pk} (A)	t_1 (μs)	I_{RMS} (A)
12 V	1.60	12.85	0.59
30 V	0.11	2.34	0.017
5$_{(Aux)}$ V	1.08	4.60	0.24
5$_{(Main)}$ V	1.28	5.39	0.31
10 V bias	0.16	1.2	1.8

Selecting Output Diodes and Capacitors

Armed with the above data, selection of diode current ratings is possible using the RMS currents calculated. Also, the output capacitors can be sized based on the peak currents. The peak-to-peak ripple will be approximately equal to (I_{pk})(ESR). On the 5 V, 80 mA output, due to a very low ripple specification, a two stage filter to minimize capacitor size was easiest to use. The inductor is a small ferrite core with a few turns of wire. The 30-V output needs only a couple of microfarads of capacitance if ESR = 0. A 2-μF ceramic capacitor fills the bill.

The timing resistor was initially selected at 500 kΩ (from the graph on the Si9120 data sheet) and was optimized empirically at 453 kΩ. Be sure to measure operating frequency on pin 5, as the scope probe capacitance on pin 9 will substantially alter the operating frequency.

Calculating the Primary Current Sense Resistor Value

The minimum current limit threshold is specified at 1 V. The calculated peak primary current is 0.28 A. Allowing approximately 25% over current,

I_{pk} = (0.28) (1.25) = 0.35 A
R_{cs} = E_s/I_{pk} = 1.0/0.35 = 2.86 Ω

2.7 Ω is the nearest standard value. R6 and C6 set a 120 ns time constant on the current sense to filter noise spikes.

The blanking circuit differentiator time constant was selected at approximately 0.5 μs. R10 and R11 reduce the gate voltage amplitude to an acceptable level. R3 and R5 divide the feedback voltage down to 4.00 V. R5 was made adjustable for test purposes, and should be approximately 15 kΩ.

Loop Compensation

A frequently asked question is "How can I close the loop without a $40-K analyzer?" Well, a number of techniques exist — some tedious, others not quite as bad. The most reliable approach is to apply a pulsed load to the output and empirically adjust the RC compensation for a well-damped exponential output-voltage recovery. With a little practice, this can be done expeditiously. It also has the advantage of showing any problems which may arise when one or more circuit elements are driven non-linear, as can occur during a large transient. This information is missing in a small-signal response plot. Be aware, however, that a load-pulse test lacks the quantitative information of a good Bode plot and fails to permit an accurate assessment of design margins. But with a little hands-on experience, it will be easy to get a good feel for when it's right.
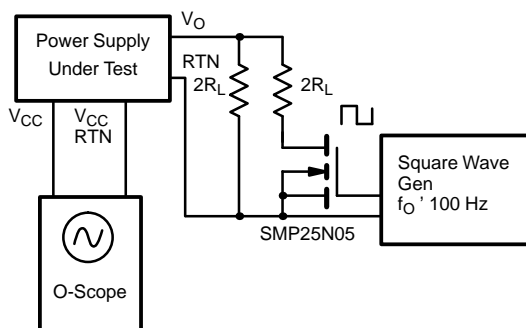
FIGURE 16. Pulse Load Test Setup

Figure 16. This allows a load step to be applied to the highest power output. If a bootstrap winding is not used for feedback, apply the step load to the regulated output. The amplitude of the step should be 25% to 50% of the full load current. The repetition rate should be low, around 100 Hz. Monitor the voltage on the V_{CC} pin of the Si9120, as this is controlled by the feedback loop, and watch the recovery characteristics. Gradually increase R4 and decrease C4 to obtain a good response.

Proceed as follows: Set C4 to approximately 0.1 μF. This sets the error amplifier to unity gain at approximately 100 Hz (Xc = R5 @ 100 Hz). Set R4 to zero. Set up the circuit shown in

Figure 17 shows the step response to several combinations of RC compensation. A small capacitor across R5 will also speed up the response, but may not be required. In addition, it may be desirable to add a small (100 to 1000 pF) capacitor directly across pins 14 and 15 of the Si9120 to roll off the error amplifier's high frequency gain. Be sure to repeat the above procedure for low and high input line voltages. When the response looks like line D in Figure 17, you're done.

FIGURE 17. Step Response to Combinations of RC Compensation

CONCLUSION

Using the Si9120, the design of low-power, high-efficiency, switching power supplies for off-line applications becomes straightforward. By running a DCM flyback topology under current-mode control, a reliable, easily compe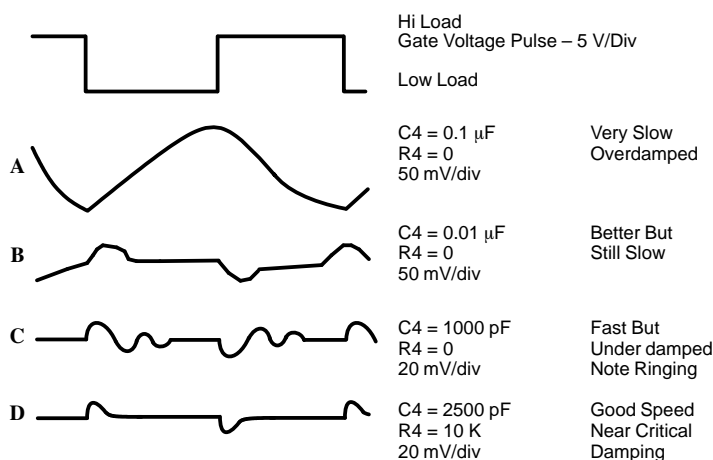nsated design is achieved. The leakage inductance spike-blanking circuit presented here makes for a well-regulated supply while allowing VDE voltage-isolation requirements to be met.

FLYBACK CONVERTER PARTS LIST

C1, C2 . . . . 0.01 µF, 250 V ac, class X2, Vishay Roederstein F1773-310-2900
C3 . . . . 33 µF, 200 V United Chemicon SL200VB33RU16X31LL
C4 . . . . 2500 pF, 50 V ceramic, Vishay Vitramon VJ1206Y252KXAAT
C5, C10, C12, C14, C16 . . . . . 0.1 µF, 50 V ceramic, Vishay Vitramon VJ1206Y104KXAAT
C6 . . . . 120 pF, 50 V ceramic, Vishay Vitramon CJ0402Y121KXAAT
C7, C8, C9 . . . . 1 µF, 50 V ceramic, Vishay Vitramon VJ1812Y105KXAAT
C11 . . . . 2200 µF, 16 V United Chemicon SXC16VB222M18X35LL
C13, C15 . . . . 2200 µF, 6.3 V United Chemicon SXC6.3VB222M16X25LL
C17 . . . . 220 µF 6.3 V United Chemicon SXC6.3VB221M10X12LL
C18 . . . . 75 pF, 500 V (mica or ceramic), Vishay Vitramon VJ12DCA750KXEAT
C19, C20 . . . . 0.0047 µF, 250 V ac, class Y, Vishay Roederstein F1710-247-1000
C21 . . . . 220 pF, 50 V (ceramic), Vishay Vitramon VJ0402Y221KXAAT
CR1 . . . . Bridge rectifier 600 V, 1 A
CR3 . . . . MUR110
CR4 . . . . 1N5822
CR5, CR6 . . . . 1N5819
IC1 . . . . Si9120DJ
L1 . . . . Common-mode choke 8 mH
L2 . . . . 13 µH: core: Magnetics Inc J40401TC with 6 turns # 26 AWG
Q1 . . . . IRF820
Q2 . . . . 2N7000
R1 . . . . 453 kΩ . . . . 1% . . . . . 1/4 W. Vishay Dale CRCW12064533FRT1
R2 . . . . 390 kΩ . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW12063903FRT1
R3 . . . . 10 kΩ . . . . 1% . . . . . 1/4 W. Vishay Dale CRCW12061002FRT1
R4 . . . . 10 kΩ . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW1206103JRT1
R5 . . . . 15 kΩ . . . . 1% . . . . . 1/4 W. Vishay Dale CRCW12061502FRT1
R6, R10 . . . . 1 kΩ . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW1206102JRT1
R7 . . . . 2.7 Ω . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW12062R7JRT1
R8 . . . . 10 Ω . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW120610RJRT1
R9 . . . . 20 Ω . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW120620RJRT1
R11 . . . . 2 kΩ . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW120602JRT1
R12 . . . . 510 Ω . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW1206511JRT1
R13 . . . . 10 kΩ . . . . 5% . . . . . 1/4 W. Vishay Dale CRCW1206103JRT1
T1 . . . . Schott Corp #6712244

REFERENCES

1) Liu, K.H., *"Effects of Leakage Inductance on the Cross Regulation in a Discontinuous-Mode Flyback Converter,"* Proceedings, 1989 High Frequency Power Conference, Naples, Florida.

2) Chryssis, G., *"High Frequency Switching Power Supplies,"* McGraw Hill 1984.