FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-26903-2E

ASSP

CMOS

Dolby Digital (AC-3) Decoder LSI

MB86342

■ DESCRIPTION

Dolby Digital (AC-3) is a perceptual digital audio coding technique of unprecedented efficiency, quality and versatility.

Fujitsu has developed Dolby Digital (AC-3) 5.1-ch full decodable LSI.

This LSI is certificated as " Dolby Digital (AC-3) Decoder LSI " by Dolby Laboratories Licensing Corporation.

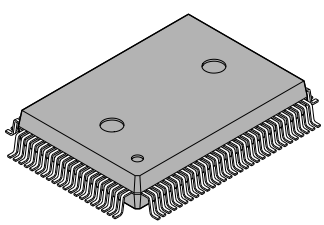
■ FEATURES

- Dolby Digital (AC-3) 5.1ch Full Decode
  - All bit-rate and All sampling frequency
  - Down Mix
  - Dialog Normalization
  - Dynamic-range Compression
  - Noise sequencer (Test tone)
  - Each channel can be independently set
- Dolby Pro Logic Decode
- Dolby Digital (AC-3) + Dolby Pro Logic Decode
- 16/18/20bit Audio Data Input/Output

(Continued)

■ PACKAGE

100 pin, Plastic QFP



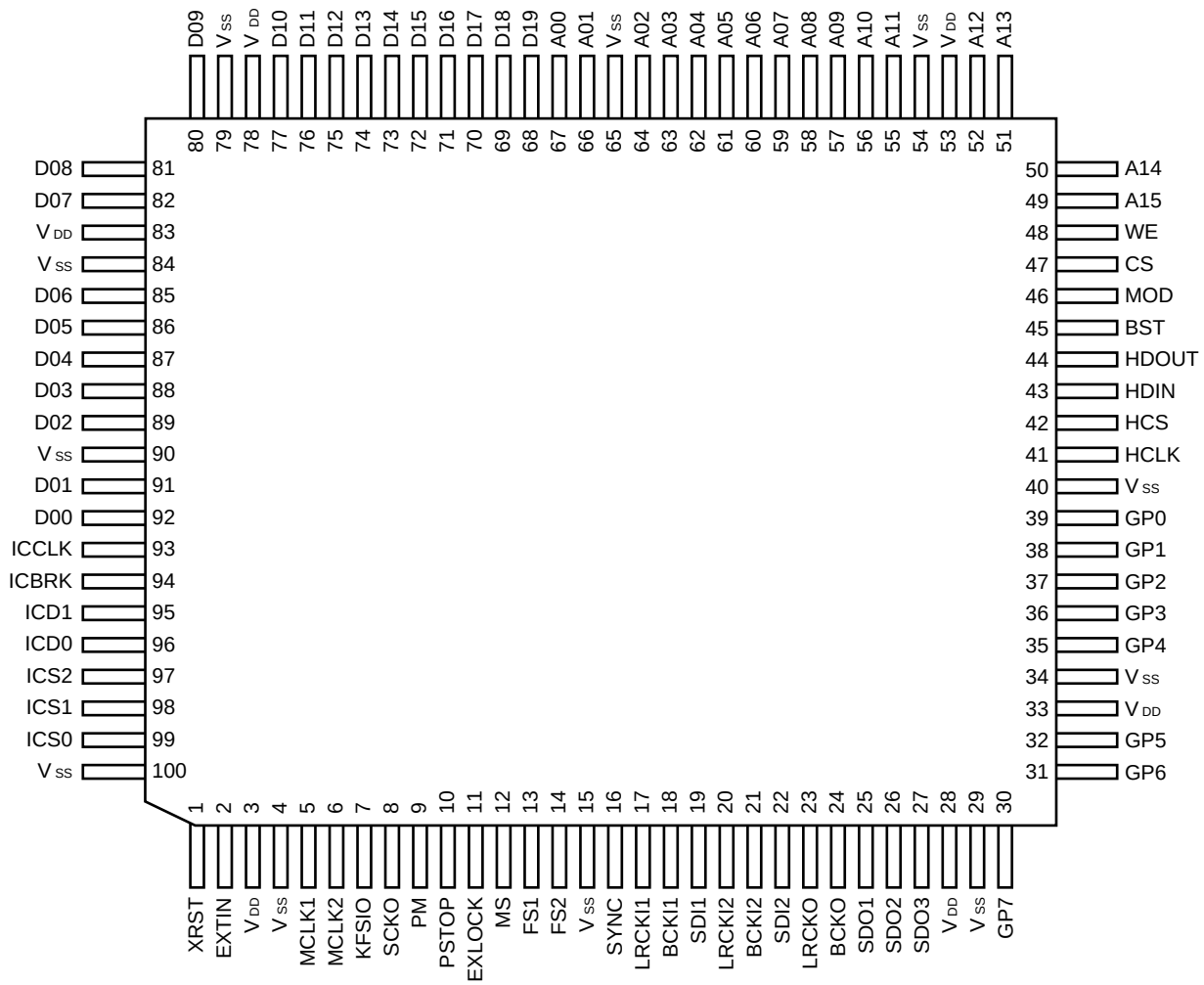
(FPT-100P-M06)

(Continued)

- Operat with only audio system clock (384fs) by built-in PLL
- Correct with ADC,DAC,DIR and DIT with type audio I/F three lines
- Control by Host I/F
- 3.0V to 3.6V operation
- QFP-100 pin package

■ PIN ASSIGNMENT

(Top view)

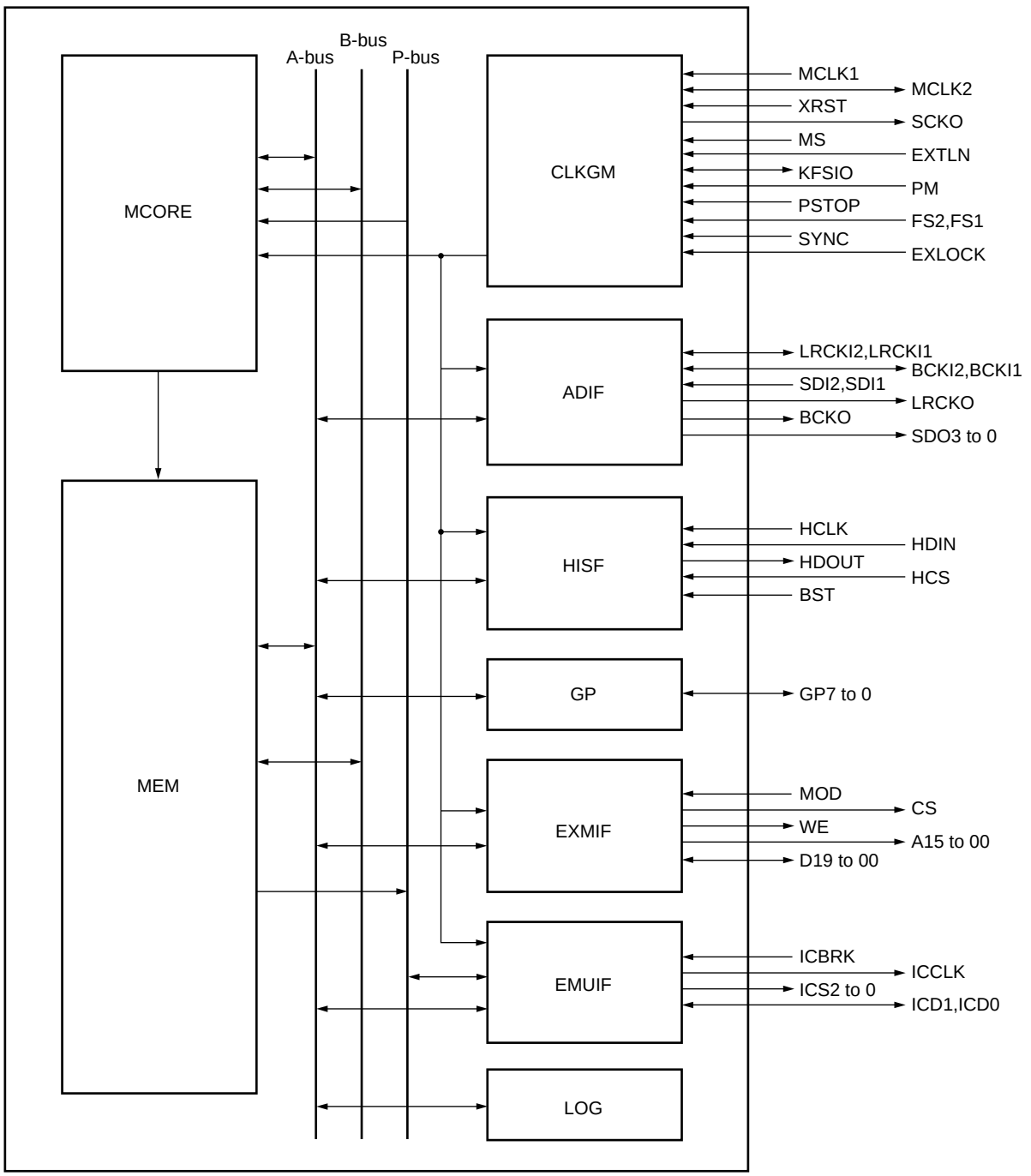


(FPT-100P- M06)

■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Function
5	MCLK1	I	Clock input
6	MCLK2	I/O	Clock input/output
1	XRST	I	Reset signal input
8	SCKO	O	System clock output
12	MS	I	Master/Slave select input L: Master (X'tal) H:Slave (external clock)
16	SYNC	I	Synchronous/Asynchronous select input
2	EXTIN	I	System clock input (384fs)
13, 14	FS1, FS2	I	Sampling frequency switching signal input
7	KFSIO	I/O	Audio input/output clock (384fs)
9	PM	I	Test pin (usually clipped to GND)
10	PSTOP	I	PLL and crystal oscillator control signal
11	EXLOCK	I	Lock signal input of EXTIN
41	HCLK	I	Clock input for serial input-data of host interface
43	HDIN	I	Serial data input of host interface
44	HDOUT	O	Serial data output of host interface
42	HCS	I	Chip-select signal input of host interface
45	BST	I	Usually clipped to GND
30 to 32, 35 to 39	GP0 to GP7	I/O	Input/output of 8-bit general port data
17	LRCKI1	I/O	Sampling clock input/output for audio interface serial data
18	BCKI1	I/O	Bit clock input/output for audio interface serial data
20	LRCKI2	I	Sampling clock input for audio interface serial data
21	BCKI2	I	Bit clock input for audio interface serial data
19, 22	SD1, SD2	I	Serial data input of audio interface
23	LRCKO	O	Sampling clock output for audio interface serial data
24	BCKO	O	Bit clock output for audio interface serial data
25 to 27	SDO1 to SDO3	O	Serial data output of audio interface
46	MOD	I	Bus-mode control signal input
47	CS	O	Chip-select signal output for external SRAM interface
48	WE	O	Write enable signal output for external SRAM interface
49 to 52, 55 to 64, 66, 67	A00 to A15	O	Address data output of external SRAM interface
68 to 77,80 to 82 85 to 89, 91, 92	D00 to D19	I/O	Data input/output of external SRAM interface
93	ICCLK	O	Clock output for emulator
94	ICBRK	I	External break control signal input for emulator
95, 96	ICD0, ICD1	I/O	Input/output signal for data/address of emulator
97 to 99	ICS0 to ICS2	O	Status signal output for emulator

■ BLOCK DIAGRAM



■ FUNCTION OF EACH BLOCK

MCORE : MUCAP Core

MUCAP Core is a 20-bit fixed point DSP core. This core operates MOVE, BRANCH, INTERRUPT, ADDRESSING and ARITHMETIC operations.

CLKGM : Clock Generation Module

This module generates internal and external clock. two type of clocks are generated external clocks and clock from external crystal oscillator.

ADIF : Audio Interface Module

This module is an interface of input/output serial audio data to external.

- 2-channels of input port, and 3-channel of output port.
- 2-audio data input registers and 6-output registers (20-bit).

HSTIF : Host Interface Module

This module transfers asynchronous serial data to host CPU, which has input data register and output data register(20-bit).

GP : General Port Module

This module has a 8-bit direction register and 8-bit data register. Each port is independent as a 1pin input/output general port(total 8pins).

EXMIF : External Memory Interface Module

This module reads and writes data to external memory(SRAM), which has 3-byte data read/write mode and 1word(20bit) data read/write mode.

This module uses in-service-register in order to read and write 3-byte data.

EMUIF : Emulator Interface Module

This module is used for in circuit emulation.

LOG : LOG Module

This module has registers to refer to table data for the operation of logarithmic functions.

MEM : Memory Module

This module restores data and programs.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Vss = 0V	Vss–0.5 to +4.0	V
Input voltage	V_{IN}	—	Vss–0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	—	Vss–0.5 to V_{DD}+0.5	V
Output current	I_{OUT}	I_{OL} = 4.0mA	±14	mA
		I_{OL} = 8.0mA		
Storage temperature	Tstg	—	–40 to +125	°C
Overshoot	—	50ns (Max.)	V_{DD}+1.0	V
Undershoot	—	50ns (Max.)	V_{DD}+1.0	V

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}	3.00	3.30	3.60	V
“H”-level input voltage	V_{IH}	$V_{DD} \times 0.7$	—	V_{DD}	V
“L”-level input voltage	V_{IL}	V_{SS}	—	$V_{DD} \times 0.2$	V
Operating temperature	Ta	0	—	70	°C

■ ELECTRICAL CHARACTERISTICS

1. Input/Output Pin Capacitance

(Ta = 25°C, frequency = 1MHz)

Parameter		Symbol	Requirements	Unit
Input pin		C_{IN}	Max.16	pF
Output pin	I_{OL} = 4mA 8mA	C_{OUT}	Max.16	
I/O pin	I_{OL} = 4mA 8mA	$C_{I/O}$	Max.16	

2. DC Characteristics

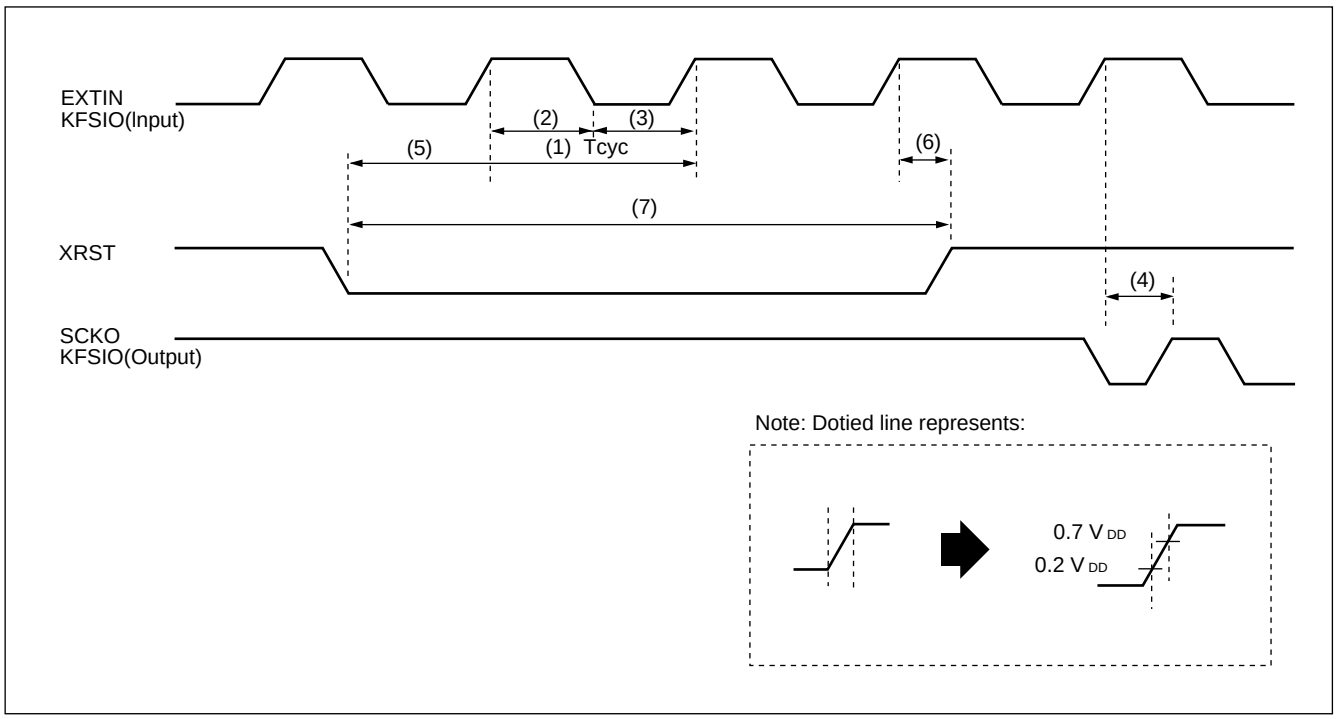
(V_{DD} = 3.0 to 3.6V, Vss = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply current	I_{DDS}	Standby mode *1	—	—	100	µA
	I_{DD}	Operating mode	—	160	240	mA
"H"-level input voltage	V_{IH}	—	$V_{DD} \times 0.7$	—	V_{DD}	V
"L"-level input voltage	V_{IL}	—	Vss	—	$V_{SS} \times 0.2$	V
"H"-level output voltage	V_{OH}	I_{OH} = –4mA	V_{DD}–0.5	—	V_{DD}	V
		I_{OH} = –8mA				
"L"-level output voltage	V_{OL}	I_{OL} = 4mA	V_{SS}	—	0.4	V
		I_{OL} = 4mA				
Input leakage current *2 (Tri-state pin Input)	I_{LI}	V_I = 0–V_{DD}	–10	—	10	µA
	I_{LZ}		–10	—	10	
Pull up/down resistance	RP	—	10	25	50	kΩ
Output short-circuit current	I_O*3	Type/condition	V_O = V_{DD}		V_O = 0V	mA
		Normal/I_{OL} = 4mA	+40		–40	
		Normal/I_{OL} = 8mA	+80		–80	

*1: V_{IH} = V_{DD}, V_{IL} = V_{SS} The memory is in the standby mode.
*2: If an Input buffer with pull-up/-down resistor is used, the input leakage current may exceed the above value.
*3: Maximum supply current at the short circuit of output V_{DD} or V_{SS}. For 1 second per LSI pin.

3. AC Characteristics

(1) EXTIN, SCKO, XRST



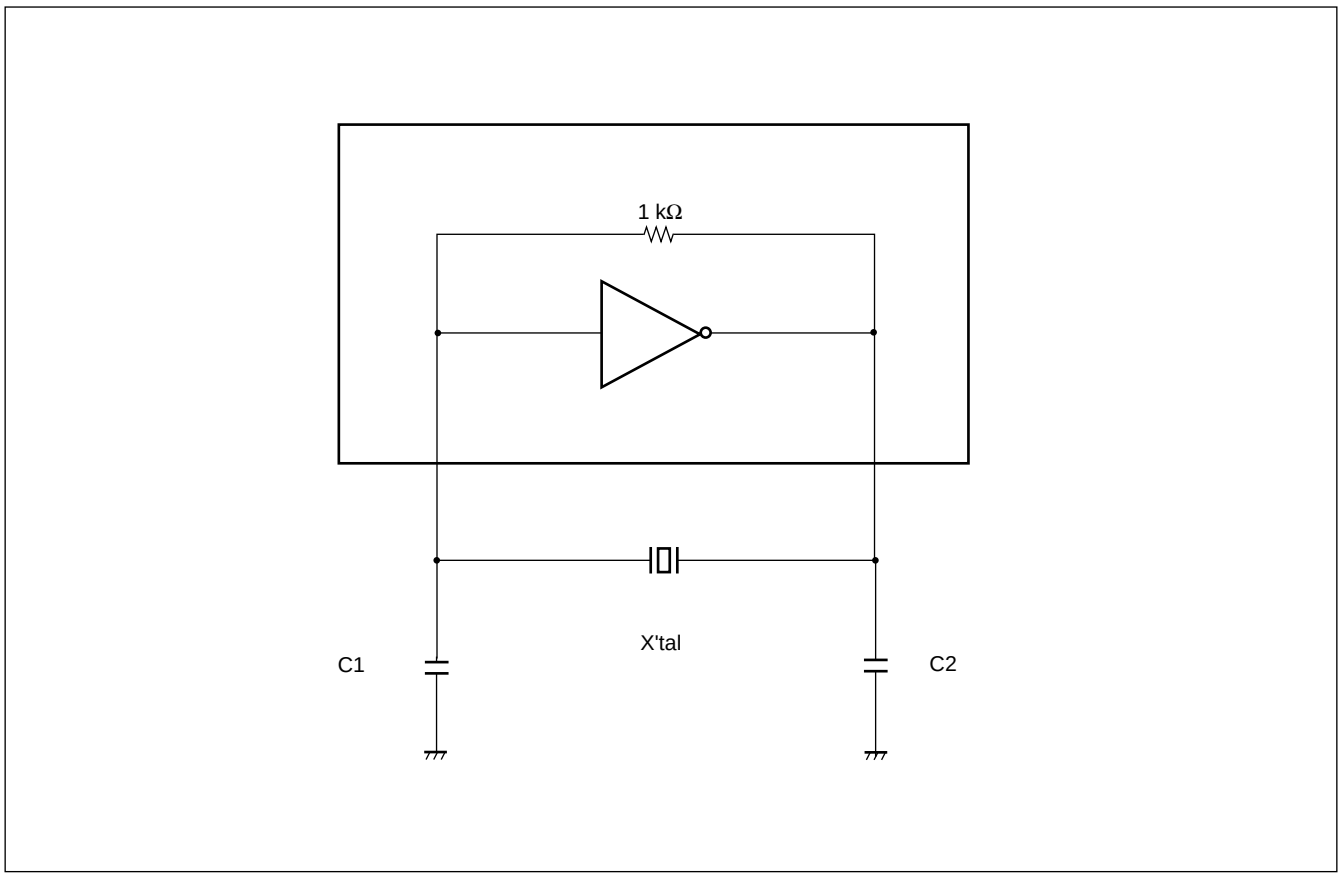
(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	EXTIN cycle	—	Tcyc	—	ns
(2)	EXTIN “H” pulse width	0.4×Tcyc	—	—	ns
(3)	EXTIN “L” pulse width	0.4×Tcyc	—	—	ns
(4)	SCKO delay time	—	—	11	ns
(5)	XRST setup time	6	—	—	ns
(6)	XRST hold time	3	—	—	ns
(7)	XRST “L” pulse width	*	—	—	ns
(8)	PLL lock-up time	100	—	—	µs

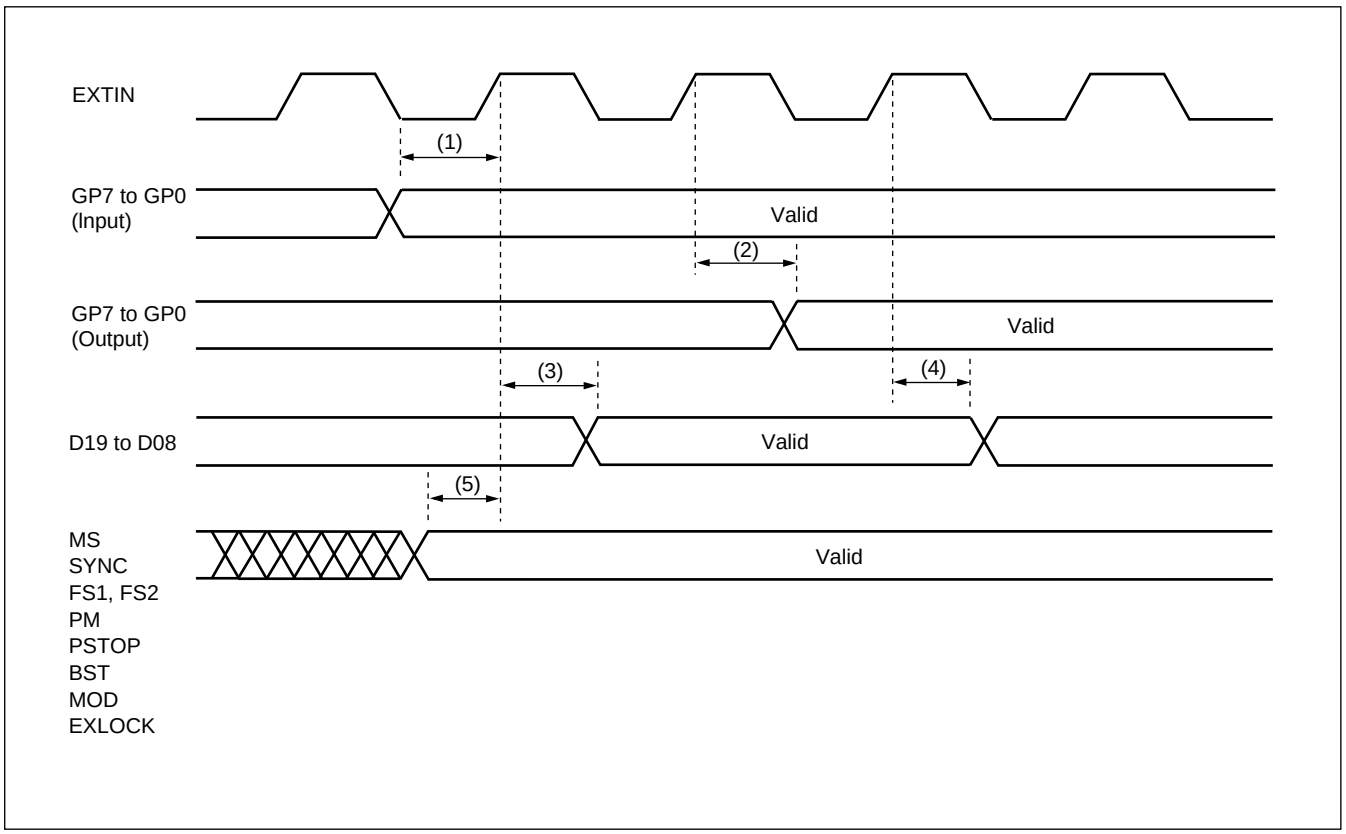
* : EXTIN frequency

EXTIN frequency (MHz)	Tcyc(ns)	Clock mode	Sampling frequency	PLL select	CORE master Clock (MHz)	XRST “L” pulse width(ns)
18.432	54.253	Fast mode	48	16/3	98.304	9/8Tcyc=61.035
		Slow mode		6	110.592	1Tcyc=54.253
16.9344	59.0514	—	44.1		101.6064	1Tcyc=59.0514
12.288	81.380	—	32	8	98.304	3/4Tcyc=61.035

(2) Crystal Oscillator



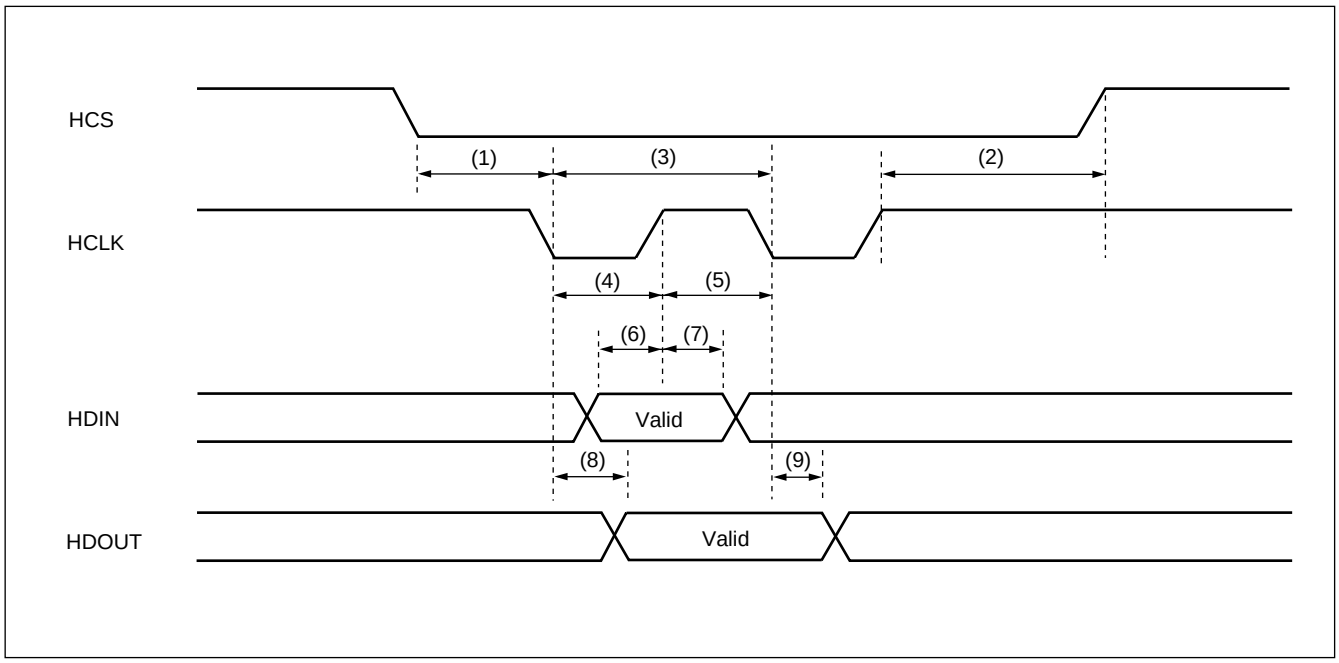
(3) GP0 to 7, D08 to 19, MS, SYSNC, FS1, FS2, PM, PSTOP



(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	GP0 to 7 setup time	6	—	—	ns
(2)	GP0 to 7 delay time	—	—	17	ns
(3)	D08 to 19 delay time	—	—	17	ns
(4)	D08 to 19 hold time	2	—	—	ns
(5)	Setup time	4	—	—	ns

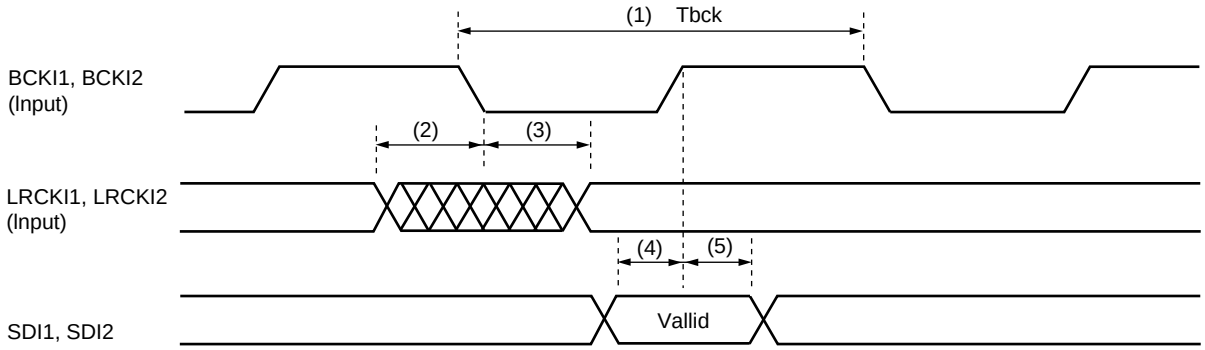
(4) HCS, HCLK, HDIN, HDOUT



(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	HCS clock active setup time	16	—	—	ns
(2)	HCS clock active hold time	16	—	—	ns
(3)	HCLK pulse cycle	36	—	—	ns
(4)	HCLK “H” pulse width	16	—	—	ns
(5)	HCLK ”L” pulse width	16	—	—	ns
(6)	HDIN setup time	4	—	—	ns
(7)	HDIN hold time	6	—	—	ns
(8)	HDOUT delay time	—	—	10	ns
(9)	HDOUT hold time	1	—	—	ns

(5) LRCKI1, LRCKI2, BCKI2, SDI1, SDI2 (Input Mode)



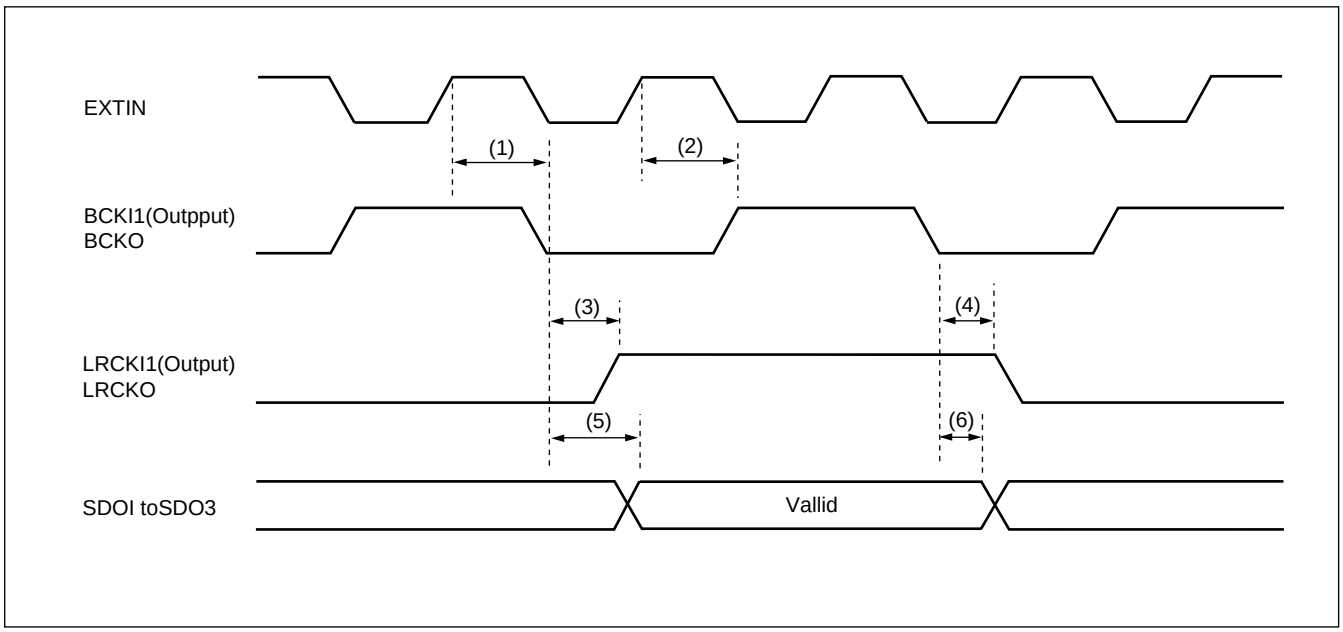
(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	BCKI1,BCKI2 cycle (Tbck)	—	*	—	ns
(2)	LRCKI1,LRCKI2 setup time	—	—	1/4 Tbck	ns
(3)	LRCKI1,LRCKI2 hold time	—	—	1/4 Tbck	ns
(4)	SDI1,SDI2 setup time	3	—	—	ns
(5)	SDI1,SDI2 hold time	6	—	—	ns

* : BCKI1, BCKI2 frequency

BCKI1, BCKI2 Tbck (ns)	Audio mode setting	EXTIN (MHz)
651.036	32fs	18.432
325.518	64fs	
708.6168	32fs	16.9344
354.3084	64fs	
976.560	32fs	12.288
488.280	64fs	

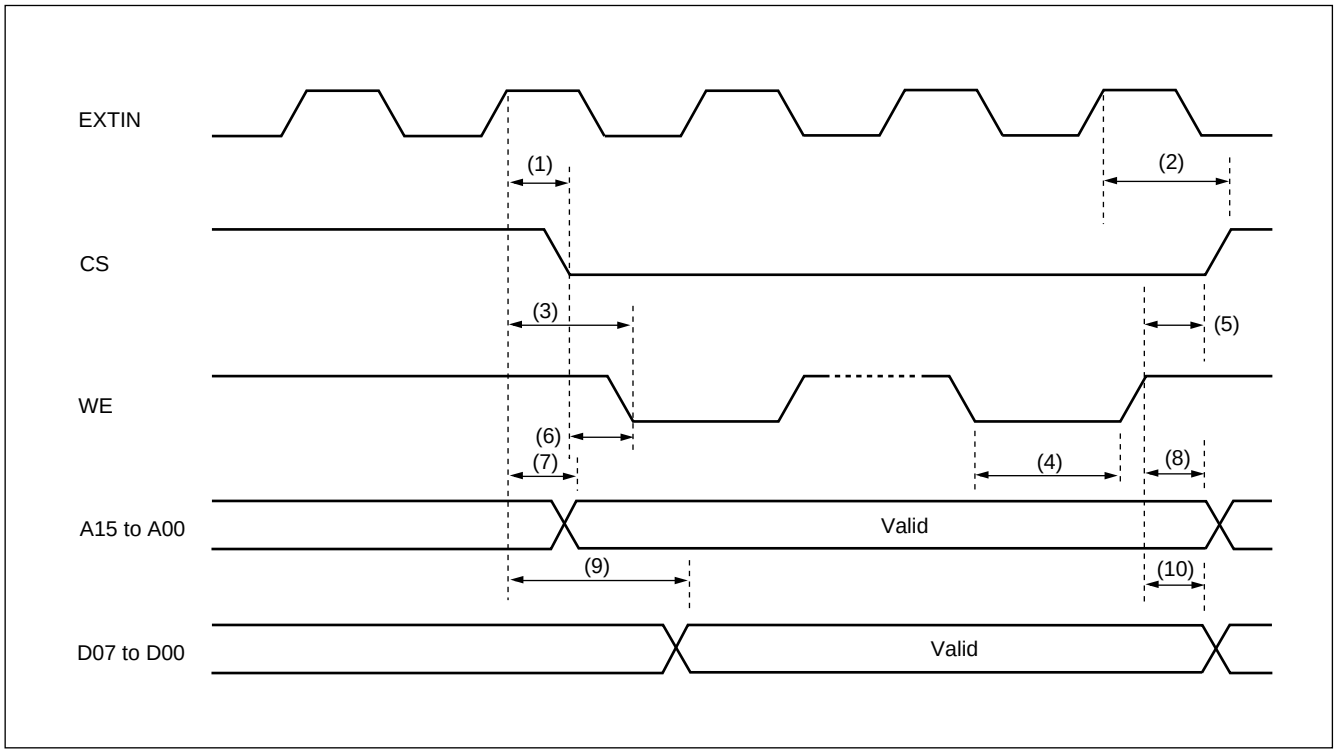
(6) LRCKI1, BCKI1, LRCKO, BCKO, SDO1 to 3 (Output Mode)



(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	BCKI1, BCKO fall delay time	—	—	11	ns
(2)	BCKI1, BCKO rise delay time	—	—	11	ns
(3)	LRCKI1, LRCKO fall delay time	—	—	5	ns
(4)	LRCKI1, LRCKO rise delay time	—	—	5	ns
(5)	SDO1 to 3 delay time	—	—	7	ns
(6)	SDO1 to 3 hold time	0.5	—	—	ns

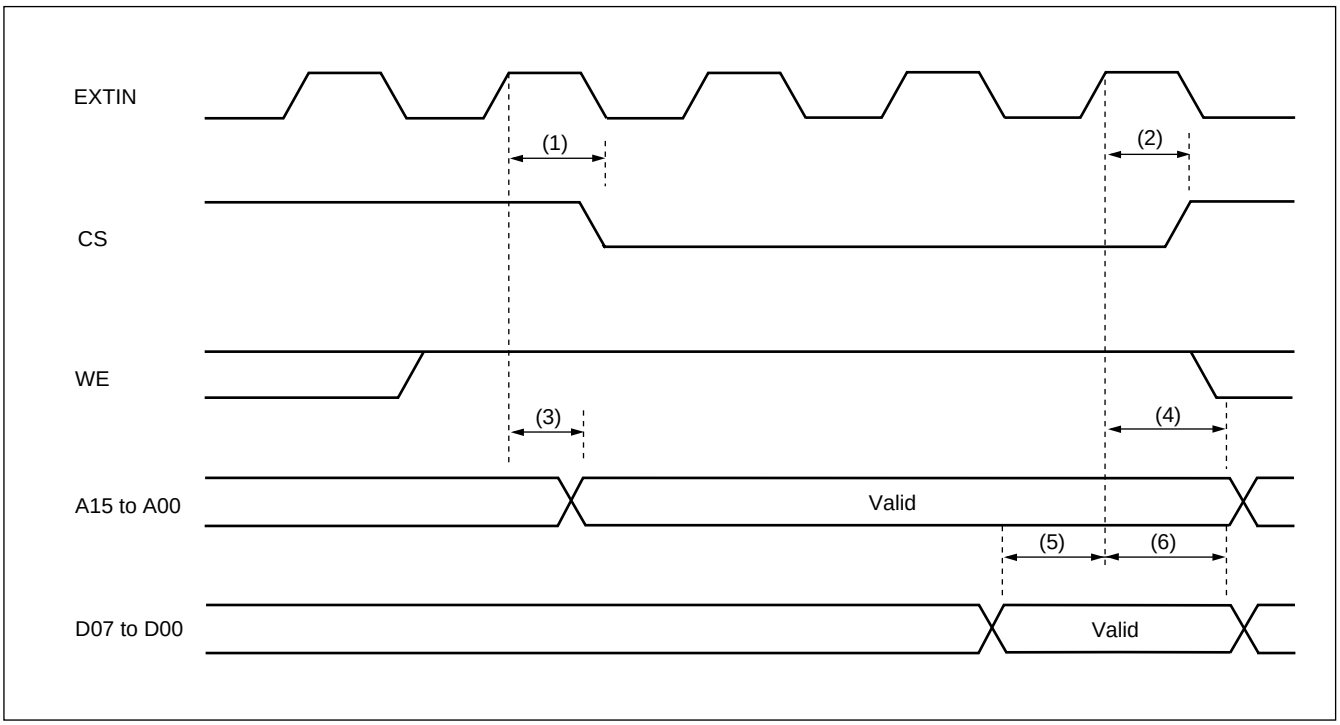
(7) CS, WE, A00 to 15, D00 to 07 (Data Write)



(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	CS delay time	—	—	20	ns
(2)	CS hold time	2	—	—	ns
(3)	WE delay time	—	—	22	ns
(4)	WE “H” pulse width	8	—	—	ns
(5)	WE hold time	2	—	—	ns
(6)	WE setup time	0.7	—	—	ns
(7)	A00 to 15 delay time	—	—	20	ns
(8)	A00 to 15 hold time	2	—	—	ns
(9)	D00 to 07 delay time	—	—	22	ns
(10)	D00 to 07 hold time	2	—	5	ns

(8) CS, WE, A00 to 15, D00 to 07 (Data Read)

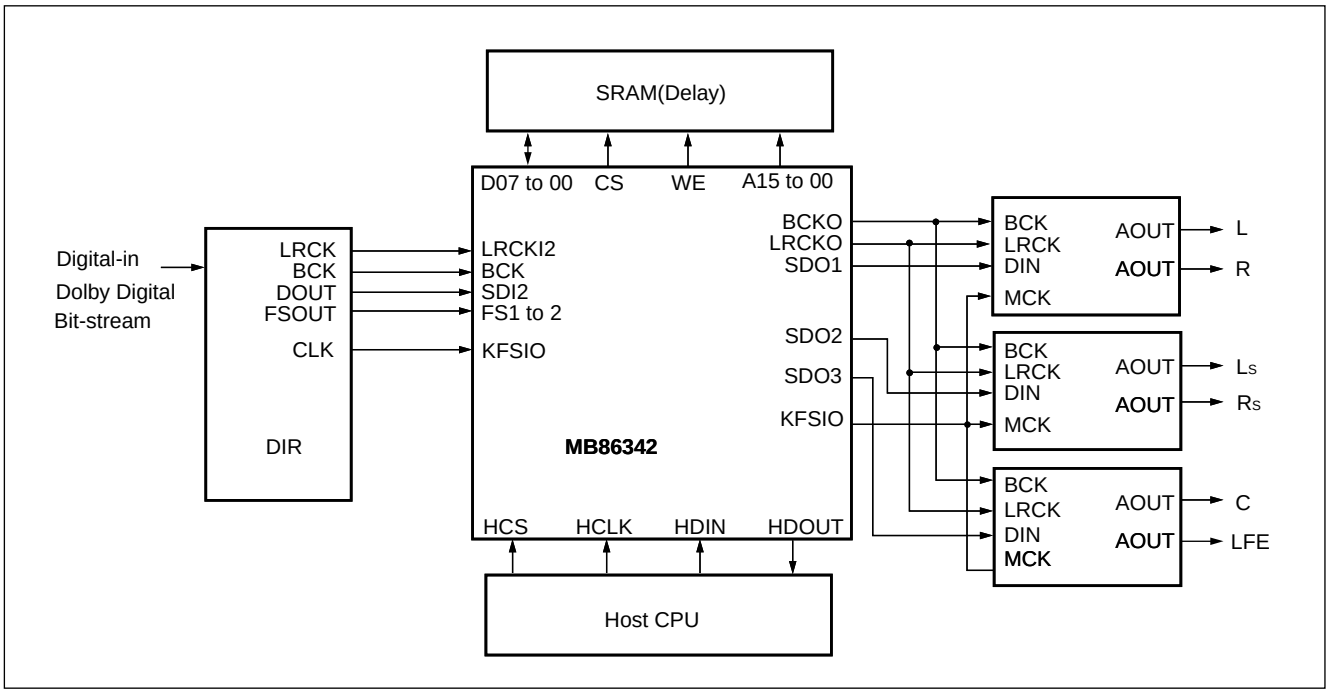


(V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, Ta = 0 to 70°C)

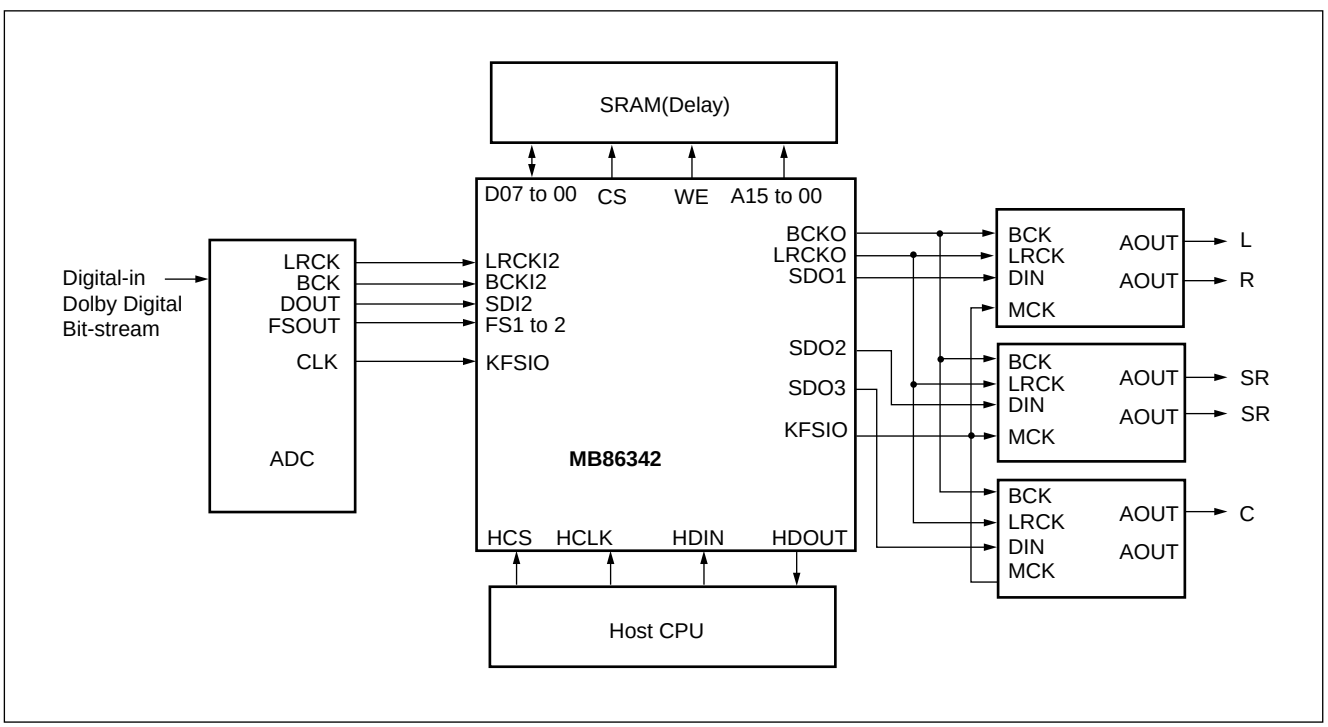
No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	CS delay time	—	—	20	ns
(2)	CS hold time	2	—	—	ns
(3)	A00 to 15 delay time	—	—	22	ns
(4)	A00 to 15 hold time	3	—	—	ns
(5)	D00 to 07 setup time	3	—	—	ns
(6)	D00 to 07 hold time	7	—	—	ns

■ SYSTEM CONSTRUCTION

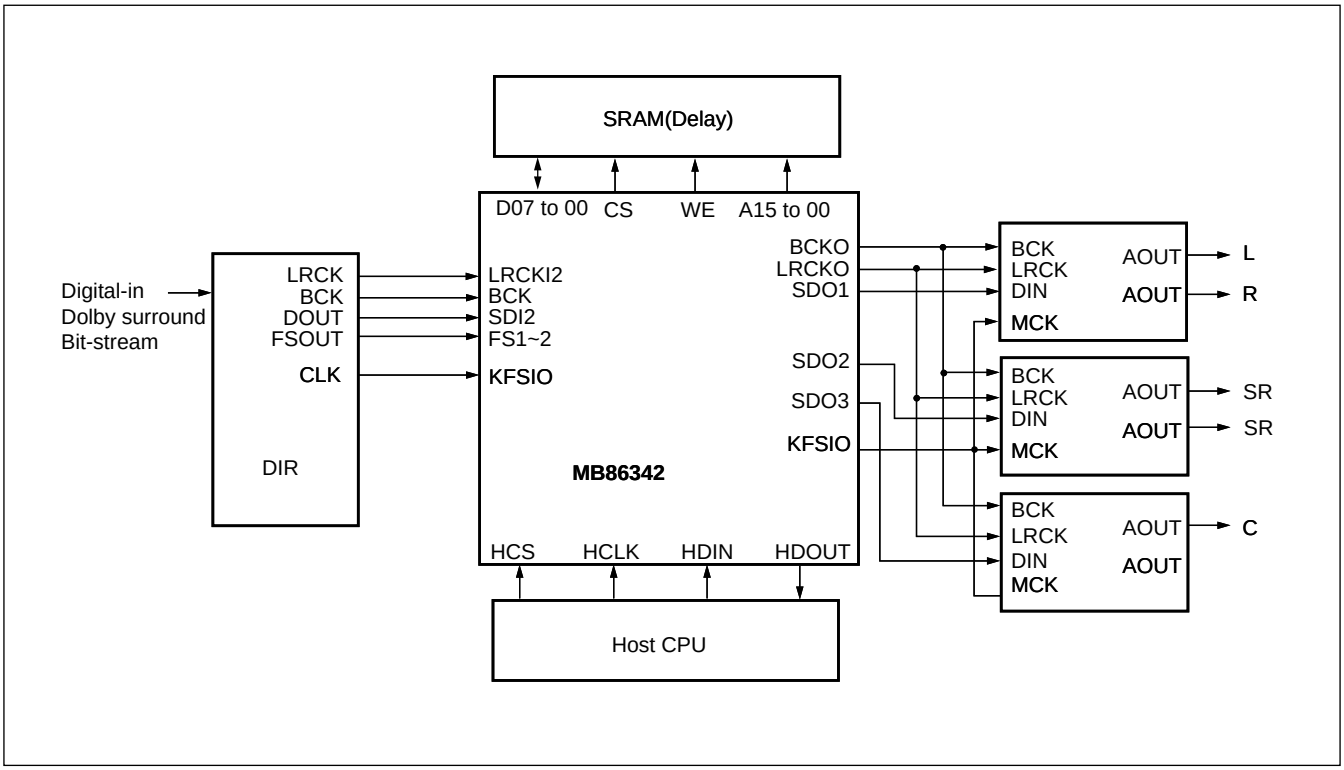
1. Dolby Digital Decoder (5.1 ch)



2. Dolby Pro Logic Decoder (4 ch)

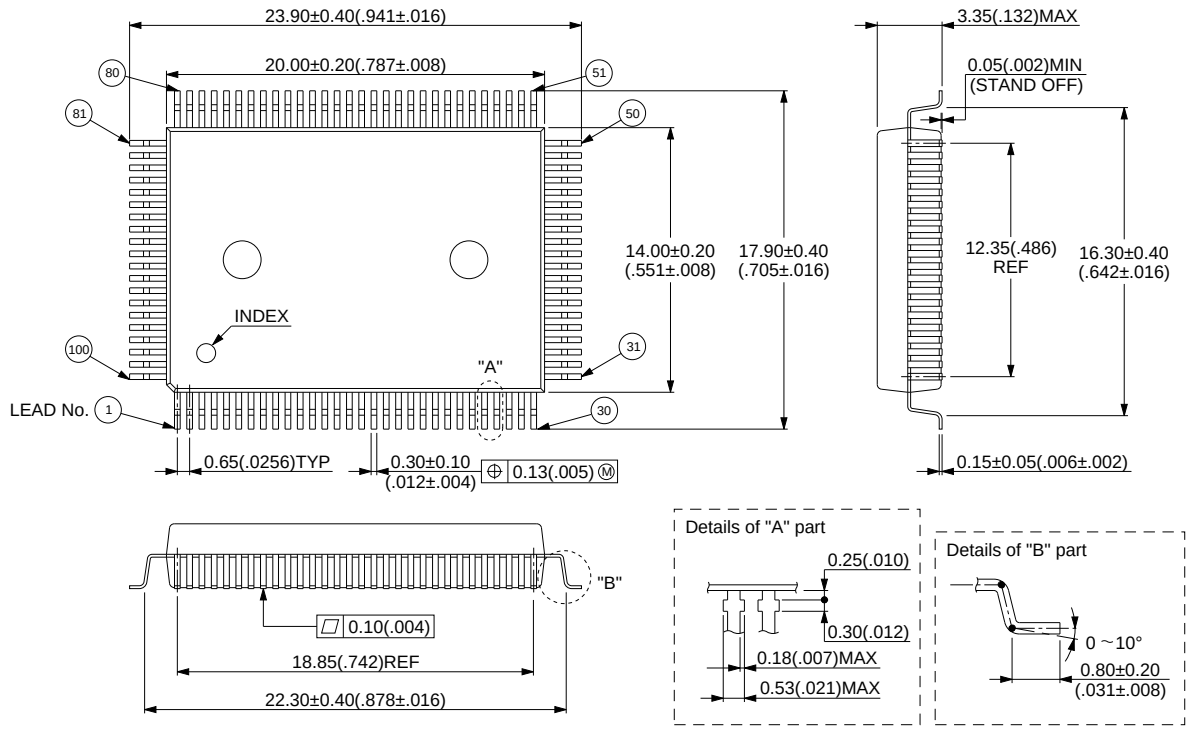


3. Dolby Digital + Dolby Pro Logic Decoder



■ PACKAGE DIMENSION

100 pin, Plastic QFP
(FPT-100P-M06)



Dimensions in mm (inch).

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