CONFIDENTIAL

ERRATA DOCUMENT

CYDxxS36V18
CYDxxS18V18

Errata Revision: **

March 15, 2006

Errata Document for CYDxxS36V18/CYDxxS18V18 18-Mb/9-Mb/4-Mb x36/x18 FullFlex™ Dual-Ports

This document describes the errata for the 18Mb/9Mb/4Mb x36/x18 FullFlex™ Dual-Ports (CYDxxS36V18/CYDxxS18V18). Details include errata trigger conditions, available workarounds, and silicon revision applicability. This document should be used to compare to the data sheet for this device to fully describe the device functionality. Please contact your local Cypress Sales Representative if you have further questions.

Part Numbers Affected

Part Number	Package	Device Characteristics	Product Status
CYD18S36V18	256-Ball FBGA	All speed grades	Sampling
CYD09S36V18	256-Ball FBGA	All speed grades	Sampling
CYD04S36V18	256-Ball FBGA	All speed grades	Sampling
CYD18S18V18	256-Ball FBGA	All speed grades	Sampling
CYD09S18V18	256-Ball FBGA	All speed grades	Sampling
CYD04S18V18	256-Ball FBGA	All speed grades	Sampling

18-Mb/9-Mb/4-Mb x36/x18 FullFlex Dual-Ports Errata Summary

The ZQ0 and ZQ1 pins on both ports (left and right) are internally shorted in the 256-Ball FBGA package substrate design. This creates an error in the Variable Impedance Matching (VIM) feature on the FullFlex Dual-Ports, as the effective output driver impedance is halved when both resistors are populated. The workaround is to remove the resistors on ZQ1L and ZQ1R for the affected devices.

Variable Impedance Matching (VIM)

- PROBLEM DEFINITION

  The 256-Ball FBGA package substrate design has the ZQ0L pin shorted to ZQ1L and ZQ0R shorted to ZQ1R. The ZQ1L and ZQ1R pins are not internally connected to the die for the affected devices; therefore, when resistors are connected to these pins to ground, the effective output driver impedance for each port is halved.
- PARAMETERS AFFECTED

  Effective output driver impedance controlled by the VIM circuitry.
- TRIGGER CONDITION(S)

  If the designer populates resistors for both ZQ0 and ZQ1, the short between ZQ0 and ZQ1 halves the effective impedance seen by the VIM calibrating circuitry.
- SCOPE OF IMPACT

  Output driver impedance is halved, as the two VIM calibrating resistors are in parallel to ground.
- WORKAROUND

  Remove ZQ1L and ZQ1R VIM resistors. Disconnecting these two resistors and leaving the pins open allow the calibrating circuitry to set the correct output driver impedance.
- FIX STATUS

  The date for the substrate design fix is TBD.

References

1. Document # 38-06072, FullFlex Synchronous DDR Dual-Port SRAM
2. Document # 38-06082, FullFlex Synchronous SDR Dual-Port SRAM

Document History Page

Document Title: Errata Document for CYDxxS36V18/CYDxxS18V18 18-Mb/9-Mb/4-Mb x36/x18 FullFlex™ Dual-Ports Document Number: 001-07077				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	435564	See ECN	YDT	Original release of spec