MCP3002

2.7V Dual Channel 10-Bit A/D Converter with SPI™ Serial Interface

Features

- 10-bit resolution
- ±1 LSB max DNL
- ±1 LSB max INL
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI™ serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 200 ksps max sampling rate at V_{DD} = 5V
- 75 ksps max sampling rate at V_{DD} = 2.7V
- Low power CMOS technology:
  - 5 nA typical standby current, 2 µA max
  - 550 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin MSOP, PDIP, SOIC and TSSOP packages

Applications

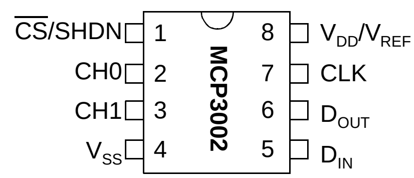
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

Description

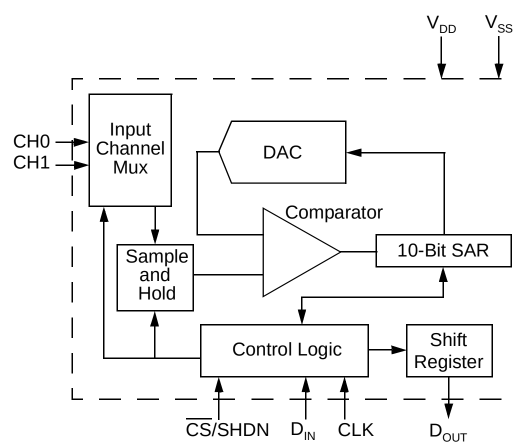
The Microchip Technology Inc. MCP3002 is a successive approximation 10-bit Analog-to-Digital (A/D) Converter with on-board sample and hold circuitry. The MCP3002 is programmable to provide a single pseudo-differential input pair or dual single-ended inputs. Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) are both specified at ±1 LSB. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of conversion rates of up to 200 ksps at 5V and 75 ksps at 2.7V. The MCP3002 device operates over a broad voltage range (2.7V - 5.5V). Low current design permits operation with a typical standby current of 5 nA and a typical active current of 375 µA. The MCP3002 is offered in 8-pin MSOP, PDIP, TSSOP and 150 mil SOIC packages.

Package Types

MSOP, PDIP, SOIC, TSSOP



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD} 7.0V
All inputs and outputs w.r.t. V_{SS} ...... -0.6V to V_{DD} +0.6V
Storage temperature .... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
ESD protection on all pins (HBM)....................... > 4kV

*Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{DD}/V_{REF}	+2.7V to 5.5V Power Supply and Reference Voltage Input
CH0	Channel 0 Analog Input
CH1	Channel 1 Analog Input
CLK	Serial Clock
D_{IN}	Serial Data In
D_{OUT}	Serial Data Out
$\overline{CS}$/SHDN	$\overline{\text{Chip Select}}$/Shutdown Input

ELECTRICAL CHARACTERISTICS

All parameters apply at V_{DD} = 5V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 200 ksps and f_{CLK} = 16*f_{SAMPLE} unless otherwise noted. Typical values apply for V_{DD} = 5V, T_{AMB} = 25°C unless otherwise noted.

PARAMETER	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Conversion Rate:						
Conversion Time	t_{CONV}	—	—	10	clock cycles	
Analog Input Sample Time	t_{SAMPLE}		1.5		clock cycles	
Throughput Rate	f_{SAMPLE}	—	—	200 75	ksps ksps	V_{DD} = 5V V_{DD} = 2.7V
DC Accuracy:						
Resolution			10		bits	
Integral Nonlinearity	INL	—	±0.5	±1	LSB	
Differential Nonlinearity	DNL	—	±0.25	±1	LSB	No missing codes over temperature
Offset Error		—	—	±1.5	LSB	
Gain Error		—	—	±1	LSB	
Dynamic Performance:						
Total Harmonic Distortion	THD	—	-76	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Signal to Noise and Distortion (SINAD)	SINAD	—	61	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Spurious Free Dynamic Range	SFDR	—	78	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Analog Inputs:						
Input Voltage Range for CH0 or CH1 in Single-Ended Mode		V_{SS}	—	V_{DD}	V	
Input Voltage Range for IN+ In pseudo-differential Mode	IN+	IN-	—	V_{DD}+IN-		
Input Voltage Range for IN- In pseudo-differential Mode	IN-	V_{SS}-100	—	V_{SS}+100	mV	
Leakage Current		—	0.001	±1	µA	
Switch Resistance	R_{SS}	—	1K	—	Ω	See Figure 4-1
Sample Capacitor	C_{SAMPLE}	—	20	—	pF	See Figure 4-1

Note 1: This parameter is established by characterization and not 100% tested.
2: The sample cap will eventually lose charge, especially at elevated temperatures, therefore f_{CLK} ≥10 kHz for temperatures at or above 70°C.

ELECTRICAL CHARACTERISTICS (CONTINUED)

All parameters apply at V_{DD} = 5V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 200 ksps and f_{CLK} = 16*f_{SAMPLE} unless otherwise noted. Typical values apply for V_{DD} = 5V, T_{AMB} = 25°C unless otherwise noted.

PARAMETER	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Digital Input/Output:						
Data Coding Format			Straight Binary			
High Level Input Voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Low Level Input Voltage	V_{IL}	—	—	0.3 V_{DD}	V	
High Level Output Voltage	V_{OH}	4.1	—	—	V	I_{OH} = -1 mA, V_{DD} = 4.5V
Low Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1 mA, V_{DD} = 4.5V
Input Leakage Current	I_{LI}	-10	—	10	µA	V_{IN} = V_{SS} or V_{DD}
Output Leakage Current	I_{LO}	-10	—	10	µA	V_{OUT} = V_{SS} or V_{DD}
Pin Capacitance (All Inputs/Outputs)	C_{IN}, C_{OUT}	—	—	10	pF	V_{DD} = 5.0V (**Note 1**) T_{AMB} = 25°C, f = 1 MHz
Timing Parameters:						
Clock Frequency	f_{CLK}	— —	— —	3.2 1.2	MHz MHz	V_{DD} = 5V (**Note 2**) V_{DD} = 2.7V (**Note 2**)
Clock High Time	t_{HI}	140	—	—	ns	
Clock Low Time	t_{LO}	140	—	—	ns	
$\overline{CS}$ Fall To First Rising CLK Edge	t_{SUCS}	100	—	—	ns	
Data Input Setup Time	t_{SU}	—	—	50	ns	
Data Input Hold Time	t_{HD}	—	—	50	ns	
CLK Fall To Output Data Valid	t_{DO}	— —	— —	125 200	ns ns	V_{DD} = 5V, see Figure 1-2 V_{DD} = 2.7V, see Figure 1-2
CLK Fall To Output Enable	t_{EN}	—	—	125 200	ns ns	V_{DD} = 5V, see Figure 1-2 V_{DD} = 2.7V, see Figure 1-2
$\overline{CS}$ Rise To Output Disable	t_{DIS}	—	—	100	ns	See Test Circuits, Figure 1-2 **Note 1**
$\overline{CS}$ Disable Time	t_{CSH}	310	—	—	ns	
D_{OUT} Rise Time	t_R	—	—	100	ns	See Test Circuits, Figure 1-2 **Note 1**
D_{OUT} Fall Time	t_F	—	—	100	ns	See Test Circuits, Figure 1-2 **Note 1**
Power Requirements:						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	— —	525 300	650 —	µA	V_{DD} = 5.0V, D_{OUT} unloaded V_{DD} = 2.7V, D_{OUT} unloaded
Standby Current	I_{DDS}	—	0.005	2	µA	$\overline{CS}$ = V_{DD} = 5.0V
Temperature Ranges:						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistance:						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	

Note 1: This parameter is established by characterization and not 100% tested.

2: The sample cap will eventually lose charge, especially at elevated temperatures, therefore f_{CLK} ≥10 kHz for temperatures at or above 70°C.

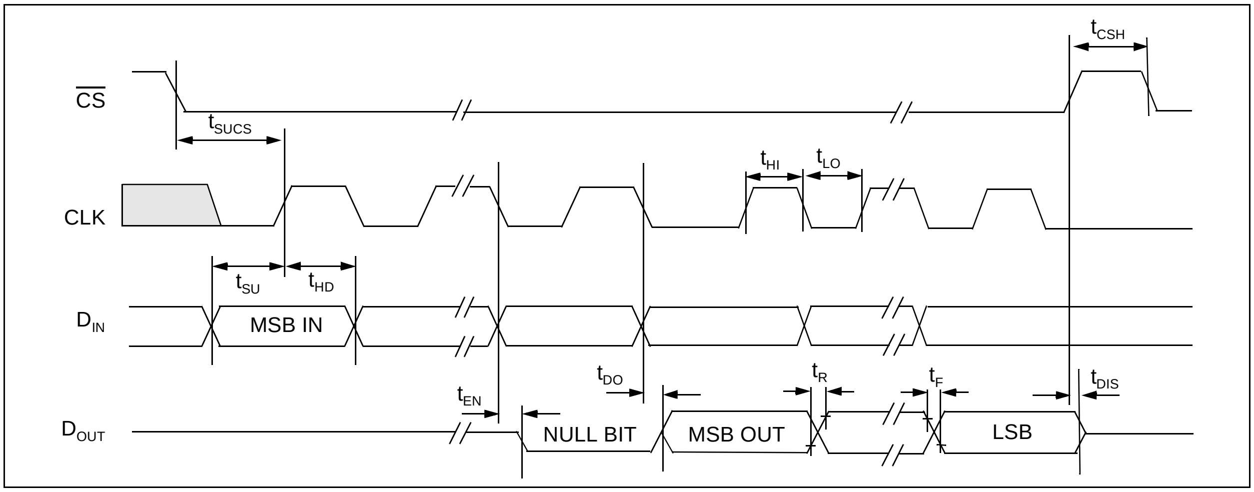
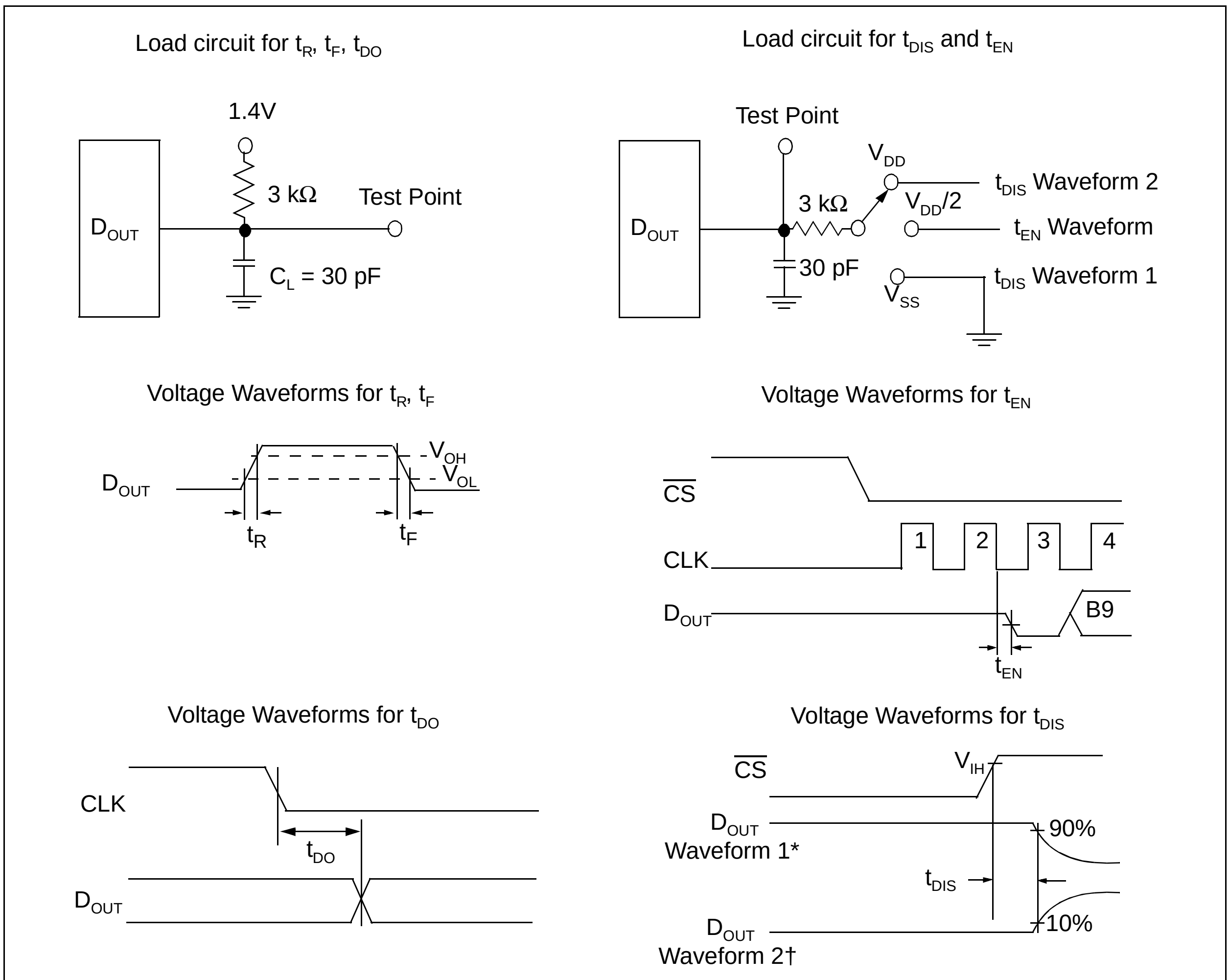


FIGURE 1-1: *Serial Timing.*



* Waveform 1 is for an output with internal conditions such that the output is high, unless disabled by the output control.

† Waveform 2 is for an output with internal conditions such that the output is low, unless disabled by the output control.

FIGURE 1-2: *Test Circuits.*

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 5V, f_{SAMPLE} = 200 ksps, f_{CLK} = 16* f_{SAMPLE}, T_A = 25°C

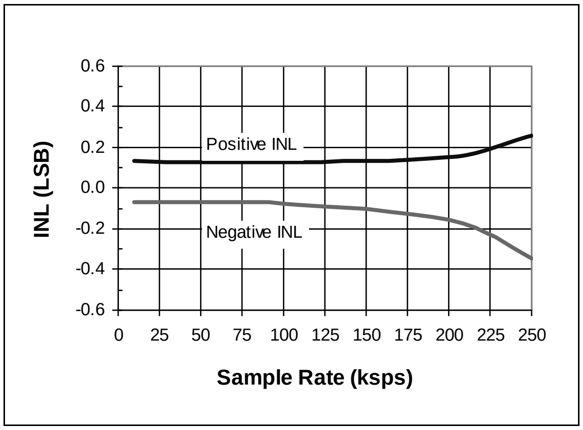


FIGURE 2-1: *Integral Nonlinearity (INL) vs. Sample Rate.*

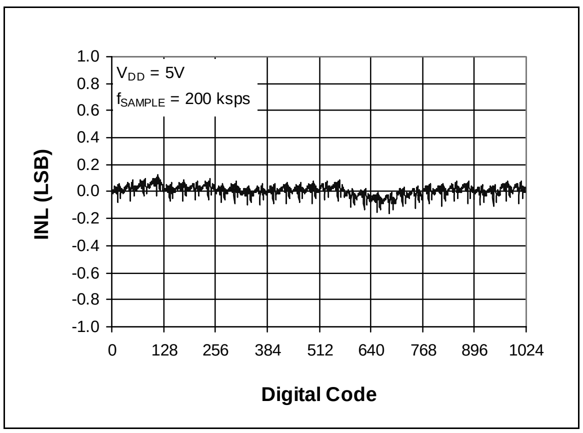


FIGURE 2-2: *Integral Nonlinearity (INL) vs. Code.*

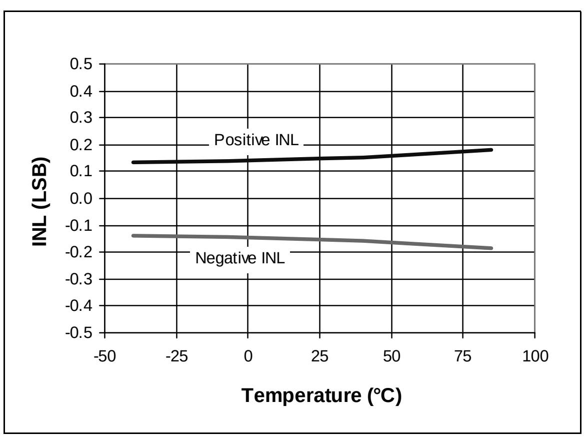


FIGURE 2-3: *Integral Nonlinearity (INL) vs. Temperature.*

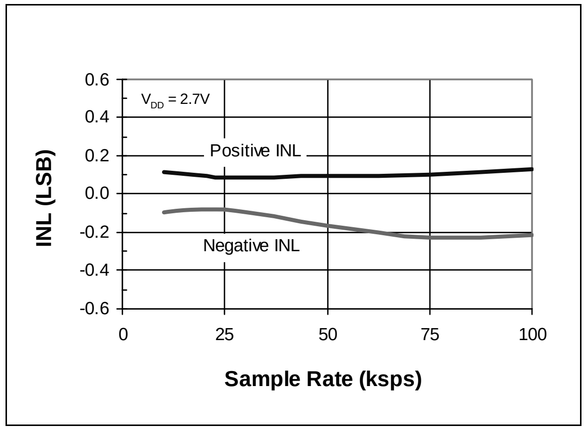


FIGURE 2-4: *Integral Nonlinearity (INL) vs. Sample Rate (V_{DD} = 2.7V).*

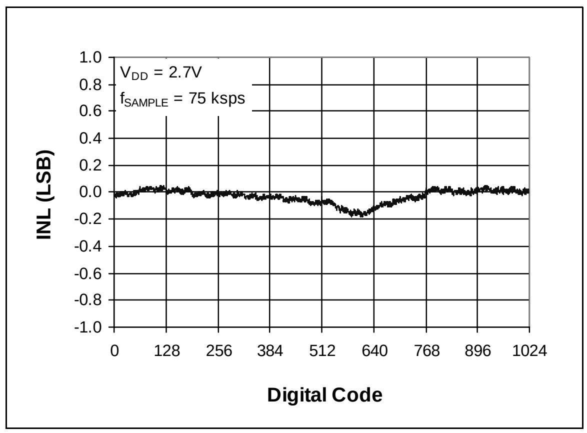


FIGURE 2-5: *Integral Nonlinearity (INL) vs. Code (V_{DD} = 2.7V).*

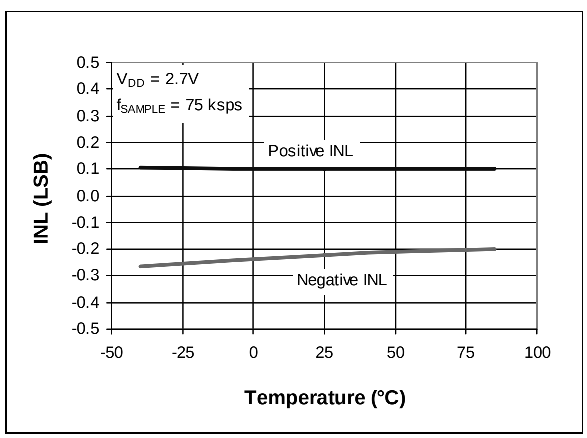


FIGURE 2-6: *Integral Nonlinearity (INL) vs. Temperature (V_{DD} = 2.7V).*

Note: Unless otherwise indicated, V_{DD} = 5V, f_{SAMPLE} = 200 ksps, f_{CLK} = 16* f_{SAMPLE},T_A = 25°C

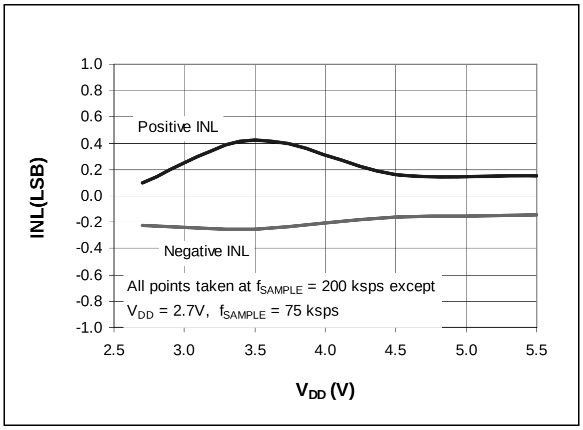


FIGURE 2-7: *Integral Nonlinearity (INL) vs. V_{DD}.*

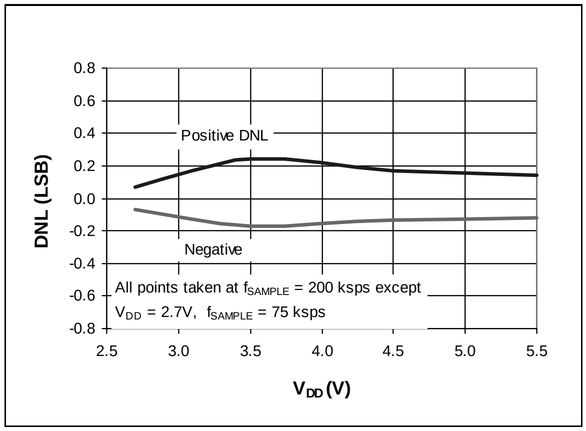


FIGURE 2-10: *Differential Nonlinearity (DNL) vs. V_{DD}.*

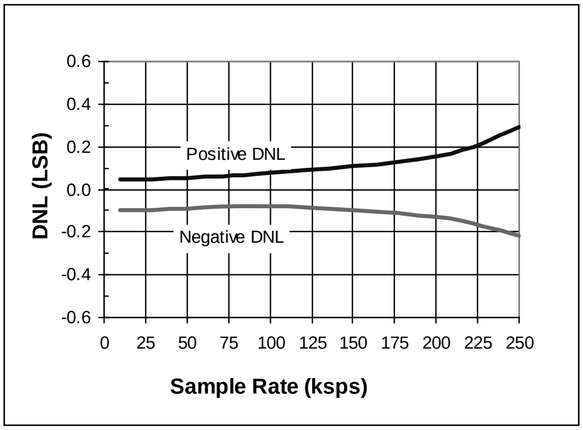


FIGURE 2-8: *Differential Nonlinearity (DNL) vs. Sample Rate.*

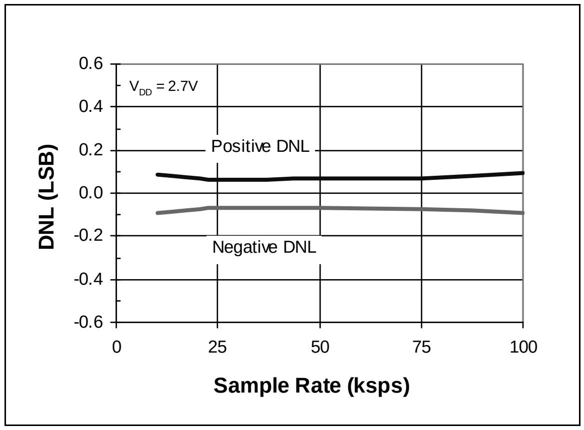


FIGURE 2-11: *Differential Nonlinearity (DNL) vs. Sample Rate (V_{DD} = 2.7V).*

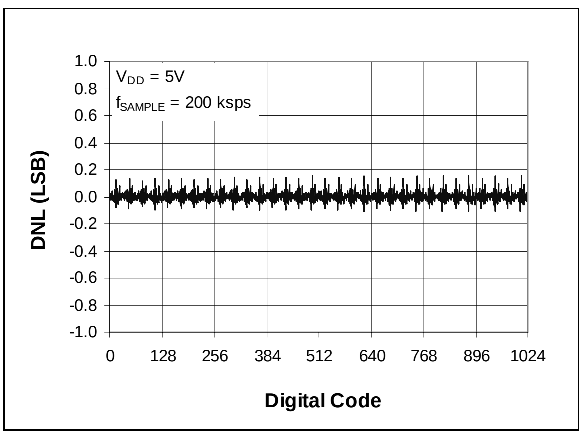


FIGURE 2-9: *Differential Nonlinearity (DNL) vs. Code (Representative Part).*

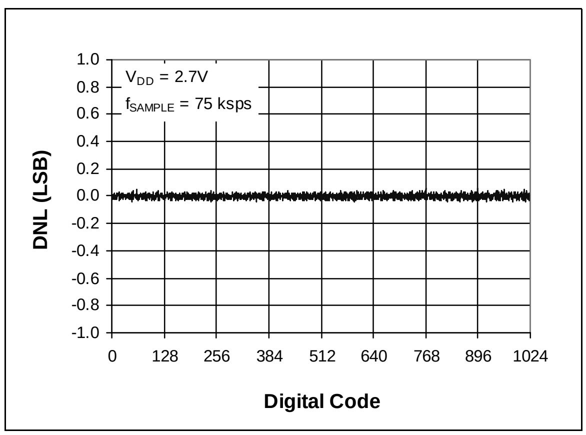


FIGURE 2-12: *Differential Nonlinearity (DNL) vs. Code (Representative Part, V_{DD} = 2.7V).*

Note: Unless otherwise indicated, V_{DD} = 5V, f_{SAMPLE} = 200 ksps, f_{CLK} = 16* f_{SAMPLE}, T_A = 25°C

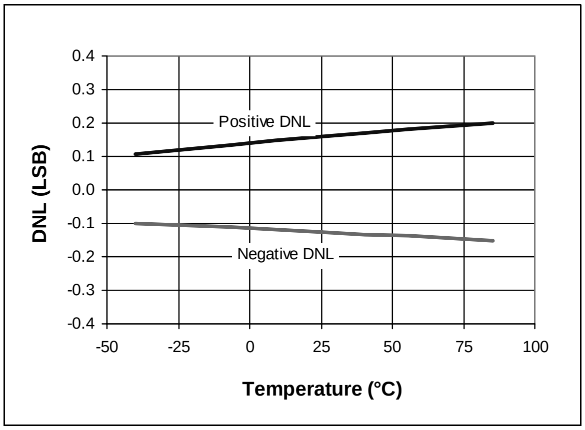


FIGURE 2-13: *Differential Nonlinearity (DNL) vs. Temperature.*

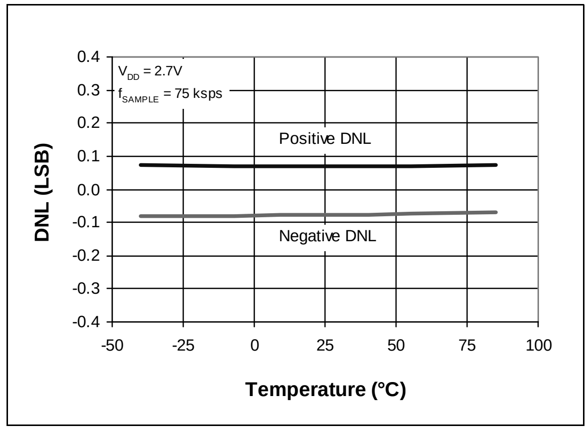


FIGURE 2-16: *Differential Nonlinearity (DNL) vs. Temperature (V_{DD} = 2.7V).*

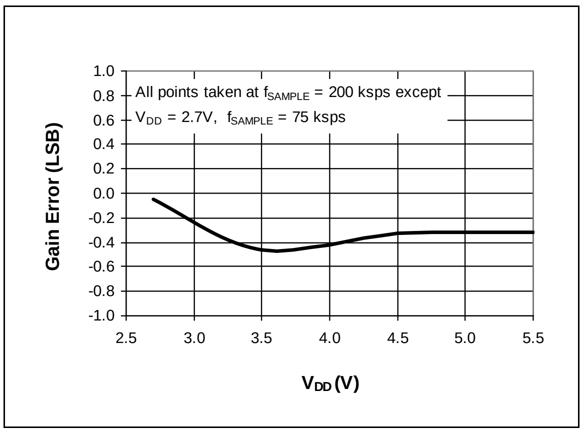


FIGURE 2-14: *Gain Error vs. V_{DD}.*

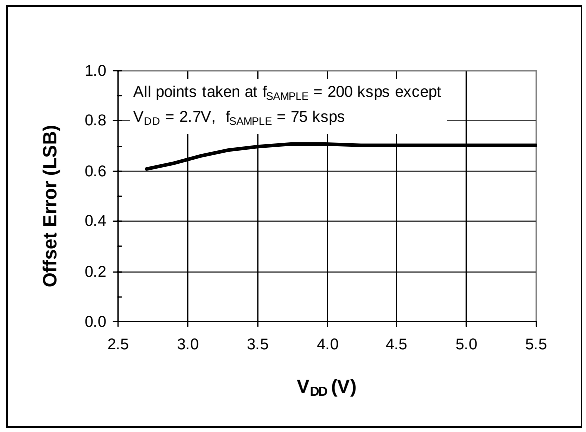


FIGURE 2-17: *Offset Error vs. V_{DD}.*

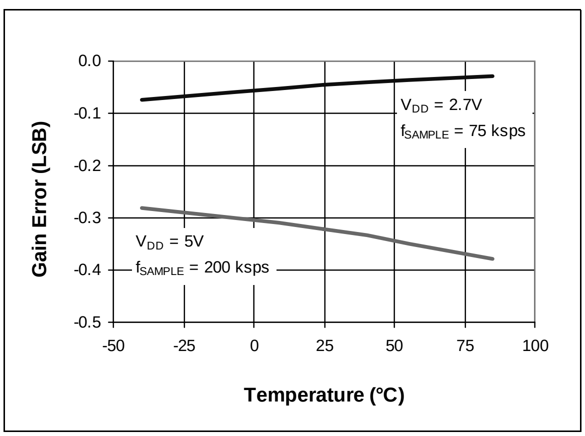


FIGURE 2-15: *Gain Error vs. Temperature.*

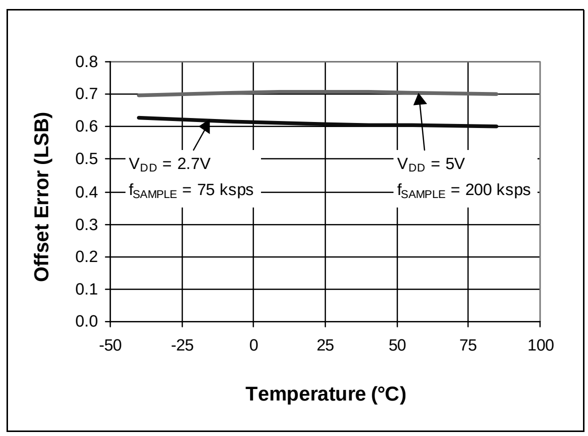


FIGURE 2-18: *Offset Error vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = 5V, f_{SAMPLE} = 200 ksps, f_{CLK} = 16* f_{SAMPLE}, T_A = 25°C

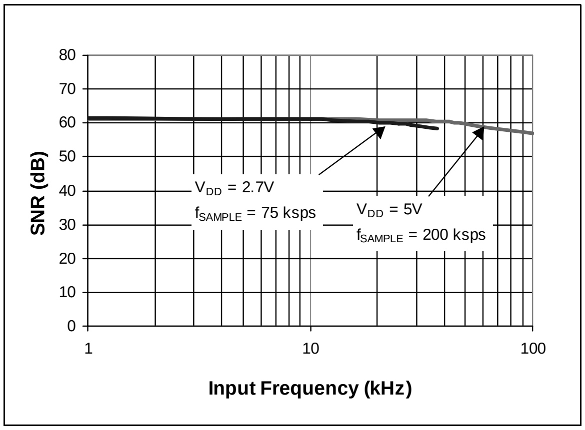


FIGURE 2-19: *Signal to Noise Ratio (SNR) vs. Input Frequency.*

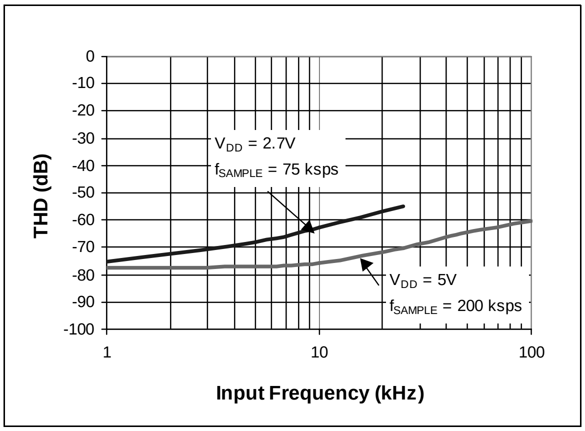


FIGURE 2-20: *Total Harmonic Distortion (THD) vs. Input Frequency.*

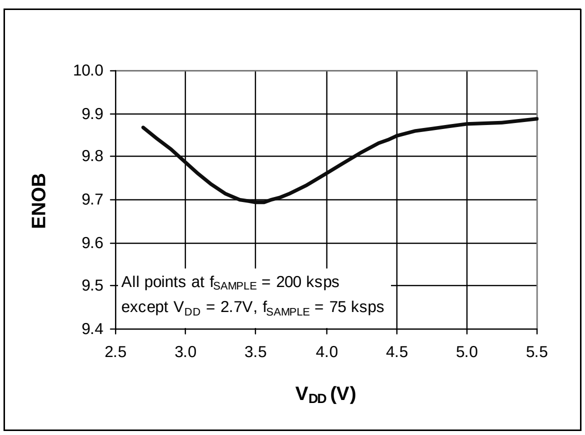


FIGURE 2-21: *Effective number of bits (ENOB) vs. V_{DD}.*

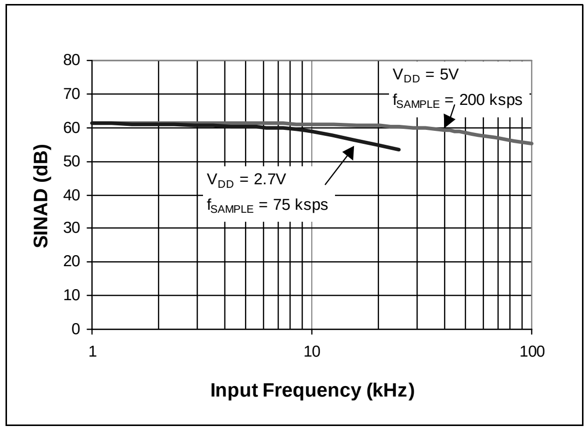


FIGURE 2-22: *Signal to Noise and Distortion (SINAD) vs. Input Frequency.*

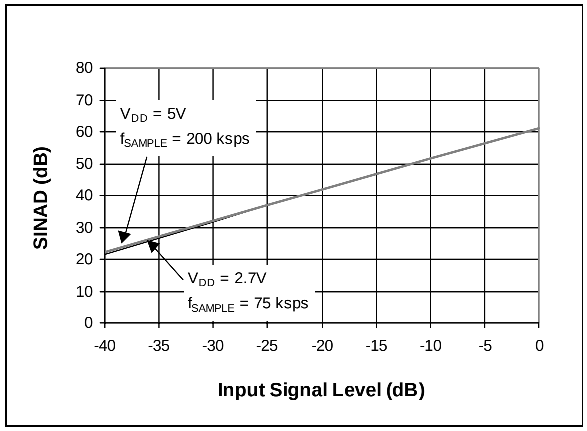


FIGURE 2-23: *Signal to Noise and Distortion (SINAD) vs. Signal Level.*

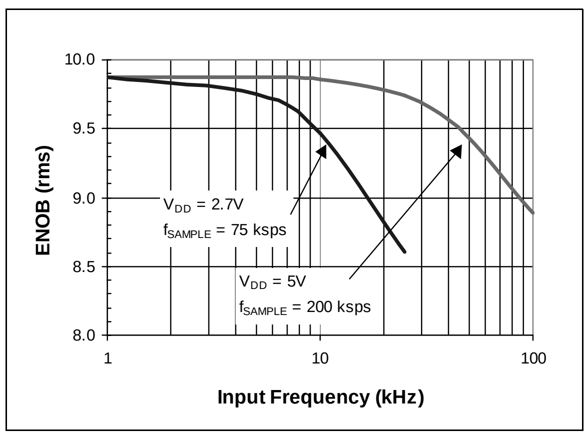


FIGURE 2-24: *Effective Number of Bits (ENOB) vs. Input Frequency.*

Note: Unless otherwise indicated, V_{DD} = 5V, f_{SAMPLE} = 200 ksps, f_{CLK} = 16* f_{SAMPLE}, T_A = 25°C

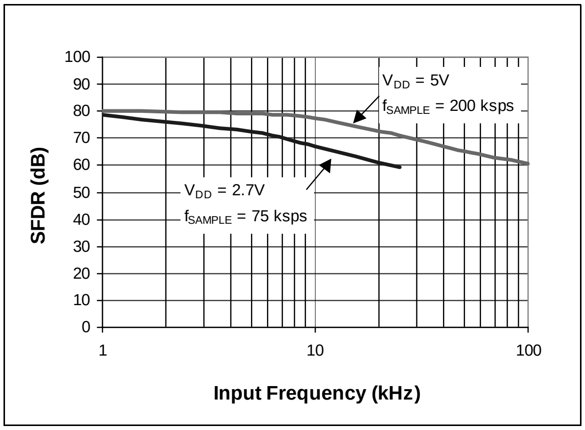


FIGURE 2-25: *Spurious Free Dynamic Range (SFDR) vs. Input Frequency.*

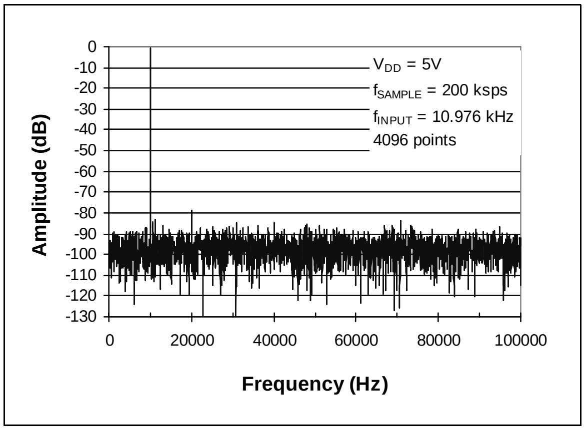


FIGURE 2-26: *Frequency Spectrum of 10 kHz input (Representative Part).*

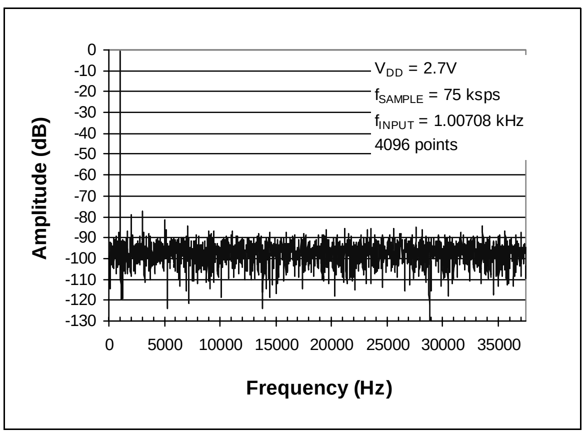


FIGURE 2-27: *Frequency Spectrum of 1 kHz input (Representative Part, V_{DD} = 2.7V).*

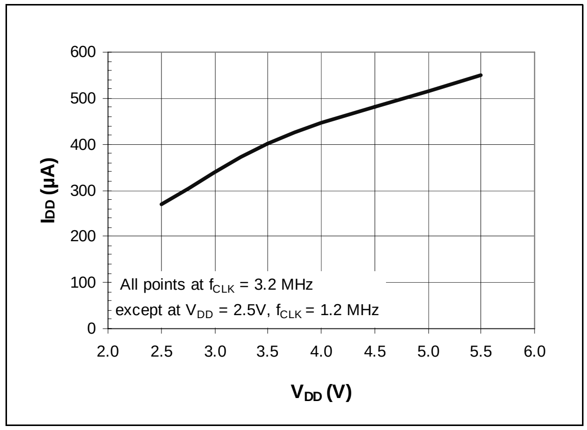


FIGURE 2-28: *I_{DD} vs. V_{DD}.*

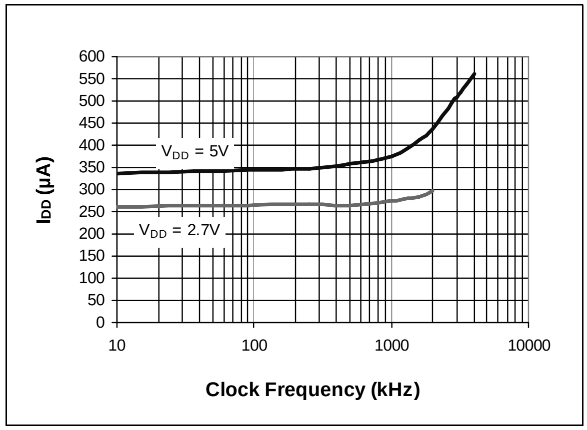


FIGURE 2-29: *I_{DD} vs. Clock Frequency.*

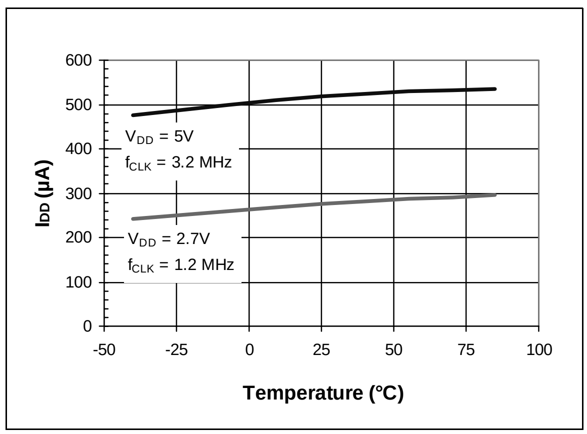


FIGURE 2-30: *I_{DD} vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = 5V, f_{SAMPLE} = 200 ksps, f_{CLK} = 16* f_{SAMPLE}, T_A = 25°C

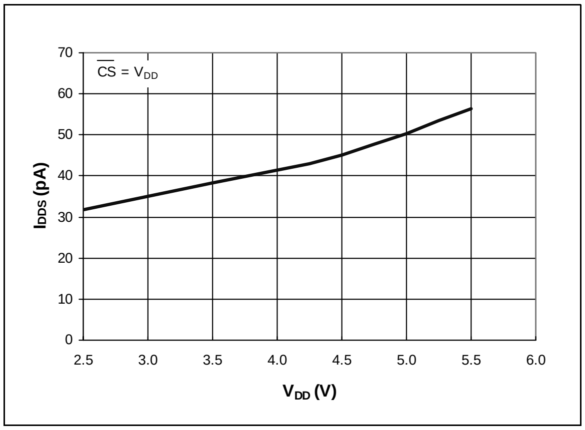


FIGURE 2-31: *I_{DDS} vs. V_{DD}.*

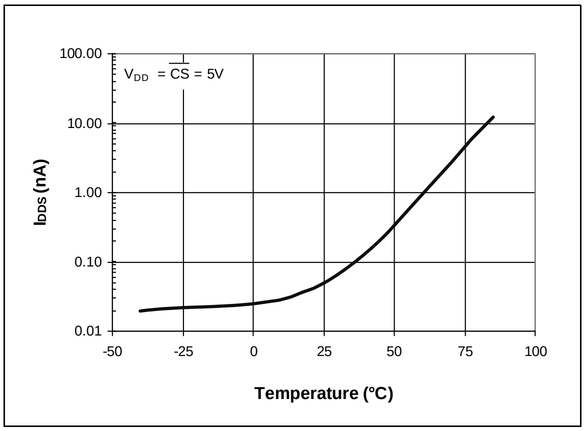


FIGURE 2-32: *I_{DDS} vs. Temperature.*

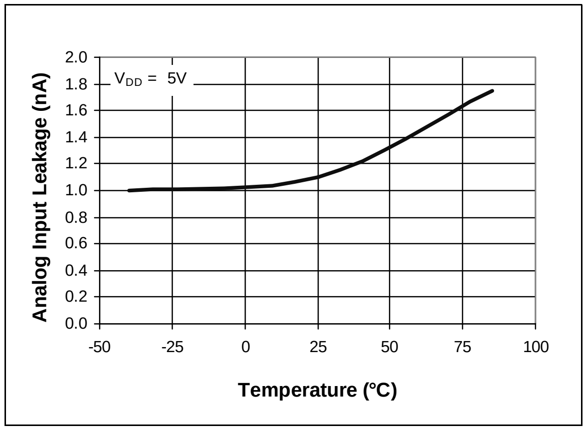


FIGURE 2-33: *Analog Input leakage current vs. Temperature.*

3.0 PIN DESCRIPTIONS

3.1 CH0/CH1

Analog inputs for channels 0 and 1 respectively. These channels can programmed to be used as two independent channels in single ended-mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See Section 5.0 for information on programming the channel configuration.

3.2 Chip Select/Shutdown ($\overline{CS}$/$\overline{SHDN}$)

The $\overline{CS}$/SHDN pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The $\overline{CS}$/SHDN pin must be pulled high between conversions.

3.3 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

3.4 Serial Data Input (D_{IN})

The SPI port serial data input pin is used to clock in input channel configuration data.

3.5 Serial Data Output (D_{OUT})

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

4.0 DEVICE OPERATION

The MCP3002 A/D converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the second rising edge of the serial clock after the start bit has been received. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 10-bit digital output code. Conversion rates of 200 ksps are possible on the MCP3002. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 3-wire SPI compatible interface.

4.1 Analog Inputs

The MCP3002 device offers the choice of using the analog input channels configured as two single-ended inputs that are referenced to V_{SS} or a single pseudo-differential input. The configuration setup is done as part of the serial command before each conversion begins. When used in the psuedo-differential mode, CH0 and CH1 are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to the reference voltage, V_{DD}. The IN- input is limited to ±100 mV from the V_{SS} rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D converter to meet specification, the charge holding capacitor (C_{SAMPLE}) must be given enough time to acquire a 10-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram, it is shown that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor, C_{SAMPLE}. Consequently, larger source impedances increase the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601 which has a closed loop output impedance of tens of ohms. The adverse affects of higher source impedances are shown in Figure 4-2.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than {[V_{DD} + (IN-)] - 1 LSB}, then the output code will be 3FFh. If the voltage level at IN- is more than 1 LSB below V_{SS}, then the voltage level at the IN+ input will have to go below V_{SS} to see the 000h output code. Conversely, if IN- is more than 1 LSB above V_{SS}, then the 3FFh code will not be seen unless the IN+ input level goes above V_{DD} level. If the voltage at IN+ is equal to or greater than {[V_{DD} + (IN-)] - 1 LSB}, then the output code will be 3FFh.

4.2 Digital Output Code

The digital output code produced by an A/D Converter is a function of the input signal and the reference voltage. For the MCP3002, V_{DD} is used as the reference voltage.

$$LSB\ Size = \frac{V_{REF}}{1024}$$

As the V_{DD} level is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is shown below.

$$Digital\ Output\ Code = \frac{1024 * V_{IN}}{V_{DD}}$$

where:

V_{IN} = *analog input voltage*

V_{DD} = *supply voltage*

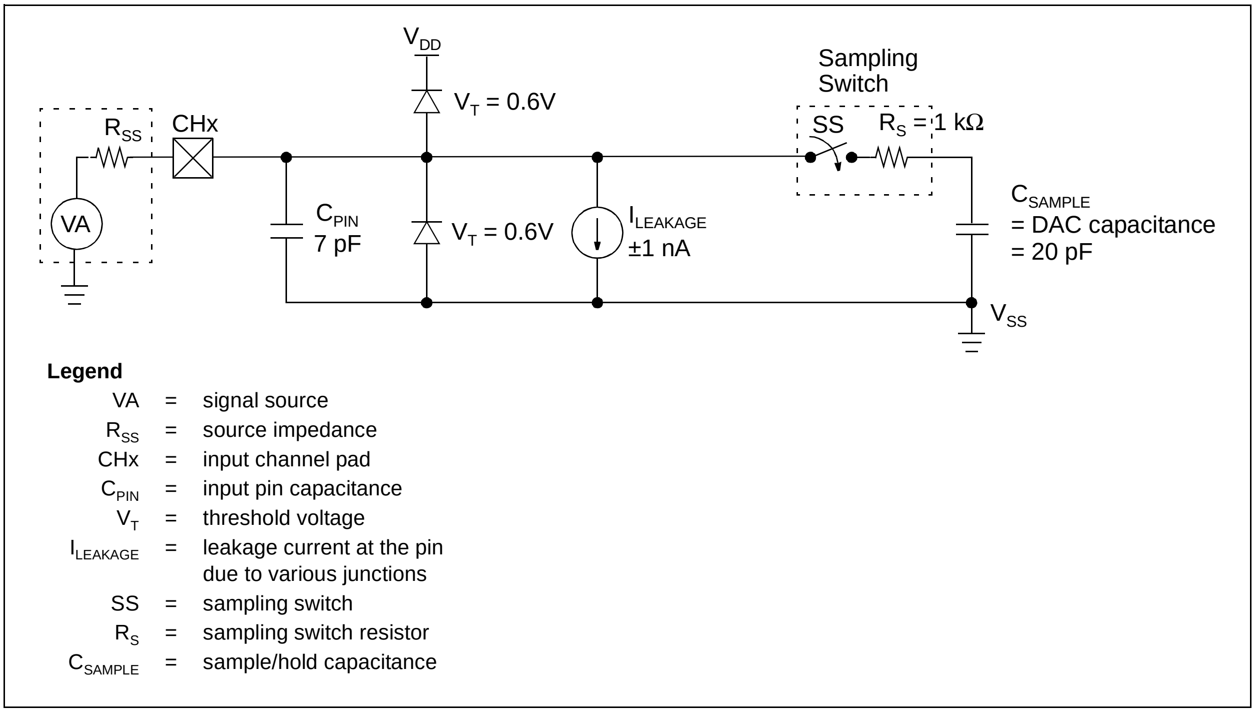


FIGURE 4-1: *Analog Input Model.*

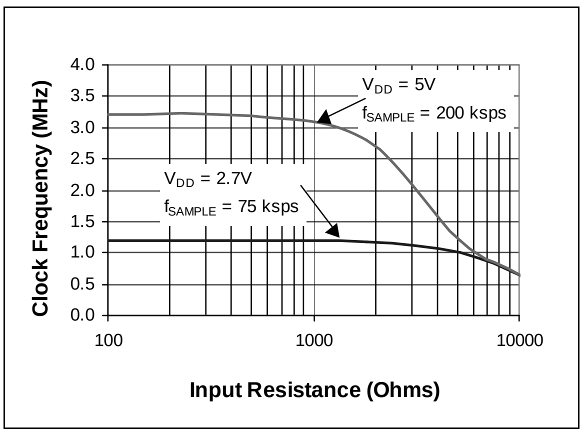


FIGURE 4-2: *Maximum Clock Frequency vs. Input resistance (R_S) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.*

5.0 SERIAL COMMUNICATIONS

5.1 Overview

Communication with the MCP3002 is done using a standard SPI-compatible serial interface. Initiating communication with the device is done by bringing the $\overline{CS}$ line low. See Figure 5-1. If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The first clock received with $\overline{CS}$ low and D_{IN} high will constitute a start bit. The SGL/$\overline{DIFF}$ bit and the ODD/$\overline{SIGN}$ bit follow the start bit and are used to select the input channel configuration. The SGL/$\overline{DIFF}$ is used to select single ended or psuedo-differential mode. The ODD/$\overline{SIGN}$ bit selects which channel is used in single ended mode, and is used to determine polarity in psuedo-differential mode. Following the ODD/$\overline{SIGN}$ bit, the MSBF bit is transmitted to and is used to enable the LSB first format for the device. If the MSBF bit is high, then the data will come from the device in MSB first format and any further clocks with $\overline{CS}$ low, will cause the device to output zeros. If the MSBF bit is low, then the device will output the converted word LSB first *after* the word has been transmitted in the MSB first format. Table 5-1 shows the configuration bits for the MCP3002. The device will begin to sample the analog input on the second rising edge of the clock, after the start bit has been received. The sample period will end on the falling edge of the third clock following the start bit.

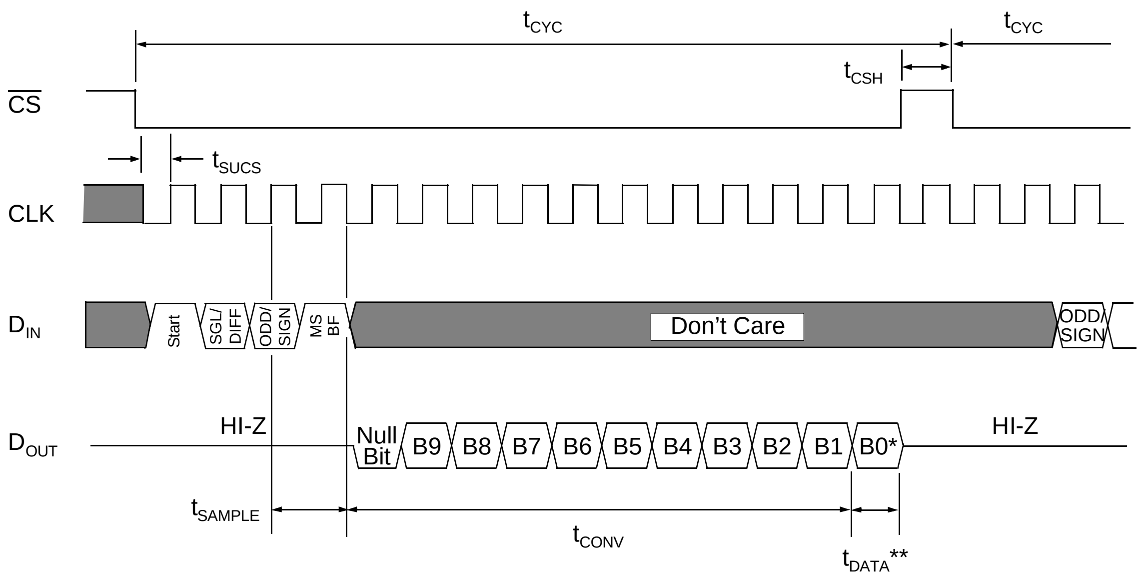
On the falling edge of the clock for the MSBF bit, the device will output a low null bit. The next sequential 10 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 10 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low (and the MSBF bit is high), the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring $\overline{CS}$ low and clock in leading zeros on the D_{IN} line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3002 devices with hardware SPI ports.

If it is desired, the $\overline{CS}$ can be raised to end the conversion period at any time during the transmission. Faster conversion rates can be obtained by using this technique if not all the bits are captured before starting a new cycle. Some system designers use this method by capturing only the highest order 8 bits and 'throwing away' the lower 2 bits.

TABLE 5-1: *Configuration Bits for the MCP3002.*

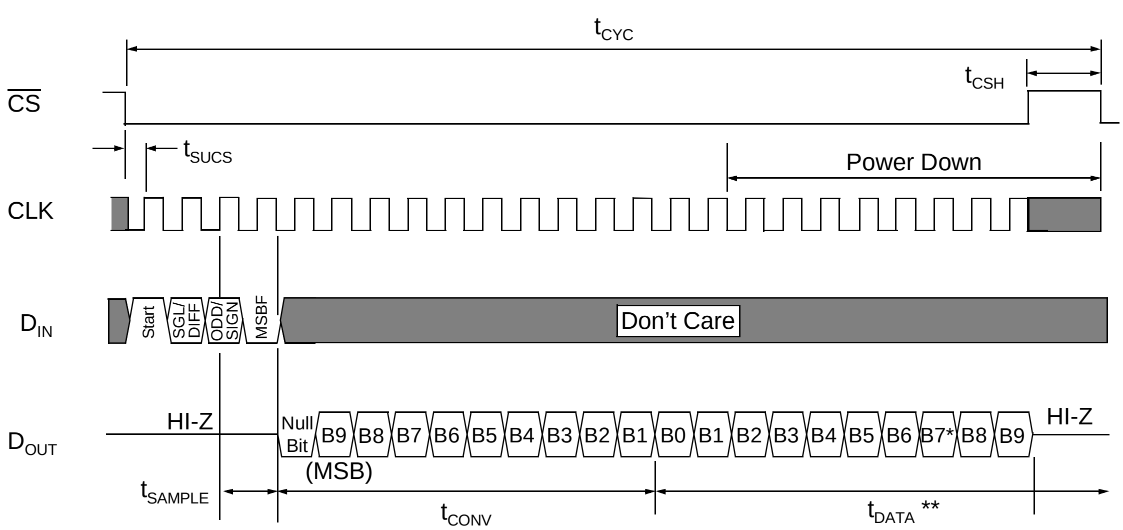
	CONFIG BITS		**CHANNEL SELECTION**		**GND**
	SGL/$\overline{DIFF}$	ODD/$\overline{SIGN}$	0	1	
SINGLE ENDED MODE	1	0	+		-
	1	1		+	-
PSEUDO-DIFFERENTIAL MODE	0	0	IN+	IN-	
	0	1	IN-	IN+	



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely. See Figure 5-2 for details on obtaining LSB first data.

** t_{DATA}: during this time, the bias current and the comparator powers down while the reference input becomes a high impedance node.

FIGURE 5-1: *Communication with the MCP3002 using MSB first format only.*



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely.

** t_{DATA}: During this time, the bias circuit and the comparator powers down while the reference input becomes a high impedance node, leaving the CLK running to clock out LSB first data or zeroes.

FIGURE 5-2: *Communication with MCP3002 using LSB first format.*

6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3002 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Depending on how communication routines are used, it is very possible that the number of clocks required for communication will not be a multiple of eight. Therefore, it may be necessary for the MCU to send more clocks than are actually required. This is usually done by sending 'leading zeros' before the start bit, which are ignored by the device. As an example, Figure 6-1 and Figure 6-2 show how the MCP3002 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1 where the clock idles in the 'high' state.

As shown in Figure 6-1, the first byte transmitted to the A/D Converter contains one leading zero before the start bit. Arranging the leading zero this way produces the output 10 bits to fall in positions easily manipulated by the MCU. When the first 8 bits are transmitted to the device, the MSB data bit is clocked out of the A/D Converter on the falling edge of clock number 6. After the second eight clocks have been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Easier manipulation of the converted data can be obtained by using this method.

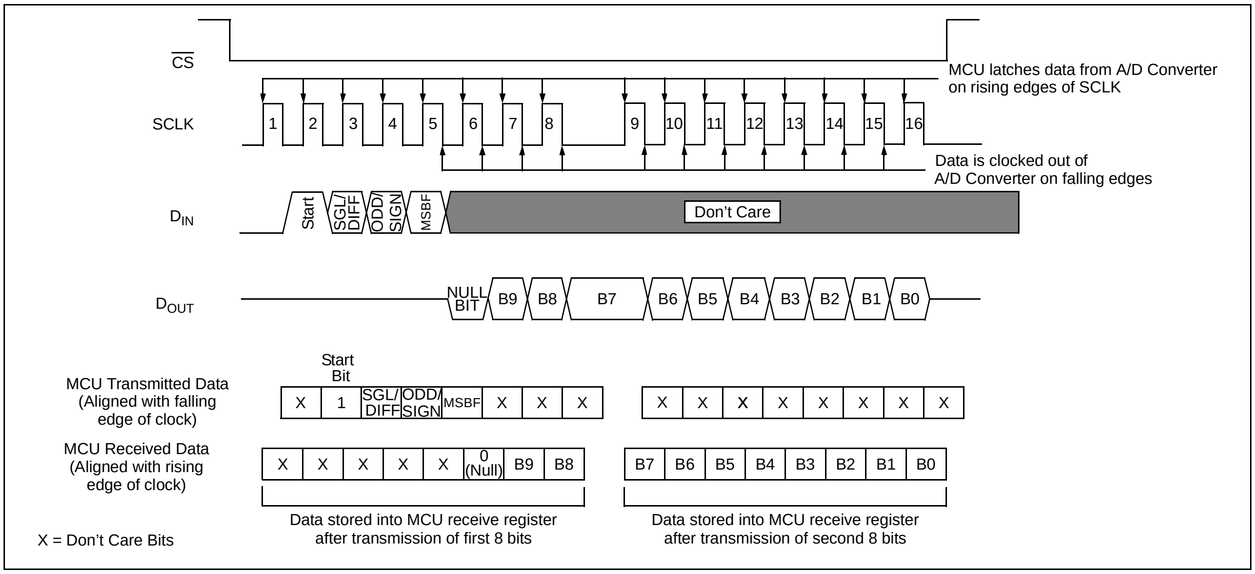


FIGURE 6-1: *SPI Communication with the MCP3002 using 8-bit segments (Mode 0,0: SCLK idles low).*

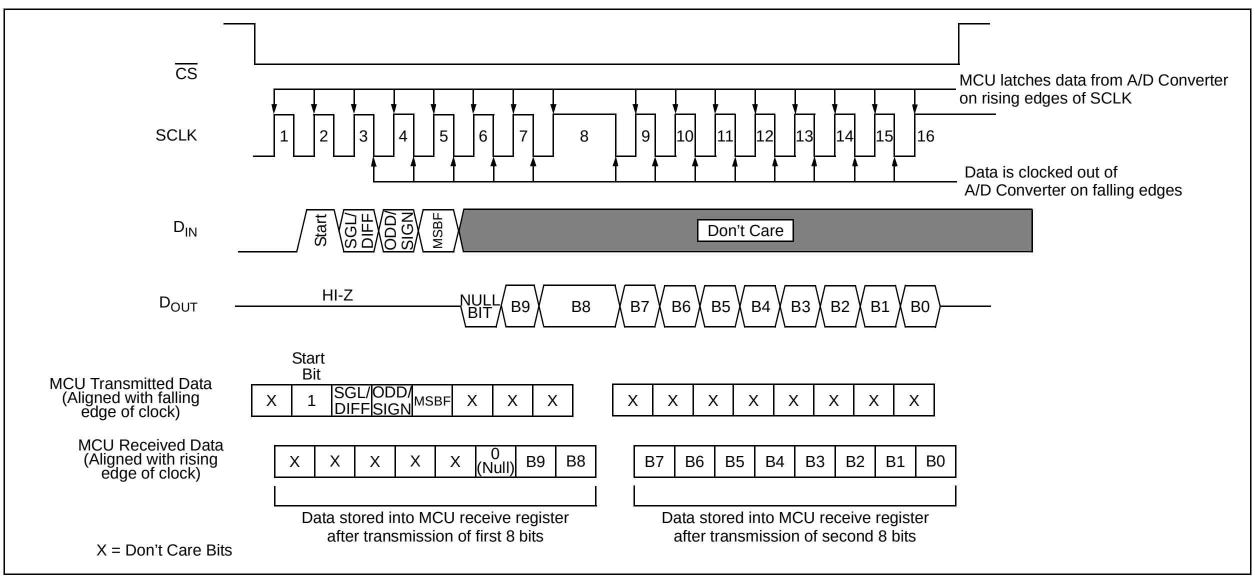


FIGURE 6-2: *SPI Communication with the MCP3002 using 8-bit segments (Mode 1,1: SCLK idles high).*

6.2 Maintaining Minimum Clock Speed

When the MCP3002 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample cap for 700 µs at V_{DD} = 2.7V and 1.5 ms at V_{DD} = 5V. This means that at V_{DD} = 2.7V, the time it takes to transmit the 1.5 clocks for the sample period and the 10 clocks for the actual conversion must not exceed 700 µs. Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. It is also recommended that a filter be used to eliminate any signals that may be aliased back in to the conversion results. This is illustrated in Figure 6-3 below where an op amp is used to drive, filter, and gain the analog input of the MCP3002. This amplifier provides a low impedance output for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab™ software. FilterLab will calculate capacitor and resistors values, as well as, determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 *"Anti-Aliasing Analog Filters for Data Acquisition Systems."*

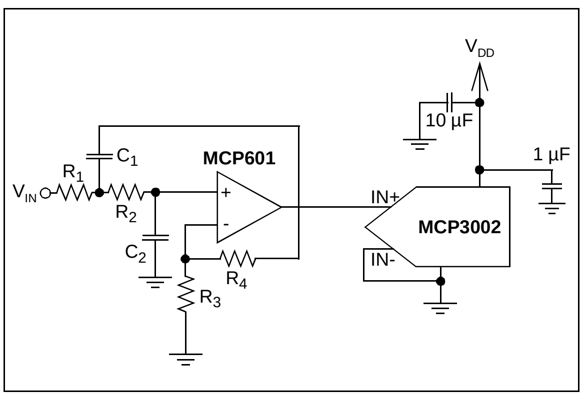


FIGURE 6-3: *Typical Anti-Aliasing Filter Circuit (2 pole Active Filter).*

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D converters, refer to AN-688 *"Layout Tips for 12-Bit A/D Converter Applications"*.

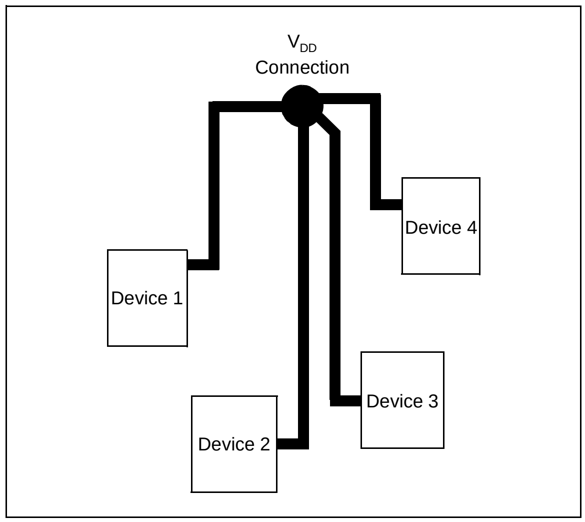
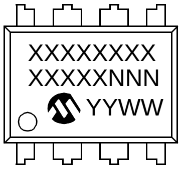


FIGURE 6-4: *V_{DD} traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.*

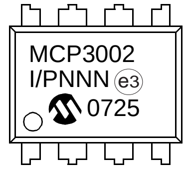
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

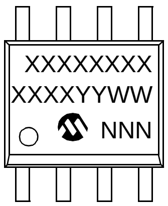
8-Lead PDIP (300 mil)



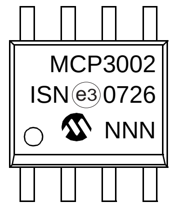
Example:



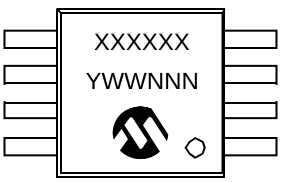
8-Lead SOIC (150 mil)



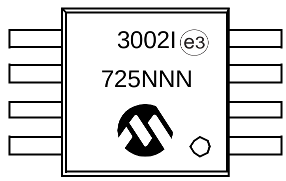
Example:



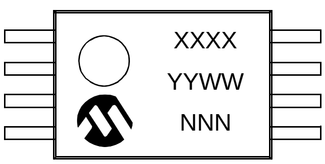
8-Lead MSOP



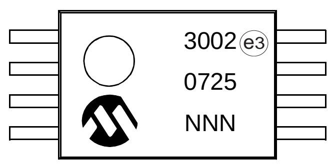
Example:



8-Lead TSSOP



Example:

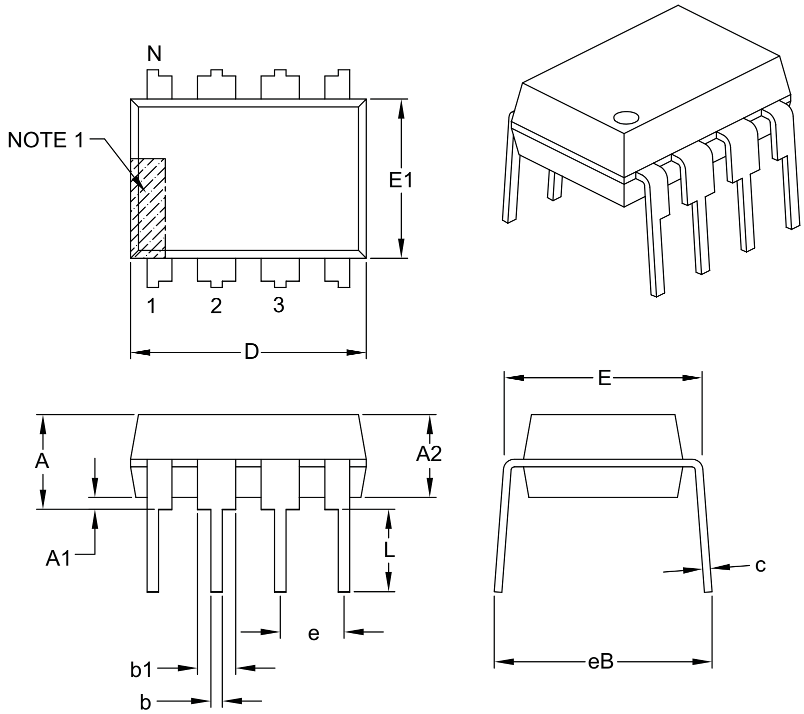


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

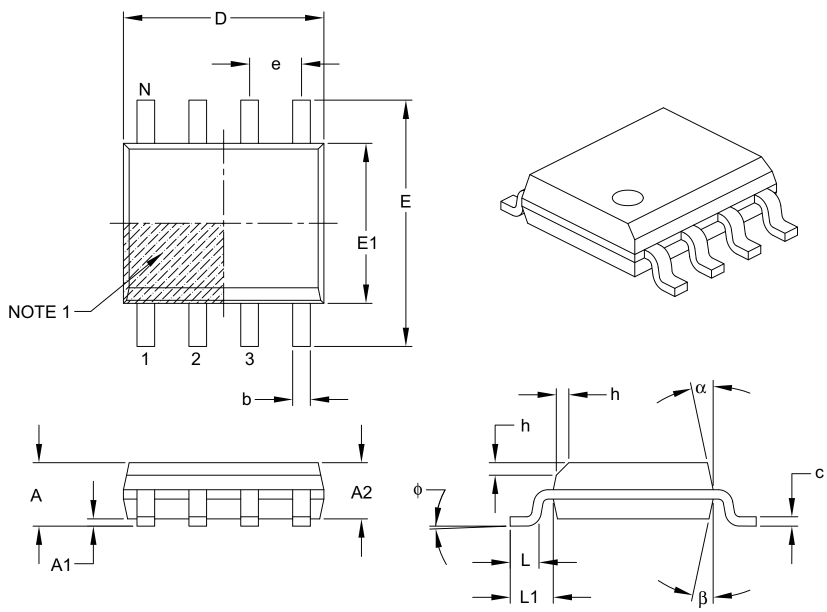
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

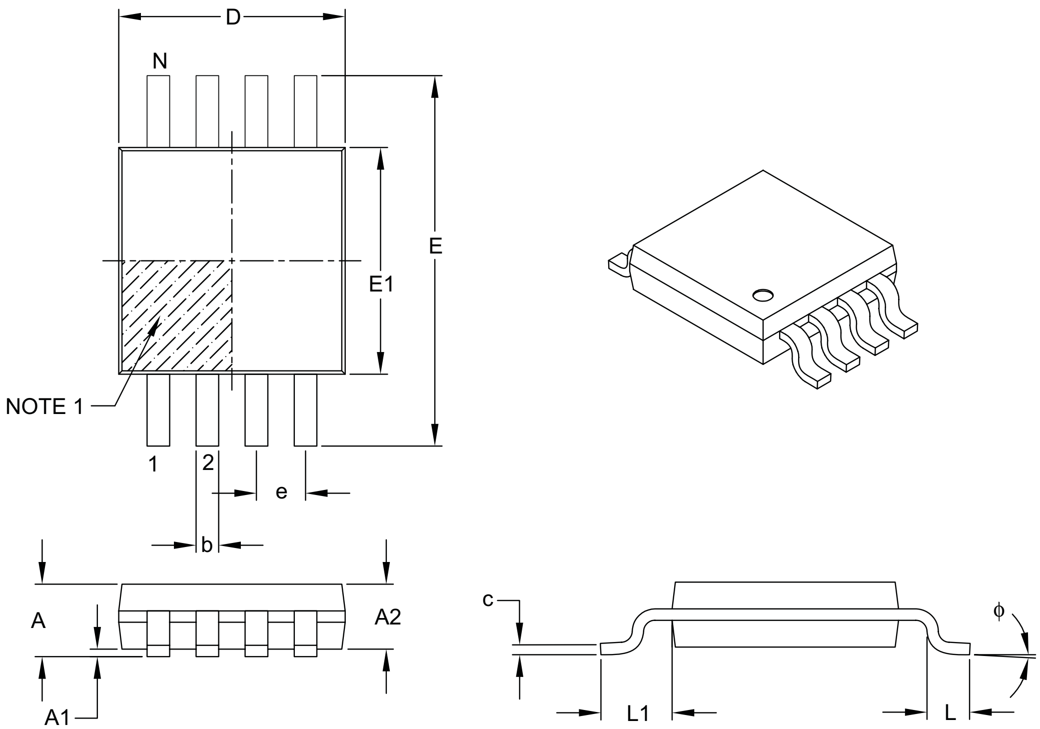
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

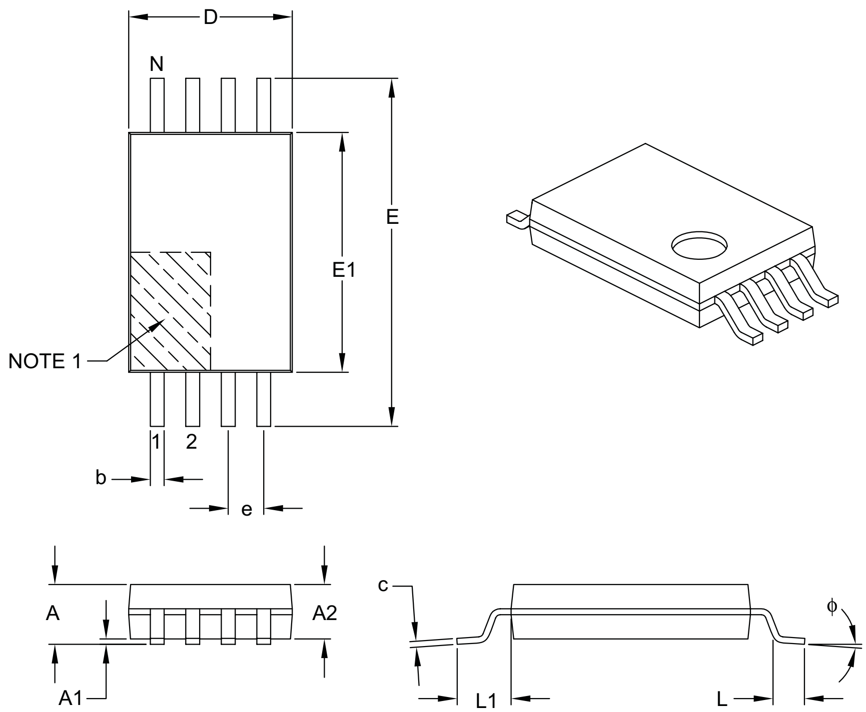
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (January 2007)

This revision includes updates to the packaging diagrams.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP3002:	10-Bit Serial A/D Converter
	MCP3002T:	10-Bit Serial A/D Converter (Tape and Reel) (SOIC and TSSOP only)
Temperature Range:	I	= -40°C to +85°C
Package:	MS	= Plastic Micro Small Outline (MSOP), 8-lead
	P	= Plastic DIP (300 mil Body), 8-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	ST	= Plastic TSSOP (4.4 mm), 8-lead

Examples:

a) MCP3002-I/P: Industrial Temperature, PDIP package.
b) MCP3002-I/SN: Industrial Temperature, SOIC package.
c) MCP3002-I/ST: Industrial Temperature, TSSOP package.
d) MCP3002-I/MS: Industrial Temperature, MSOP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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