

10A, 120V and 150V, 0.300 Ohm, N-Channel Power MOSFETs

These are N-channel enhancement-mode silicon-gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09192.

Ordering Information

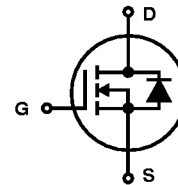
PART NUMBER	PACKAGE	BRAND
RFM10N12	TO-204AA	RFM10N12
RFM10N15	TO-204AA	RFM10N15
RFP10N12	TO-220AB	RFP10N12
RFP10N15	TO-220AB	RFP10N15

NOTE: When ordering, include the entire part number.

Features

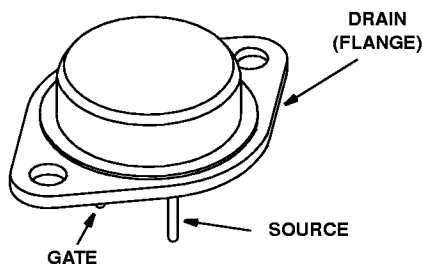
- 10A, 120V and 150V
- $r_{DS(ON)} = 0.3\Omega$
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

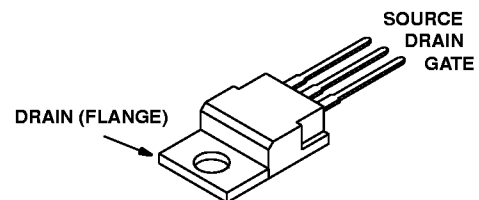


Packaging

TO-204AA



TO-220AB



RFM10N12, RFM10N15, RFP10N12, RFP10N15S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFM10N12	RFM10N15	RFP10N12	RFP10N15	UNITS
Drain to Source Voltage (Note 1) V_{DS}	120	150	120	150	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) V_{DGR}	120	150	120	150	V
Continuous Drain Current I_D	10	10	10	10	A
Pulsed Drain Current (Note 3) I_{DM}	25	25	25	25	A
Gate to Source Voltage V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation P_D	75	75	60	60	W
Linear Derating Factor	0.6	0.6	0.48	0.48	W/ $^\circ\text{C}$
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s. T_L	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See TB334. T_{pkg}	260	260	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFM10N12, RFP10N12	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0$	120	-	-	V
			RFM10N15, RFP10N15	150	-	-
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$, (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, T_C = 125^\circ\text{C}$	-	-	25	mA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 10\text{A}, V_{GS} = 10\text{V}$, (Figures 6, 7)	-	-	0.300	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 10\text{A}, V_{GS} = 10\text{V}$	-	-	3.0	V
Turn-On Delay Time	$t_d(ON)$	$I_D \approx 5\text{A}, V_{DD} = 75\text{V}, R_G = 50\Omega,$ $V_{GS} = 10\text{V}, R_L = 14.7\Omega$ (Figures 10, 11, 12)	-	40	60	ns
Rise Time	t_r		-	165	250	ns
Turn-Off Delay Time	$t_d(OFF)$		-	90	135	ns
Fall Time	t_f		-	90	135	ns
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1\text{MHz}$, (Figure 9)	-	-	850	pF
Output Capacitance	C_{OSS}		-	-	230	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	100	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFM10N12, RFM10N15	-	-	1.67	$^\circ\text{C/W}$
		RFP10N12, RFP10N15S	-	-	2.083	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 5\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 4\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	200	-	ns

NOTE:

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
3. Repetitive rating: pulse width is limited by maximum junction temperature.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

Typical Performance Curves

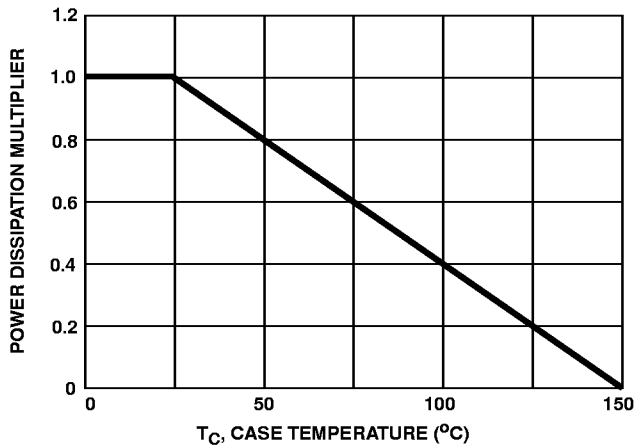


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

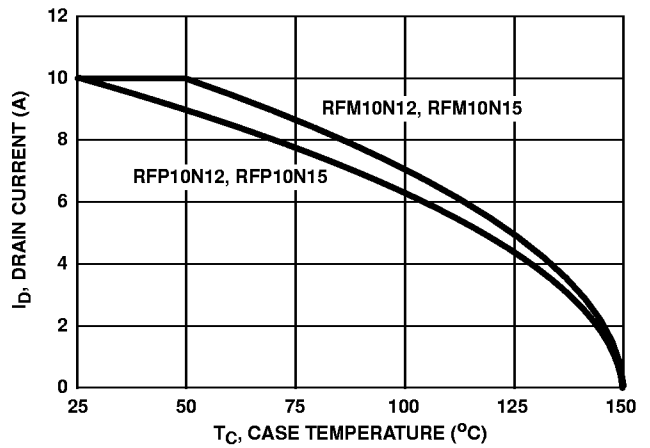


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

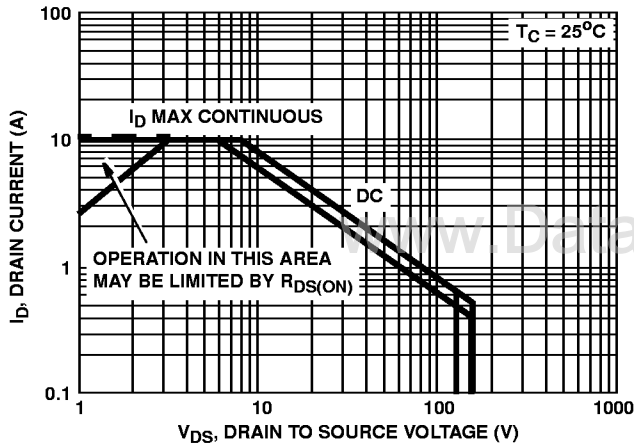


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

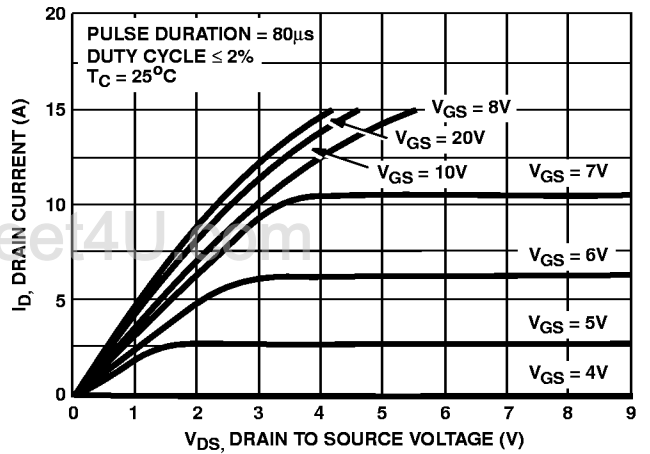


FIGURE 4. SATURATION CHARACTERISTICS

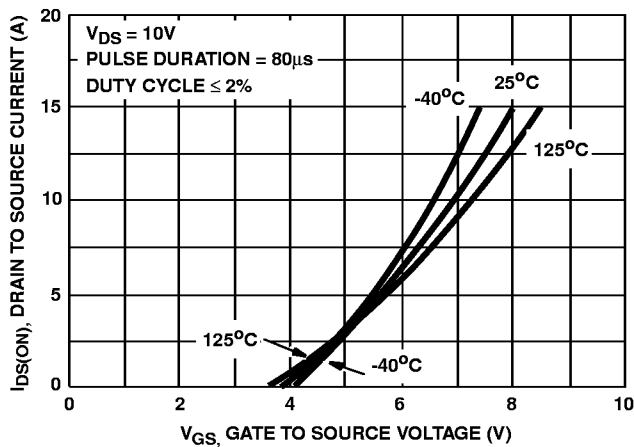


FIGURE 5. TRANSFER CHARACTERISTICS

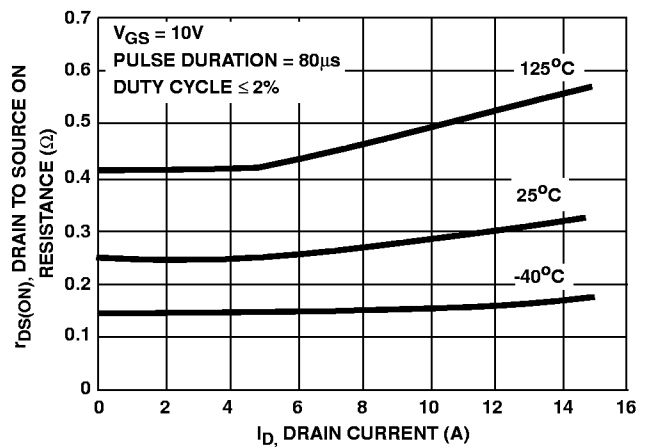


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

RFM10N12, RFM10N15, RFP10N12, RFP10N15

Typical Performance Curves (Continued)

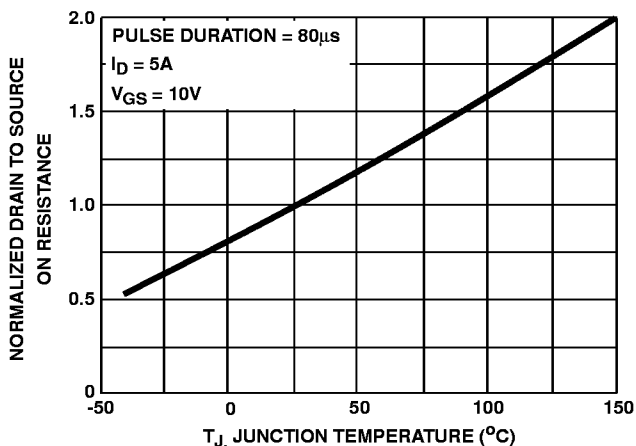


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

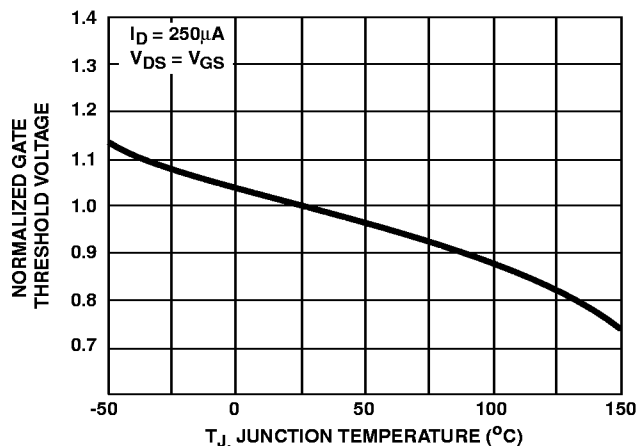


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

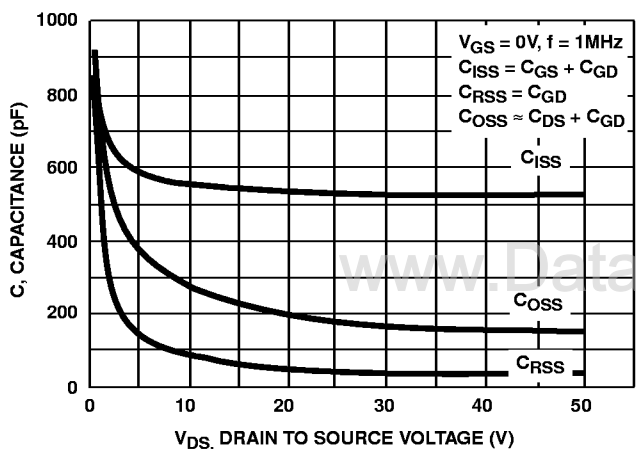
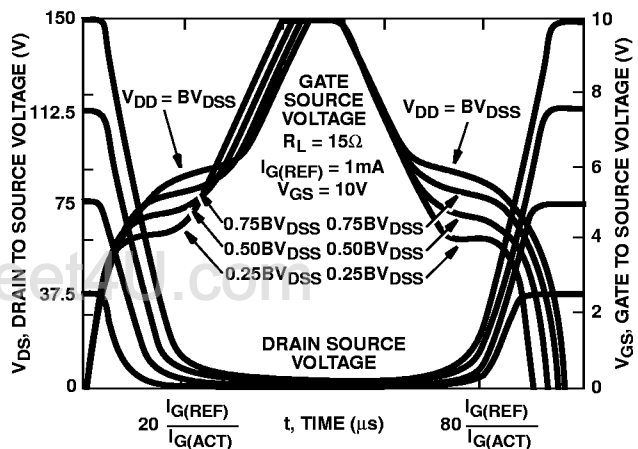


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Applications Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

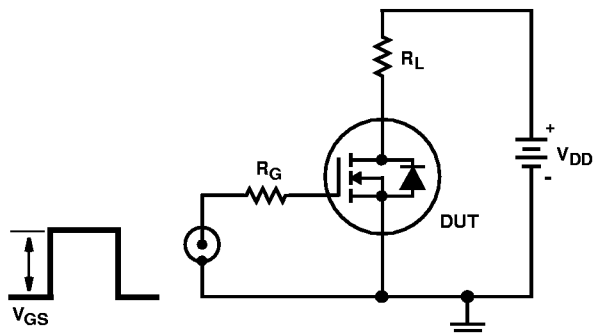


FIGURE 11. SWITCHING TIME TEST CIRCUIT

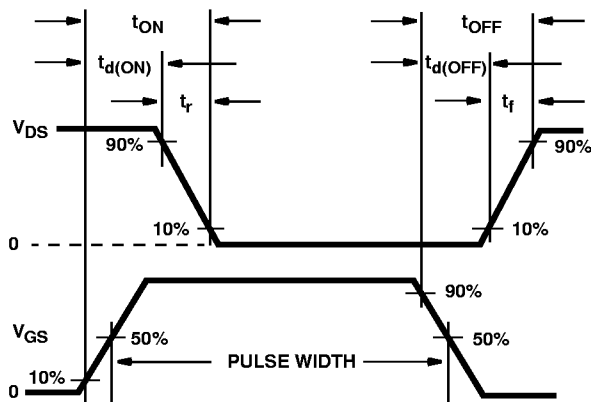


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms

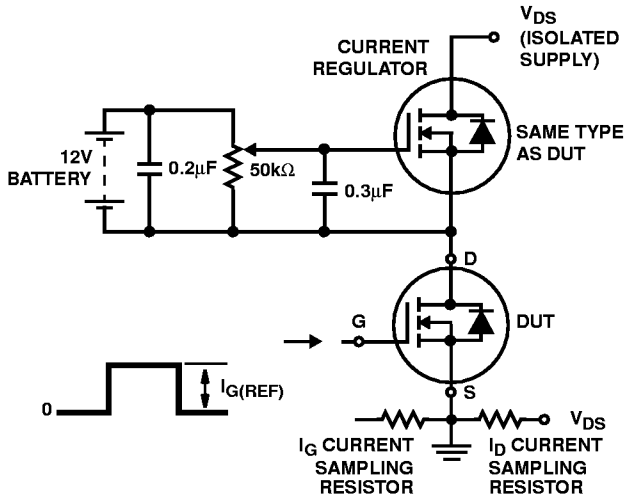


FIGURE 13. GATE CHARGE TEST CIRCUIT

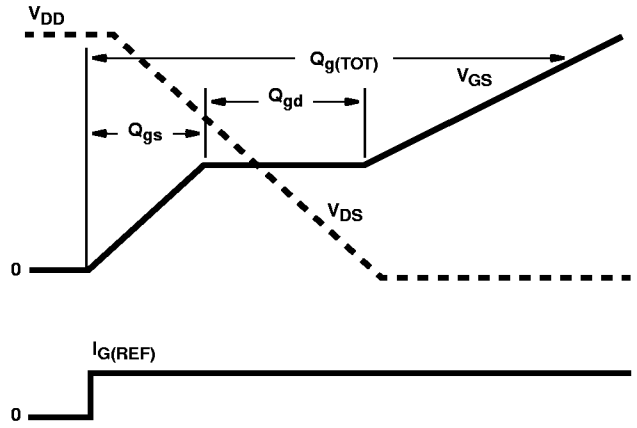


FIGURE 14. GATE CHARGE WAVEFORMS