AK2307/LV
SPEECH CODEC for Digital Key telephone (5.0V/3.3V)

GENERAL DISCREPTION

AK2307/LV is an integrated LSI with PCM CODEC, Voice path control, MIC amplifier and Handset driver suitable for PBX/KTS digital key telephone, VoIP Telephone.

PCM CODEC is compliant to ITU specification, very low noise, and low power dissipation CODEC. A-law and u-law selectable through Serial I/F register.
PCM I/F provides Long/Short frame format and GCI.
The output is 8bit compressed data along with 16bit linear format.

Voice path block consists of Tone generator, Volume for both TX and RX, Analog inputs, outputs for Handset speaker and the speaker for hands-free conversation, and the path control switch.
Side tone can be added internally and its volume is controlled through serial I/F.

FEATURES

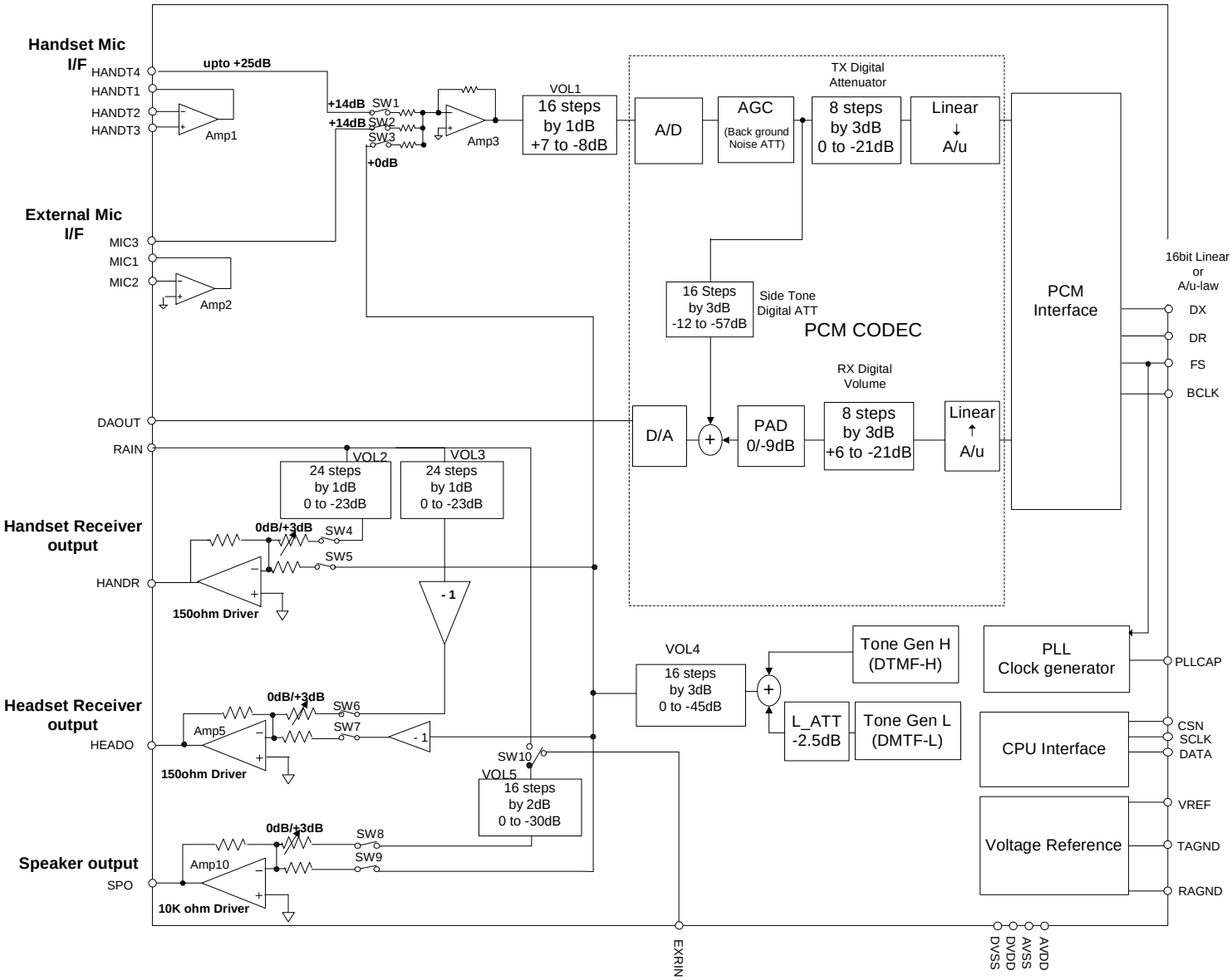
- 2 MIC AMP for the handset and microphone are integrated.
- A 150 ohm handset driver and an extra 150 ohm driver for a headset receiver are provided.
- Path control and volume control via serial CPU I/F
- programmable tone generator
- 5.0V+/-5%, 3.3V+/-0.3V single power supply
- Low noise, low power consumption

Package

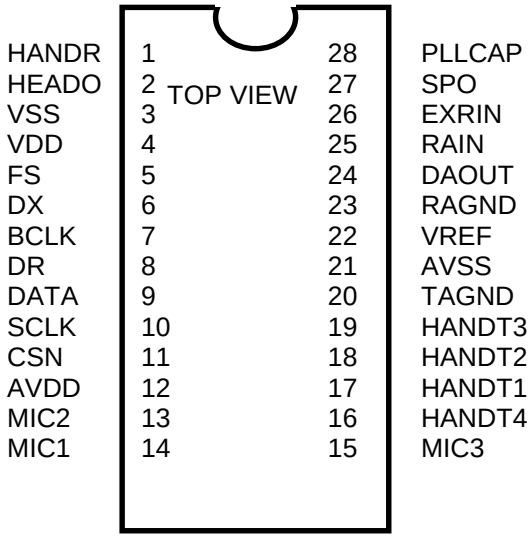
28pin VSOP package

- Package size; 9.8*7.6mm(pin to pin)
- Pin pitch; 0.65mm

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN CONDITIONS

Pin types;
NIN: Normal Input
NOUT: Normal Output
TOUT: Tri-state output
AOUT: Analog output
PWR: Power supply
AIN: Analog Input

Table 1

Name	Type	Pin function	Max Cap load	Mln Res load	comment
HANDT2	AIN	Analog input for Handset microphone			
HANDT3	AIN	Analog input for Handset microphone			
HANDT1	AOUT	OPamp output for Handset microphone			
HANDT4	AIN	Analog input for A/D converter			
HANDR	AOUT	Analog output for Handset receiver	1000pF	150ohm	
MIC3	AIN	2nd Analog input for A/D converter			
MIC2	AIN	Analog input for External microphone			
MIC1	AOUT	Output of External microphone amplifier			
DAOUT	AOUT	Analog output of D/A converter			
RAIN	AIN	Analog input to RX voice path			
HEADO	AOUT	RX output for Headset receiver	1000pF	150ohm	
SPO	AOUT	RX output for External Speaker Driver	20pF	10kohm	
EXRIN	AIN	External input for Speaker pre-driver			
DATA	I/O	Data input for internal register access	50pF		
SCLK	NIN	Serial data clock for internal register access			
CSN	NIN	Chip select input			
DR	NIN	RX PCM data serial input			
DX	TOUT	TX PCM data serial output. Tri-state output	50pF		
BCLK	NIN	Bit clock input for DR, DX			
FS	NIN	8KHz frame sync signal input for PCM I/F			
DVSS	PWR	Power supply for digital block:0V			
DVDD	PWR	Power supply for digital block: 3.3V			
AVSS	PWR	Power supply for Analog block:0V			
AVDD	PWR	Power supply for Analog block: 3.3V			
PLLCAP	AOUT	Output to connect the PLL loop filter Capacitance			1.0uF external capacitance
TAGND	AOUT	TX side Analog ground output.			1.0uF external capacitance
RAGND	AOUT	RX side Analog ground output			1.0uF external capacitance
VREF	AOUT	Voltage reference output			1.0uF external capacitance

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Power Supply Voltages Analog/Digital Power Supply	VDD	-0.3	6.5	V
VSS Voltage	VSS	-0.1	0.1	V
Digital Input Voltage	V_{TD}	-0.3	VDD+0.3	V
Analog Input Voltage	V_{TA}	-0.3	VDD+0.3	V
Input current (except power supply pins)	I_{IN}	-10	10	mA
Storage Temperature	Tstg	-55	125	^{o}C

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies Analog/Digital power supply(AK2307LV)	VDD	3.0	3.3	3.6	V
Analog/Digital power supply(AK2307)	VDD	4.75	5.0	5.25	V
Ambient Operating Temperature	Ta	-10		85	^{o}C
Frame Sync Frequency	FS	-	8	-	kHz

Note) All voltages reference to ground : VSS=0V

1. SERIAL INTERFACE

The internal registers can be read/written via serial CPU interface which consists of SCLK, DATA, and CSN pin.
1 word consists of 16bits. The first 3bits are the instruction code which specifies read or write.
The following 4bits specify the address. The rest of 8bits are the data stored in the internal registers.

Table1-A CPU I/F ADDRESS/DATA STRUCTURE

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
I2	I1	I0	A3	A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
Instruction code (3 bit)			Address (4bit)				*	Data for internal registers (8bit)							

*)Dummy bit for adjusting the I/O timing when reading register.

Table1-B INSTRUCTION CODE

I2	I1	I0	Read/Write
1	1	0	Read
1	1	1	Write
Others			No action

1-2 Timing of the Serial Interface

SCLK and DATA timing in WRITE/READ operation

(1) Input data are loaded into the internal shift register at the rising edge of SCLK.
(2) The rising edge of SCLK is counted after the falling edge of CSN.
(3) When CSN is “L” and more than 16 SCLK pulses:
[WRITE] Data are loaded into the internal register at the rising edge of the SCLK 16th pulse.
[READ] DATA pin becomes an input pin at the falling edge of the SCLK 16th pulse.

CSN timing and WRITE/READ CANCELLATION

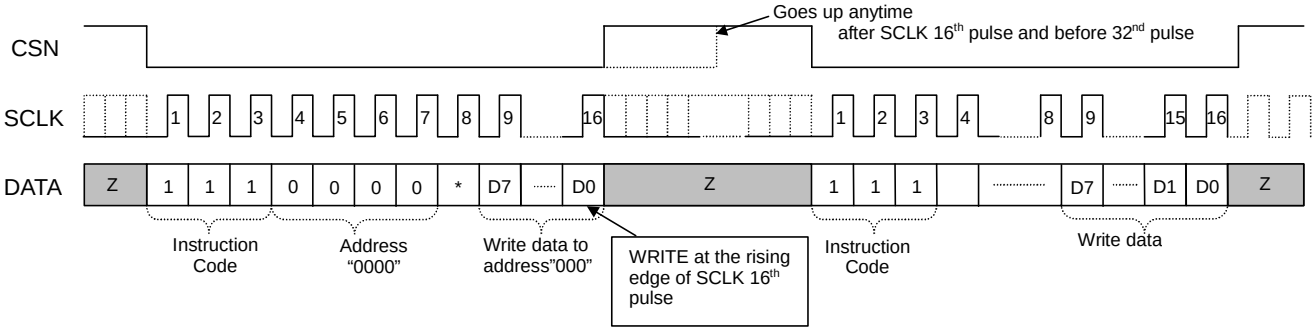
(1) WRITE is cancelled when CSN goes up before the rising edge of the SCLK 16th pulse.
(2) READ is cancelled when CSN goes up before the falling edge of the SCLK 16th pulse.

SERIAL WRITE/READ ACCESS timing (SERIAL ACCESS MODE)

(1) Serial write and read operation will be done by feeding the another 16 SCLK pulse and data after 1st write or read operation.
(2) It is not necessary to make CSN high between 1st operation and 2nd operation.

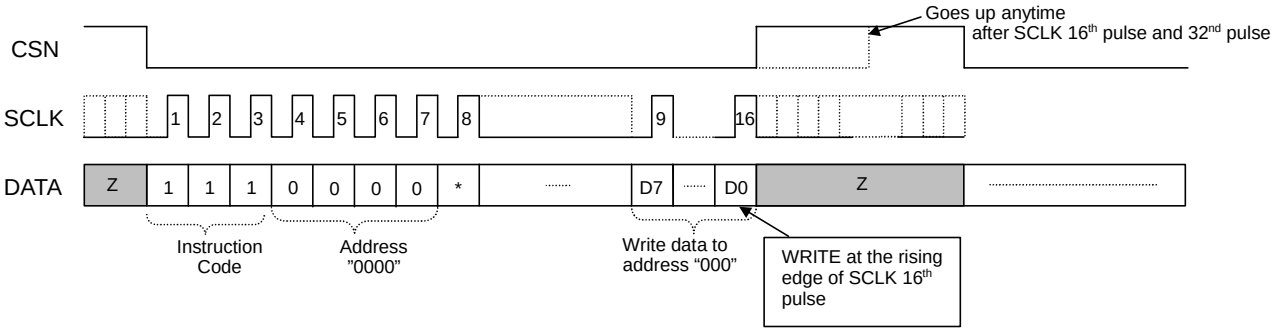
WRITE

Continuous SCLK

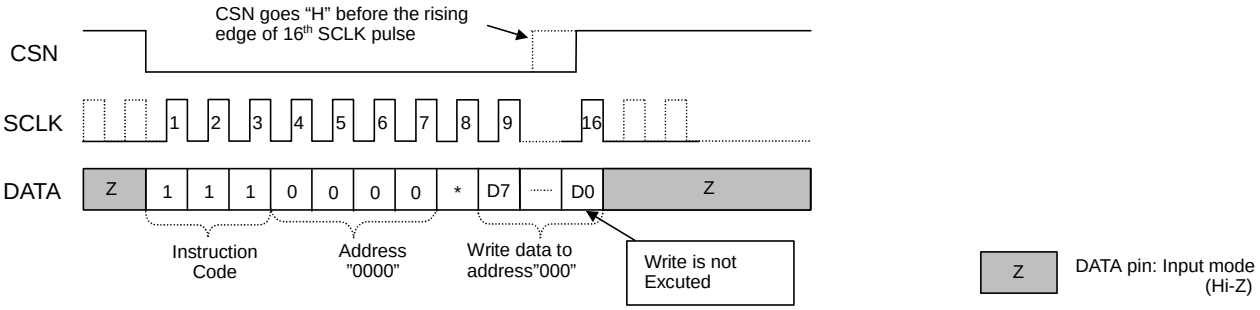


Burst SCLK

SCLK can be stoped at "H" level or "L" level at anytime during the write cycle. After resuming the SCLK, write cycle is retrieved normally.

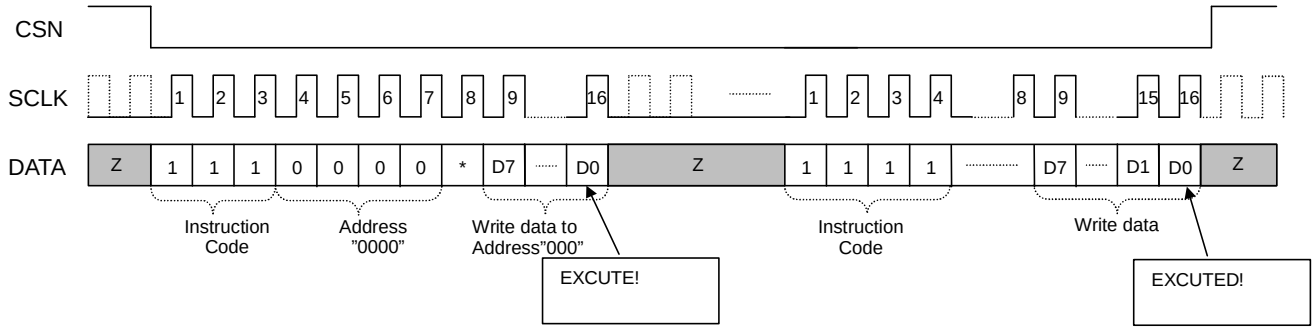


CANCELLATION



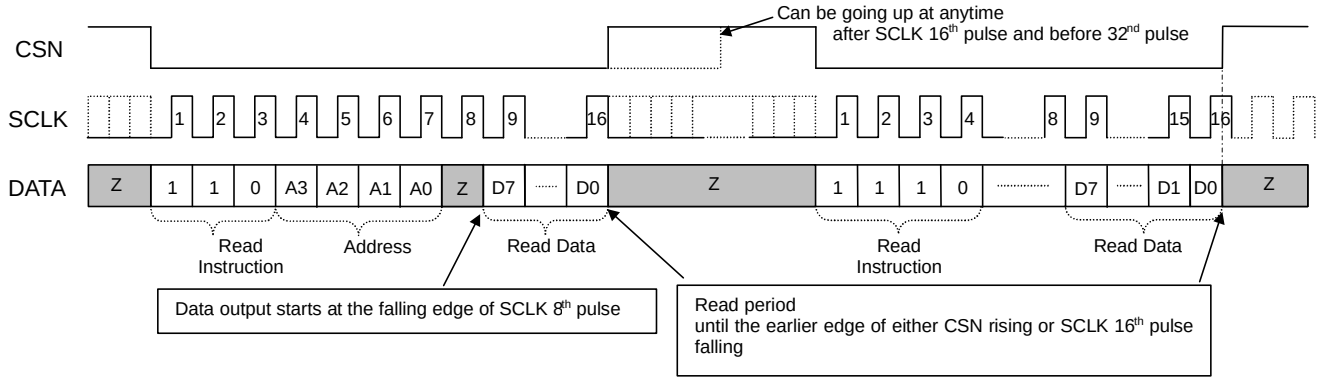
SERIAL ACCESS

Serial access can be done by CSN staying "L" during the serise of write cycle.

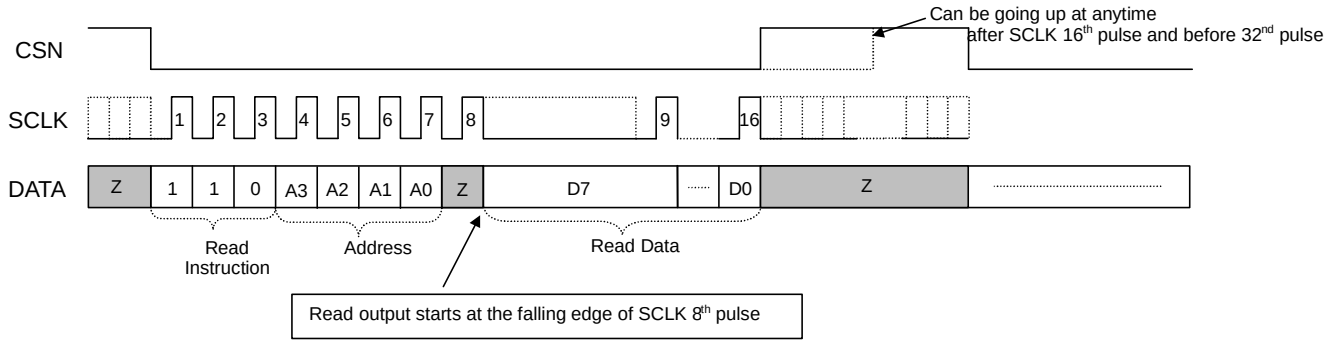


READ

Continuous SCLK

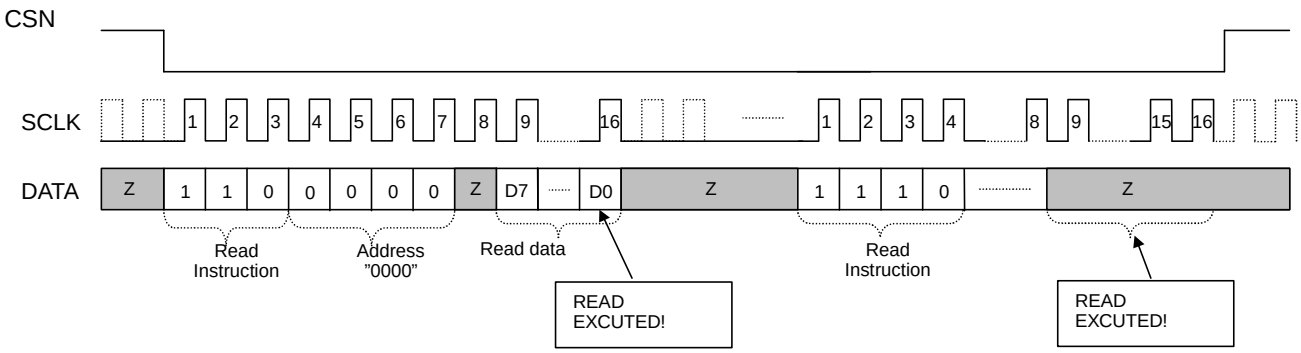


Burst SCLK

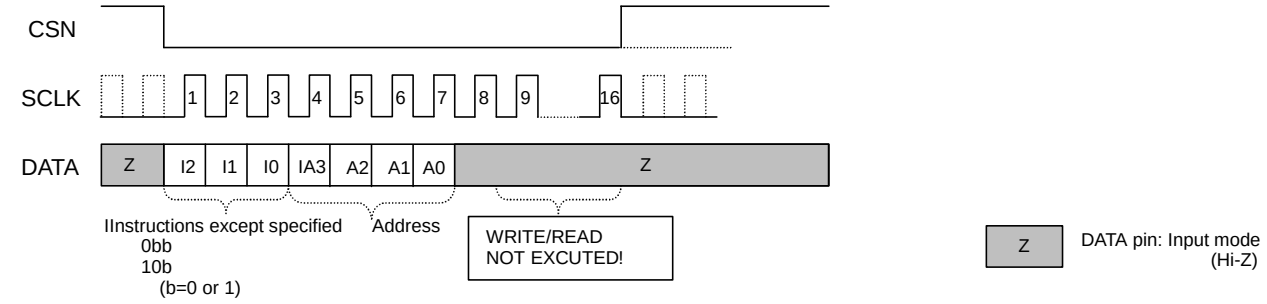


SERIAL ACCESS

Serial access can be done by CSN staying "L" during the serise of read cycle



DISCORD OF INSTRUCTION CODE



Register Map

Register Type : Read/ Write

Add (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Register Name (Functions)
0	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	Path Control 1
1	RX_ A_gain	RX Pad -9dB	Side Tone	PCM_1	PCM_0	u/A-law	SW10	SW9	Path Control 2 & PCM Control
2	0	TX Attenuator			VOL1				TX Digital Volume Control
3	RX Volume				Side Tone Attenuator				RX Digital Volume Control
4	0	0	0	0	VOL4				Tone Volume Control
5	0	0	Tone Freq. Select						Tone Generator 1
6	0	L-ATT	Tone Freq. Select						Tone Generator 2
7	0	0	0	VOL2					RX Handset Volume Control
8	0	0	0	VOL3					RX Headset Volume Control
9	-	-	-	-	VOL5				RX Speaker Volume Control
A	-	AGC_ON	Falling time		Rising time		Threshold level		AGC Control
B – F	-	-	-	-	-	-	-	-	Reserved for test use

Address "1" ; PCM_1/2 ---- Selection of the PCM interface Mode(Long/Short frame, AK130-1,AK130-2, 16bit linear)
Address "6" ; L-ATT ---- -6dB attenuation for Tone generator-L output in case of DTMF tone generation.

Bits in which "0" is filled are for test mode activation. Please fill the data "0" for the normal operation.
Bits in which "-" is filled are for test use and can not write the data from CPU interface. In case the read operation, data "0" are read from CPU interface.

2. PCM Data Interface

AK2307/LV supports 4 PCM data interface modes.

- **A/u-Law PCM data mode(Long or Short frame)**
  This mode is for interface of 64kbps PCM data which are compressed /extended by A -law or u-law. Both Long frame and short frame format data are acceptable. The PCM data occupies the first time slot of the PCM data bus which is specified by the frame sync signal. Please refer to the format diagram.
- **16 bit Linear data Mode**
  This mode interfaces the 16 bit linear PCM data. PCM CODEC of AK2307/LV operates at 14 bit accuracy. The 2 bits of the LSB are fixed in the 16 bit data stream.
- **AK130 B1 Mode**
  This mode provides the PCM data Interface to AK130, the TCM transceiver for PBX/KTS system. PCM data format is 64kbps A-law or u-law data. The timing between data and FS is different from the A/u -Law PCM data mode written above. In this mode the PCM data are transmitted/received via B1 channel , one of the PCM data channel of the AK130.
- **AK130 B2 Mode**
  This mode provides the PCM data interface to AK130 B2 channel in as same manner as AK130 B1 Mode.

In every modes, the digital voice data are in and out from DR and DX pin and the bit clock and the 8KHz frame sync signal will be fed via BCLK and FS, respectively. The order of PCM and linear data is MSB first .

Table 2-A Summary of PCM interface modes

Mode	**PCM data format**	**BCLK rate**	**frame signal**	**Time slot**
A/u-Law PCM data mode	A/u-Law	64K x N (N: 1 to 32)	LF/SF auto select	1st Time slot
16bit Linear data mode	16bit Linear	128K x N (N: 1 to 16)	SF only	first 16 bit after FS signal
AK130 B1 mode	A/u-Law	2.048MHz	AK130 FS signal	xxth time slot of 2.048MHz(B1 channel)
AK130 B2 mode	A/u-Law	2.048MHz	AK130 FS signal	xxth time slot of 2.048MHz(B2 channel)

2-1. Selection of the interface mode

These four interface modes are selectable through the CPU register which specified below.
A/u-Law selection is also selectable from the same CPU register and it is effective in the u/ A-law interface mode and AK130 B1/B2 modes.

Register Name; Path Control 2 Register Type : Read Write

ADD	D7	D6	D5	D4	D3	D2	D1	D0
1	-	RX Pad	Side Tone	**PCM_1**	**PCM_0**	**u/A law**	SW10	SW9
Default	0	0	0	**0**	**0**	**0**	0	0

PCM_1、0 ; PCM interface mode select

PCM_1	**PCM_0**	Mode
0	0	A/u-Law PCM data mode
0	1	16bit Linear interface mode
1	0	AK130 B1 mode
1	1	AK130 B2 mode

u/A-law ; PCM compress/Extend format select

A/u-law	Compress/Extend
0	u-law
1	A-law

2-2 Timing and format of the PCM interface

2-2-1 u/A-Law PCM data Mode

8 bits PCM data is accommodated in 1 frame(125us) defined by 8kHz frame sync signal.
Although there are 32 time slots at maximum in 8kHz frame(when BCK=2.048MHz), PCM data for AK2307/LV occupies first time slot as is indicated in figures below.

2-2-1-a Signals

- Frame Sync signal (FS)
8kHz reference signal. This signal indicated the timing and the frame position of 8kHz PCM interface. All the internal clock
of the LSI is generated based on this FS signal.

- Bit Clock (BCLK)
BCLK defines the PCM data rate. BCLK can be varied from 64kHz to 2.048MHz by 64kHz step.

- PCM data output (DX)
DX is an output signal of 64Kbps PCM u/A-law data. The data is synchronized to the BCLK which determines the data rate. The period which the PCM data is not occupied, the DX pin turns to Hi-impedance output. In the long frame mode, the LSB bit turns to Hi-impedance at the faster edge of ether FS falling edge or 9th rising edge of BCLK.

- PCM data input (DR)
DR is an input signal of 64Kbps PCM u/A-law data. The data is clocked by BCLK at the falling edge and fed into the D/A block.

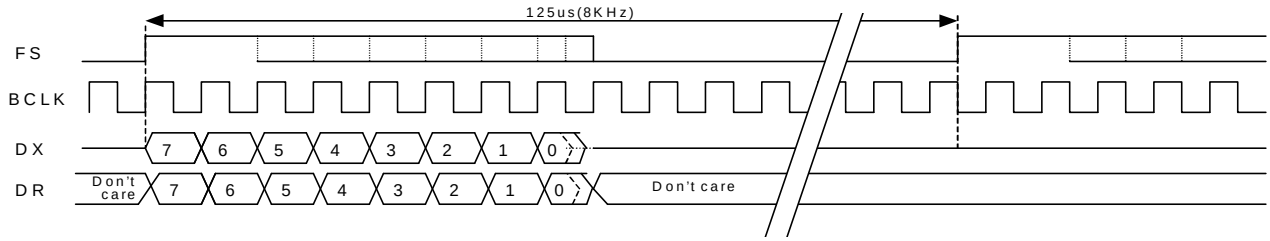
2-2-1-b LONG FRAME(LF) / SHORT FRAME (SF) Automatic selection

AK2307/LV monitors the duration of the "H" level of FS and automatically selects LF or SF interface format.

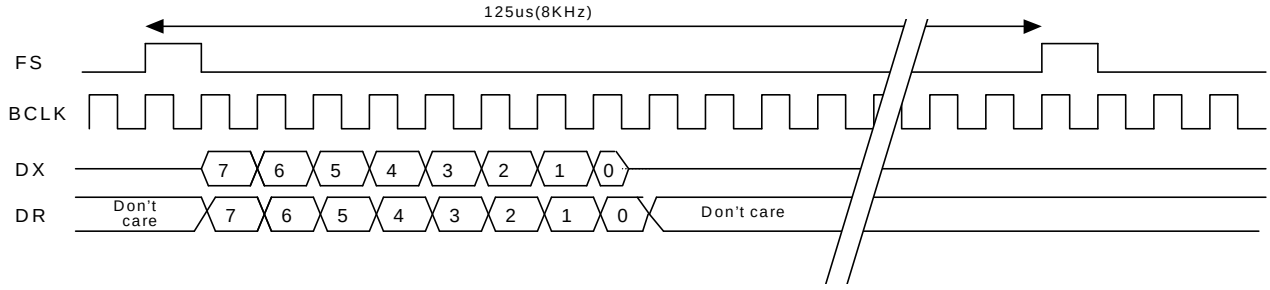
period of FS="H"	Interface format
more than 2 clocks of BCK	LF
1 clock of BCK	SF

2-2-1-c Frame format of the interface

Long Frame format



Short Frame format



2-2-2 16 bit Linear PCM data mode

In this mode the 16 bit linear PCM data are interfaced to the outside. This mode is useful to compress/extend the PCM data by much higher compress rate algorithm than u/A-law algorithm by the external DSP. The AK2307/LV CODEC operates at 14bit accuracy, thus the least 2 bits are output as fixed value.

2-2-2-a Signals

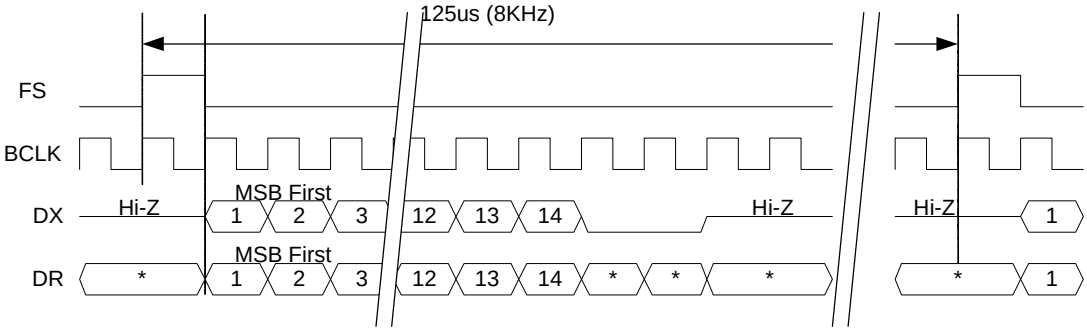
- Frame Sync signal (FS)
8kHz reference signal which is same as in u/A-law PCM data mode. How the FS pulse H level width should be 1 clock period which is like the short frame FS signal.

- Bit Clock (BCLK)
BCLK defines the PCM data rate. BCLK can be varied from **128kHz to 2.048MHz by 128kHz step** which is different from in the u/A-law PCM data mode.

- PCM data output (DX)
DX is an output signal of 128Kbps linear PCM data. The data is synchronized to the BCLK which determines the data rate. The period which the PCM data is not occupied, the DX pin turns to Hi-impedance output.

- PCM data input (DR)
DR is an input signal of 128Kbps linear PCM data. The data is clocked by BCLK at the falling edge and fed into the D/A
block.

16bti Linear Frame format



2-2-3 AK130 B1/B2 Mode

These modes are for connecting the PCM interface to AK130, AKM's TCM(ping-pong) transceiver for PBX/KTS system.
The PCM data format is A-law or u-law which can be selected by the register. The AK130 B1 mode interfaces the data to B1 channel which is one of two B channels which AK130 provides, and the AK130 B2 mode interfaces to B2 channel.

2-2-3-a Signals

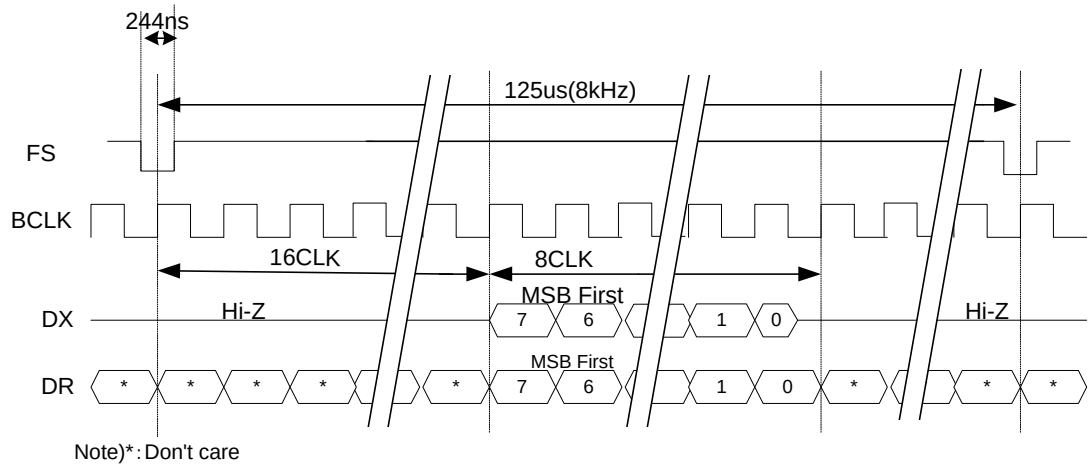
- Frame Sync signal (FS)
Please feed the FS signal which is generated by AK130.($\overline{F0o}$, pin#3)

- Bit Clock (BCLK)
BCLK defines the PCM data rate. Please use 2.048MHz clock which is generated by AK130 .(E2o,pin#5)

- PCM data output (DX)
DX is an output signal of 128Kbps linear PCM data. Please connect to the PCM data input pin of AK130.(DSTi,pin#11)

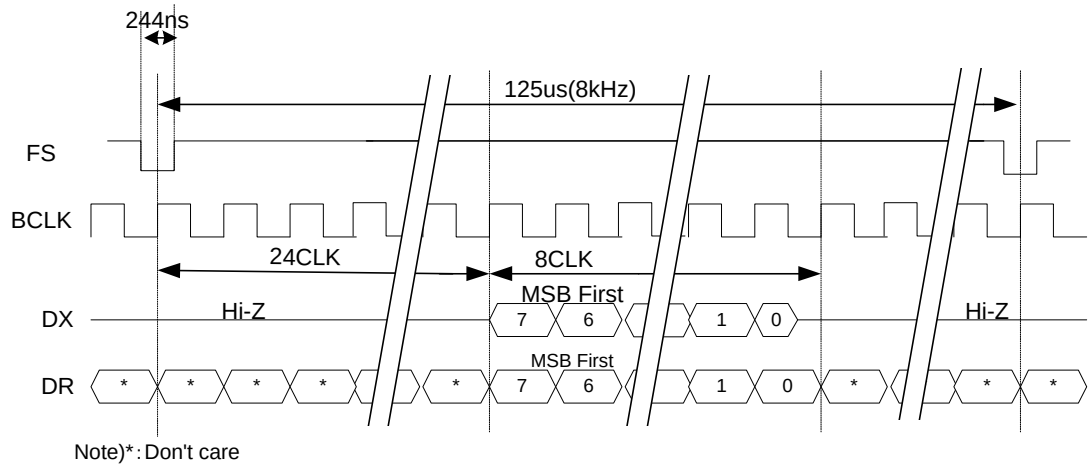
- PCM data input (DR)
DR is an input signal of 128Kbps linear PCM data. The data is clocked by BCLK at the falling edge and fed into the D/A
block. Please connect to the PCM data output pin of AK130.(DSTo,pin#6)

AK130 B1 Mode



Note)* : Don't care

AK130 B2 Mode



Note)* : Don't care

3. Path and Gain Controls

Voice path, gain control of both RX and TX side, and the tone control are controlled from the CPU registers.

3-1. Path control switches;

AK2307/LV has 10 analog switches to control the RX and TX analog path. These switches are controlled from
following 2 registers, Path control 1/2.

Path Control 1

Register Type : Read Write[Address:0000 D7-D0:(SW8-SW1)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
0	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
Default	0	0	0	0	0	0	0	0

Path Control 2

Register Type : Read Write[Address:0001 D6-D5,D1-D0:(RX_Pad, Side_Tone,SW10-SW9)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
1	RX _Apad	RX _Pad	Side Tone	PCM_1	PCM_0	u-law A-law	SW10	SW9
Default	0	1	0	0	0	0	0	0

Table3-a Switch function

SW Name	Function	Polarity
SW10	External voice input enable for Speaker	1: External input path 0: Internal Voice path
SW9	RX Tone output enable for Speaker	1: Tone output ON 0: Tone output OFF
SW8	RX Voice path enable for Speaker	1: Voice path ON 0: Voice path OFF
SW7	RX Tone output enable for Headset	1: Tone output ON 0: Tone output OFF
SW6	RX Voice path enable for Headset	1: Voice path ON 0: Voice path OFF
SW5	RX Tone output enable for Handset	1: Tone output ON 0: Tone output OFF
SW4	RX Voice path enable for Handset	1: Voice path ON 0: Voice path OFF
SW3	TX Tone output enable	1: Tone output ON 0: Tone output OFF
SW2	TX MIC path enable	1: MIC input ON 0: MIC input OFF
SW1	TX Handset path enable	1: Handset path ON 0: Handset path OFF

3-2 Voice path gain Controls

AK2307/LV provides the RX and TX voice gain control functions both in analog domain and in digital domain. These gain
can be controlled from following five registers.

3-2-1. RX voice path gain controls

RX side voice path has three gain control blocks and two gain Pads. These gain stages are controlled through following four registers, Path Control 2, RX digital Volume control, RX handset control, RX Headset control and RX speaker control.

Path Control 2

Register Type : Read Write[Address:0001 D6-D5,D1-D0:(RX_Pad, Side_Tone,SW10-SW9)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
1	RX _Apad	RX _Pad	Side Tone	PCM_1	PCM_0	u-law A-law	SW10	SW9
Default	0	1	0	0	0	0	0	0

RX_Apad ; Analog +3dB gain pad at three RX voice output amps. This gain for to get the extra gain in the RX level diagram. This means, for example, the analog output will be equivalent to one correspond to –7dBm0 digital code when this gain is enabled. However, please notice the maximum analog output can not exceed the one which is defined in analog characteristics specification. The three gain stages at each output can not be changed individually.

Name	Porarity		Comment
RX_Apad	0	0dB	default
	1	+3dB	

RX_Pad; A digital –9dB gain pad at D/A digital domain. This gain pad is for a gain adjustment between the in-system call and the external call.

Name	Porarity		Comment
RX_Pad	0	0dB	default
	1	-9dB	

RX Digital Volume Control

Register Type : Read Write[Address:0011 D7-D0(VTX3-VTX0, VSD_3-VSD_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
3	VRX3	VRX2	VRX1	VRX0	VSD_3	VSD_2	VSD_1	VSD_0
Default	0	1	1	1	1	1	1	1

VRX[3-0]; RX side digital volume from +6dB to –21dB by 3dB step.

when VRX3=1 Gain[dB]＝ 3 x VRX[2-0] (VRX[2-0]=1 or 2)

VRX3=0 Gain[dB]＝ - 3×VRX[2-0]

VRX3	VRX2	VRX1	VRX0	RX digital Attenuator	Comment
0	0	0	0	0dB	Ref level=0dBm0
0	0	0	1	-3dB	
0	0	1	0	-6dB	
0	0	1	1	-9dB	
0	1	0	0	-12dB	
0	1	0	1	-15dB	
0	1	1	0	-18dB	
0	1	1	1	-21dB	default
1	0	0	0	NA	
1	0	0	1	+3dB	
1	0	1	0	+6dB	
1	0	1	1	NA	
1	1	0	0	NA	
1	1	0	1	NA	
1	1	1	0	NA	
1	1	1	1	NA	

NA ; Not applicable

RX Handset Volume Control (Vol 2)

Register Type : Read Write [Address:0111 D4-D0(V2_4-V2_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
7	-	-	-	V2_4	V2_3	V2_2	V2_1	V2_0
default	0	0	0	1	1	1	1	1

V2_[4-0]; Analog volume for the RX side Handset output. The gain is variable from 0dB to –23dB by 1 dB step.

Gain[dB] = -V2[dB] (when 0 <// V2<// 23)

V2_4	V2_3	V2_2	V2_1	V2_0	VOL2	Comment
0	0	0	0	0	0dB	ref level=0dBm0
0	0	0	0	1	-1dB	
0	0	0	1	0	-2dB	
0	0	0	1	1	-3dB	
0	0	1	0	0	-4dB	
0	0	1	0	1	-5dB	
0	0	1	1	0	-6dB	
0	0	1	1	1	-7dB	
0	1	0	0	0	-8dB	
0	1	0	0	1	-9dB	
0	1	0	1	0	-10dB	
0	1	0	1	1	-11dB	
0	1	1	0	0	-12dB	
0	1	1	0	1	-13dB	
0	1	1	1	0	-14dB	
0	1	1	1	1	-15dB	
1	0	0	0	0	-16dB	
1	0	0	0	1	-17dB	
1	0	0	1	0	18dB	
1	0	0	1	1	-19dB	
1	0	1	0	0	-20dB	
1	0	1	0	1	-21dB	
1	0	1	1	0	-22dB	
1	0	1	1	1	-23dB	
1	1	X	X	X	NA	default

NA ; Not applicable

RX Headset Volume Control (Vol 3)

Register Type : Read Write [Address:1000 D4-D0(V3_4-V2_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
8	-	-	-	V3_4	V3_3	V3_2	V3_1	V3_0
default	0	0	0	1	1	1	1	1

V3_[4-0]; Analog volume for the RX side Headset output. The gain is variable from 0dB to –23dB by 1 dB step.

Gain[dB] = -V3[dB] (when 0 <// V2<// 23)

V3_4	V3_3	V3_2	V3_1	V3_0	VOL3	Comment
0	0	0	0	0	0dB	ref level=0dBm0
0	0	0	0	1	-1dB	
0	0	0	1	0	-2dB	
0	0	0	1	1	-3dB	
0	0	1	0	0	-4dB	
0	0	1	0	1	-5dB	
0	0	1	1	0	-6dB	
0	0	1	1	1	-7dB	
0	1	0	0	0	-8dB	
0	1	0	0	1	-9dB	
0	1	0	1	0	-10dB	
0	1	0	1	1	-11dB	
0	1	1	0	0	-12dB	
0	1	1	0	1	-13dB	
0	1	1	1	0	-14dB	
0	1	1	1	1	-15dB	
1	0	0	0	0	-16dB	
1	0	0	0	1	-17dB	
1	0	0	1	0	18dB	
1	0	0	1	1	-19dB	
1	0	1	0	0	-20dB	
1	0	1	0	1	-21dB	
1	0	1	1	0	-22dB	
1	0	1	1	1	-23dB	
1	1	X	X	X	NA	default

NA ; Not applicable

RX Speaker Volume Control (Vol 5)

Register Type : Read Write [Address:1001 D4-D0(V5_4-V5_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
9	-	-	-	-	V5_3	V5_2	V5_1	V5_0
default	0	0	0	0	1	1	1	1

V5_[4-0]; Analog volume for the RX side Speaker output. The gain is variable from 0dB to –30dB by 2 dB step.

Gain[dB] = -2 x V5[dB] (when 0 <// V2<// 15)

V5_3	V5_2	V5_1	V5_0	VOL5	Comment
0	0	0	0	0dB	ref level=0dBm0
0	0	0	1	-2dB	
0	0	1	0	-4dB	
0	0	1	1	-6dB	
0	1	0	0	-8dB	
0	1	0	1	-10dB	
0	1	1	0	-12dB	
0	1	1	1	-14dB	
1	0	0	0	-16dB	
1	0	0	1	-18dB	
1	0	1	0	-20dB	
1	0	1	1	-22dB	
1	1	0	0	-24dB	
1	1	0	1	-26dB	
1	1	1	0	-28dB	
1	1	1	1	-30dB	default

3-2-2. TX voice path gain controls

TX side voice path has two gain control blocks. One is a analog volume and the other is a digital attenuator after D/A converter. These voice path gains are controlled through the following regi ster.

TX Voice Path Gain Control (TX digital Attenuator, VOL 1)

Register Type : Read Write[Address:0010 D6−D0: (VTX2−VTX0, V1_3−V1_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
2	-	VTX2	VTX1	VTX0	V1_3	V1_2	V1_1	V1_0
default	0	1	1	1	0	0	0	0

VTX[2-0]; The digital attenuator for TX side voice path. The gain variation is from 0dB to –21dB by 3dB step.

Gain[dB]= - 3 x VTX(3dB step)

VTX2	VTX1	VTX0	TX voice path digital Attenuator	Comment
0	0	0	0dB	ref level=0dBm0
0	0	1	-3dB	
0	1	0	-6dB	
0	1	1	-9dB	
1	0	0	-12dB	
1	0	1	-15dB	
1	1	0	-18dB	
1	1	1	-21dB	default

V1_[3-0]; An analog volume for TX side voice path. The variable range is from –8dB to +7dB by 1 dB.

Gain[dB] ; -8 + V1 (1dB step)

V1_3	V1_2	V1_1	V1_0	VOL1 TX voice path analog volume	Comment
0	0	0	0	-8dB	default
0	0	0	1	-7dB	
0	0	1	0	-6dB	
0	0	1	1	-5dB	
0	1	0	0	-4dB	
0	1	0	1	-3dB	
0	1	1	0	-2dB	
0	1	1	1	-1dB	
1	0	0	0	0dB	ref level=0dBm0
1	0	0	1	+1dB	
1	0	1	0	+2dB	
1	0	1	1	+3dB	
1	1	0	0	+4dB	
1	1	0	1	+5dB	
1	1	1	0	+6dB	
1	1	1	1	+7dB	

3-2-3. Side Tone path gain controls

AK2307/LV provides the side tone pass from TX to RX in digital domain. The activation of this pass is set through Path Control 1 register(address=0) and the side tone attenuation is controled through “RX Digital volume control” register(address=2).

Path Control 2

Register Type : Read Write[Address:0001 D6-D5,D1-D0:(RX_Pad, Side_Tone,SW10-SW9)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
1	RX _Apad	RX _Pad	Side Tone	PCM_1	PCM_0	u-law A-law	SW10	SW9
Default	0	1	0	0	0	0	0	0

Side Tone; A pass enable of the side tone from TX to RX.

Name	Porarity		Comment
Side Tone	0	OFF	default
	1	ON	

Side Tone digital attenuator gain

Register Type : Read Write[Address;0011 D7-D0:(VTX3-VTX0, VSD_3-VSD_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
3	VRX3	VRX2	VRX1	VRX0	VSD_3	VSD_2	VSD_1	VSD_0
default	0	1	1	1	1	1	1	1

VSD_[3-0]; Side tone digital Attenuator. The gain variation range is from –12dB to –57dB.

Gain[dB]＝ -12 –3×VSD

VSD_3	VSD_2	VSD_1	VSD_0	Side Tone digital Attenuator gain	Comment
0	0	0	0	-12dB	
0	0	0	1	-15dB	
0	0	1	0	-18dB	
0	0	1	1	-21dB	
0	1	0	0	-24dB	
0	1	0	1	-27dB	
0	1	1	0	-30dB	
0	1	1	1	-33dB	
1	0	0	0	-36dB	
1	0	0	1	-39dB	
1	0	1	0	-42dB	
1	0	1	1	-45dB	
1	1	0	0	-48dB	
1	1	0	1	-51dB	
1	1	1	0	-54dB	
1	1	1	1	-57dB	default

4. Tone generator

AK2307/LV has two tone generators to generate the service tone, DTMF tone and melody tone. Each generator can select the 42 tone frequencies individually, and they are added each other before output from RX receiver amp or TX A/D path.
After the adding stage there is a gain stage to attenuate the tone level from 0dB to –45dB by 3dB step. For the DTMF low
frequency tone, there is another attenuator to attenuate by –2.5dB which can be set from the register.

The signal format is 64 stepwise pseudo sine wave. When the tone frequency is changed, the frequency is changed at the 0 cross point of the tone to prevent the switching noise.

4-1. Tone frequency select

The 43 tone frequencies for the generator-H and the generator-L can be selected individually from the different registers, "Tone generator H-frequency select" and "Tone generator L-frequency select".

There is two kind of parameters to select the tone frequency. One is to select the fundamental frequency and another is to select the dividing ratio of the fundamental frequency to get the final tone frequency. For example, when 1600Hz is selected as a fundamental frequency and the number 1/4 is selec ted as a dividing factor, then the final tone frequency shall be 400Hz.

Tone generator H-frequency select

Register Type : Read Write[Address=0101: D5-D0:(DIVH_1-DIVH_0, TH_3-TH_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
5	-	-	DIVH_1	DIVH_0	TH_3	TH_2	TH_1	TH_0
default	0	0	0	0	0	0	0	0

Tone generator L-frequency select

Register Type : Read Write[Address=0110 D6-D0: (LT_ATT, DIVL_1-DIVL_0, TL_3-TL_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
6	-	LT_ATT	DIVL_1	DIVL_0	TL_3	TL_2	TL_1	TL_0
default	0	0	0	0	0	0	0	0

TH_[3-0] / TL_[3-0]; The select bits of the fundamental frequency for the tone generator-H and the tone generator-L, respectively.

Fundamental frequencies

Tx_3	Tx_2	Tx_1	Tx_0	Fundamental frequency(Hz)
0	0	0	0	mute
0	0	0	1	1600.00
0	0	1	0	1471.26
0	0	1	1	1391.30
0	1	0	0	1333.33
0	1	0	1	1207.55
0	1	1	0	1174.31
0	1	1	1	1049.18
1	0	0	0	1000.00
1	0	0	1	941.18
1	0	1	0	888.89
1	0	1	1	853.33
1	1	0	0	785.28
1	1	0	1	771.08
1	1	1	0	727.27
1	1	1	1	571.43

Tx ; TH or TL

DIVH_[1-0] / DIVL_[1-0]; The dividing factor of the fundamental frequency to get the final tone frequency.

Tone frequency = fundamental frequency x dividing factor.

Dividing factor

DIVx_1	DIVx_0	dividing factor
0	0	1
0	1	1/2
1	0	1/4
1	1	NA

DIVx ; DIVH or DIVL

Tone frequency list;

Fundamental Freq. (TH,TL3-0)		Dividing factor(DIVH/L1-0)		
Code	Fundamental Freq(Hz)	1(Hz)	1/2(Hz)	1/4(Hz)
0	Mute	-	-	-
1	1600.00	1600.00	800.00	400.00
2	1471.26	1471.26	735.63	367.82
3	1391.30	1391.30	695.65	347.83
4	1333.33	1333.33	666.67	333.33
5	1207.55	1207.55	603.78	301.89
6	1174.31	1174.31	587.16	293.58
7	1049.18	1049.18	524.59	262.30
8	1000.00	1000.00	500.00	250.00
9	941.18	941.18	470.59	235.30
A	888.89	888.98	444.49	222.25
B	853.33	853.33	426.67	213.33
C	785.28	785.28	392.64	196.32
D	771.08	771.08	385.54	192.77
E	727.27	727.27	363.64	181.82
F	571.43	571.43	285.72	142.86

functional category of the tone

Category	Nominal freq. (Hz)	Fundamental Freq(Hz)	Dividing Factor	Tx_[3-0] Code	DIVx_[1-0] Code	error (Typ)	Comment
Melody	1397	1391.3	1	0011	00	-0.4%	Fa''
	1318	1333.33	1	0100	00	+1.1%	Mi''
	1175	1174.31	1	0110	00	-0.1%	Re''
	1046	1049.18	1	0111	00	+0.3%	Do''
	988	1000	1	1000	00	+1.2%	Si'
	880	882.76	1	1010	00	+0.3%	la'
	784	785.28	1	1100	00	+0.2%	So'
	698	1391.3	2	0011	01	-0.3%	Fa'
	659	1333.33	2	0100	01	+1.2%	Mi'
	587	1174.31	2	0110	01	0.0%	Re'
	523	1049.18	2	0111	01	+0.3%	Do'
	494	1000	2	1000	01	+1.2%	Si
	440	882.76	2	1010	01	+0.3%	la
	392	785.28	2	1100	01	+0.2%	So
DTMF	697	1391.3	2	0011	01	-0.2%	Low
	770	771.08	1	1101	00	+0.1%	Low
	852	853.33	1	1011	00	+0.2%	Low
	941	941.18	1	1001	00	±0.0%	Low
	1209	1207.55	1	0101	00	-0.1%	High
	1336	1333.33	1	0100	00	-0.2%	High
	1477	1471.26	1	0010	00	-0.4%	High
Misc.	726	727.27	1	1110	00	+0.2%	
4k/n	4k/16=250	1000	4	1000	10	0.0%	
	4k/12=333.33	1333.33	4	0100	10	0.0%	
	4k/11=363.64	727.27	2	1110	01	0.0%	
	4k/10=400	1600	4	0001	10	0.0%	
	4k/9 =444.44	888.89	2	1010	01	0.0%	
	4k/8 =500	1000	2	1000	01	0.0%	
	4k/7 =571.43	571.43	1	1111	00	0.0%	
	4k/6 =666.67	1333.33	2	0100	01	0.0%	
	4k/5 =800	1600	2	0001	01	0.0%	
	4k/4 =1000	1000	1	1000	00	0.0%	
Misc.	350	1391.3	4	0011	10	-0.6%	
	440	882.76	2	1010	01	+0.3%	
	600	1174.31	2	0110	01	-2.1%	
	680	1391.3	2	0011	01	+2.3%	
	1600	1600	1	0001	00	0.0%	

4-2 Tone volume control

The volume control of the tone is done through "Tone Volume Control" register. The gain is changed after two tones are added, thus the signal level of two tone is always same. Only L-ATT bit in "Tone generator L-frequency select" register can change the signal level between two tones by -2.5dB.

Tone generator L-frequency select

Register Type : Read Write[Address=0110 D6-D0: (LT_ATT, DIVL_1-DIVL_0, TL_3-TL_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
6	-	LT_ATT	DIVL_1	DIVL_0	TL_3	TL_2	TL_1	TL_0
default	0	0	0	0	0	0	0	0

LT_ATT; Attenuation bit for the low frequency tone generator.

LT_ATT	DTMF Low frequency(Tone generator L)	Comments
0	0dB	default
1	-2.5dB	

*) Gain error of the LT_ATT is +/-1.0dB at the worst case. In this case, LT_ATT is irregular from the DTMF standard.

Tone Volume Control (vol 4)

Register Type : Read Write[Address=0100: D3-D0: (V4_3-V4_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
4	-	-	-	-	V4_3	V4_2	V4_1	V4_0
default	0	0	0	0	1	1	1	1

V4_[3-0]; Tone volume control.(Volume4) The gain range is from 0dB to –45dB by 3dB step.

Gain[dB]= - 3×V4

V4_3	V4_2	V4_1	V4_0	VOL4 Tone volume control	Comment
0	0	0	0	0dB	
0	0	0	1	-3dB	
0	0	1	0	-6dB	
0	0	1	1	-9dB	
0	1	0	0	-12dB	
0	1	0	1	-15dB	
0	1	1	0	-18dB	
0	1	1	1	-21dB	
1	0	0	0	-24dB	
1	0	0	1	-27dB	
1	0	1	0	-30dB	
1	0	1	1	-33dB	
1	1	0	0	-36dB	
1	1	0	1	-39dB	
1	1	1	0	-42dB	
1	1	1	1	-45dB	default

5. Power on Reset

Power on Reset
AK2307/LV automatically generates the internal reset pulse which resets all the circuit that is necessary to start the initialization after the power on reset. The CPU registers are set to the default value.

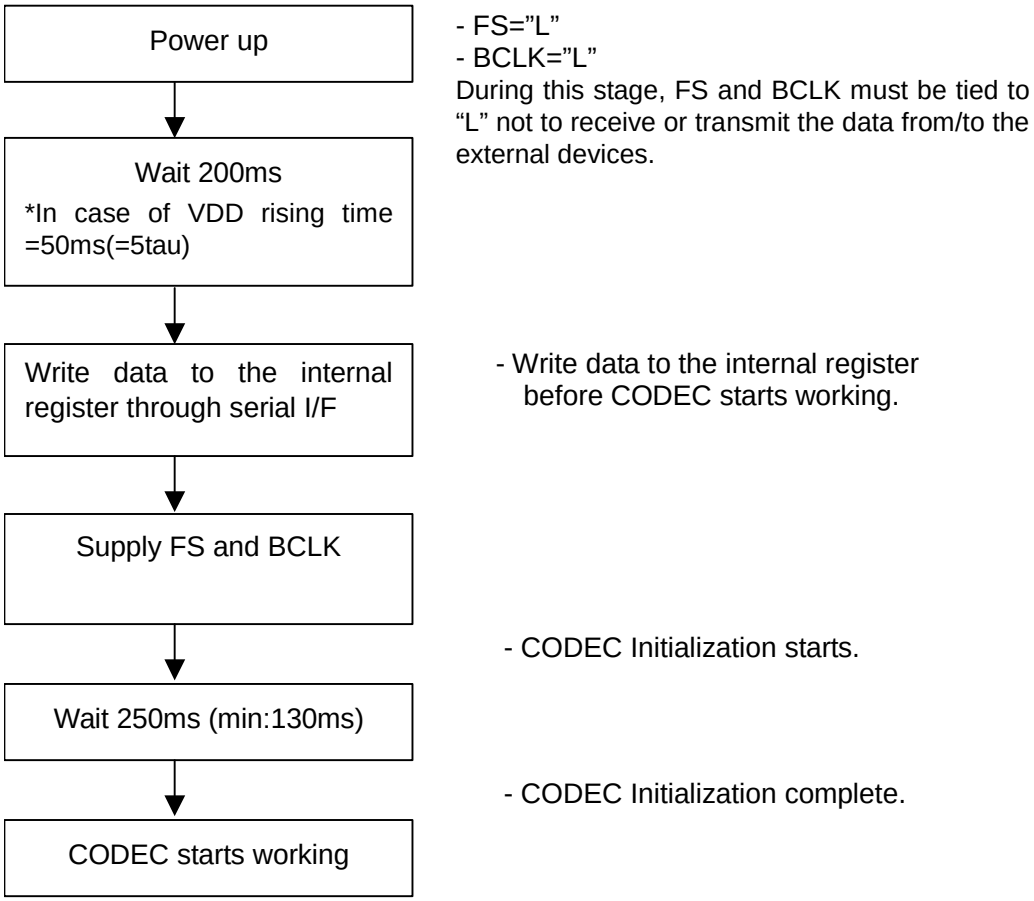
After the internal reset pulse is generated, CODEC starts the initialization procedure by being fed FS signal, and it takes 150ms(typ.), 330ms(max) to complete the initialization after the detection of power on.

Power up slope to enable the Power-on Reset
When the power-up slope is no longer than 50ms(=5tau:tau is time constant), Power On Reset works normally.

When the time is longer than 50ms, Power On Reset may not be activated and no internal regist ers are initialized. In this case all registers must be written through CPU interface.

NOTE) For the stable operation after power up, we recommend to write all register value through CPU interface in any case after the power up.

Recommended start up procedure
The following start up procedure is recommended when AK2307/LV is going to power up.



ELECTRICAL CHARACTERISTICS

Unless otherwise noted, guaranteed for VDD=+5.0V+/-5%(AK2307), VDD=+3.3V+/-0.3V(AK2307LV), Ta = –10 ~ +85 °C, FS=8kHz.

DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Consumption BCLK=2048kHz	Idd	* Note1)	-	20	-	mA
Output High Voltage (CMOS level)	V_{OH}	I_{OH}=-1.6mA	VDD-0.5			V
Output Low Voltage (CMOS level)	V_{OL}	I_{OL}=1.0mA			0.4	V
Input High Voltage1 (CMOS level)	V_{IH1}		0.7VDD			V
Input Low Voltage1 (CMOS level)	V_{IL1}				0.3VDD	V
Input Leakage Current	Ii		-10		+10	uA
Input Capacitance	Ci				5	pF
Input Leakage Current	Ill		-10		10	uA
Output Leakage Current	Ilt	Tri-state mode	-10		10	uA

*Note1) All the output pin are unloaded. 1020Hz@0dBm0 sine wave from HANDT2/3, A to A loopbacked.
All the volume gain are set to 0dB and two of the tone generator are off. The handset mic and receiver paths are only active.

◆AC Characteristics

Note) Otherwise specified, Ta=-10℃～+70 degree, VDD=5.0V +/- 5%(AK2307),VDD=3.3V +/- 0.3V(AK2307LV), VSS=0V, FS=8kHz are assumed. All the timing parameters are measured at VOH=VDD-0.5, VOL=0.4V.

PCM Interface

u/A-law mode（Long Frame ,Short Frame） & Linear PCM mode

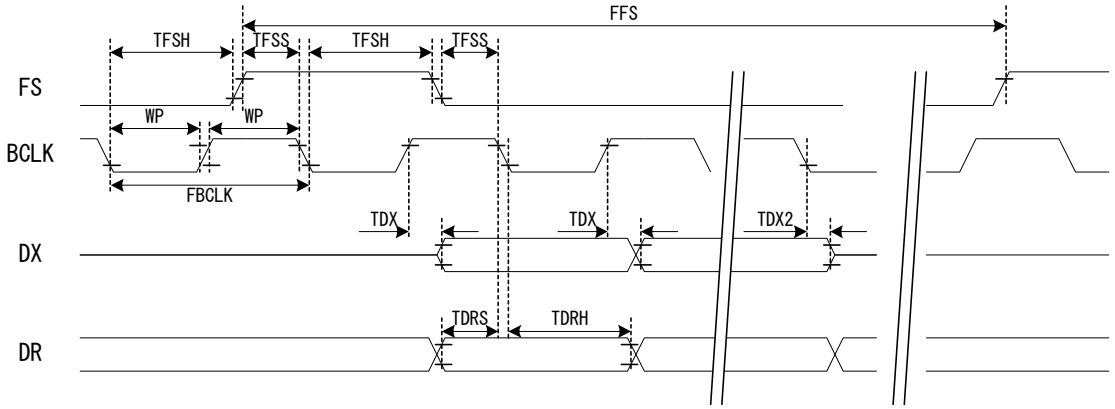
Items	Pin Name	Parm.	Conditions	MIN	TYP	MAX	Unit
FS frequency	FS	FFS	-	-	8	-	kHz
BCLK frequency Note1)	BCLK	FBCLK	-	-	64×N 128K X N	-	kHz
Clock width	BCLK	WP	-	160	-	-	ns
Falling/rising time	FS,BCLK,DR	TD	-	-	-	40	ns
Output delay	DX	TDX	Cl=50pF	-	-	60	ns
	DX	TDX2	Cl=50pF	10	-	-	ns
Setup time	FS	TFSS	-	70	-	-	ns
	DR	TDRS	-	40	-	-	ns
Hold time	FS	TFSH	-	40	-	-	ns
	DR	TDRH	-	40	-	-	ns
FS Low level width	FS	TWLFS	-	1	-	-	BCLK

Note1） Short Frame:64 x N kHz (N=1 to 32), Long Frame:64 x N kHz(N=1 to 32), Linear mode:128 x N kHz(N=1to 16)

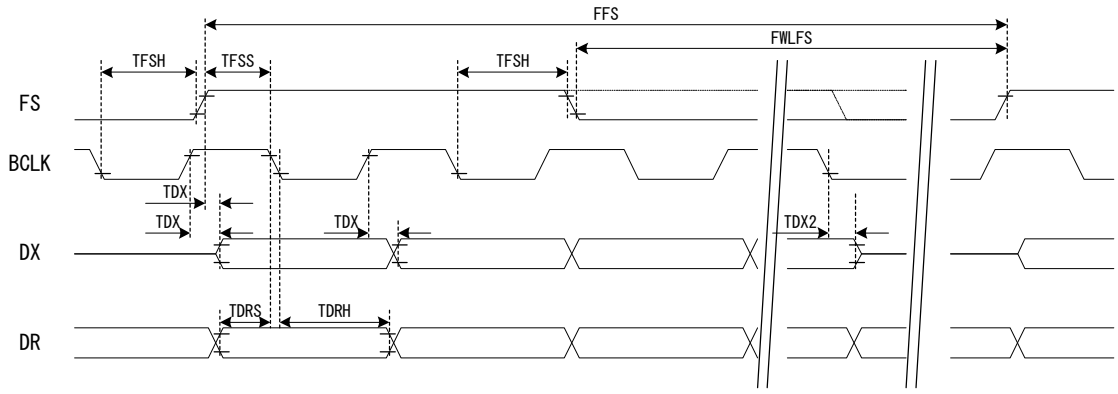
AK130 B1ch/B2ch mode

Items	Pin Name	Parm.	Conditions	MIN	TYP	MAX	Unit
FS frequency	FS	FFS	-	-	8	-	kHz
Clock frequency	BCLK	FBCLK	-	-	2.048	-	kHz
Pulse width	BCLK	WP	-	-	244	-	ns
Falling/Rising time	FS,BCLK,DR	TD	-	-	-	40	ns
Output delay	DX	TDX	CL=50pF	-	-	60	ns
	DX	TDX2	CL=50pF	10	-	60	ns
Setup time	FS	TFSS	-	70	-	-	ns
	DR	TDRS	-	40	-	-	ns
Hold time	FS	TFSH	-	40	-	-	ns
	DR	TDRH	-	40	-	-	ns

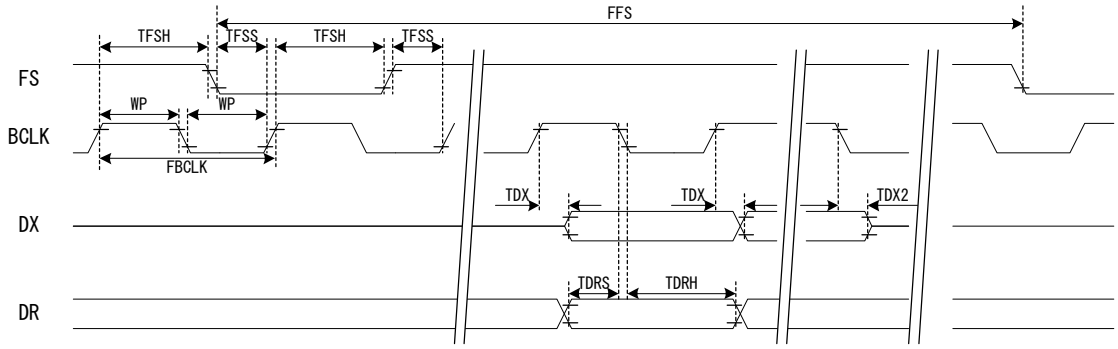
u/A-law PCM mode（Short Frame） & Linear PCM mode



u/A law PCM mode（Long Frame）



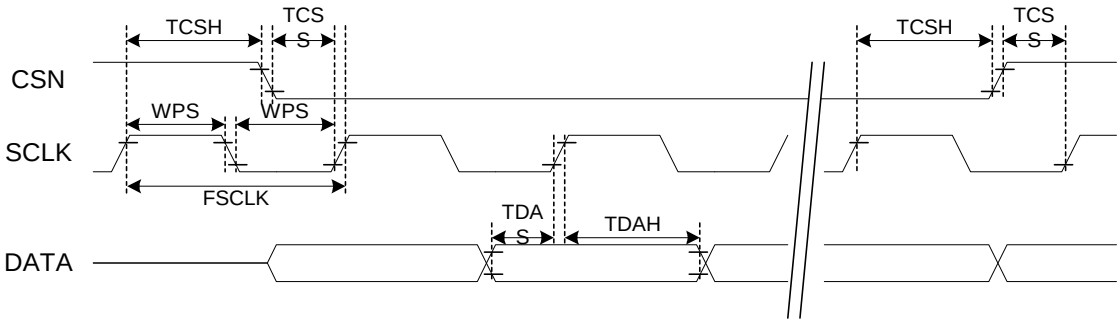
AK130 B1ch/B2ch mode



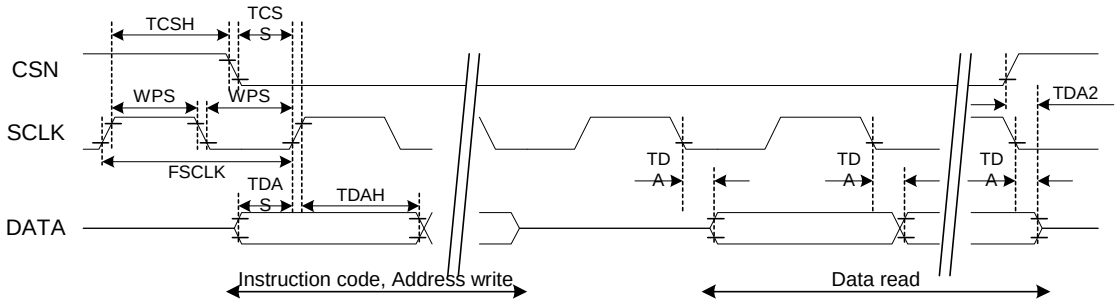
CPU I/F

Items	Pin Name	Parm.	Conditions	MIN	TYP	MAX	Unit
SCLK frequency	SCLK	FSCLK	-	-	-	4	MHz
SCLK pulse width	SCLK	WPS	-	40	-	-	ns
Falling/rising time	CSN,SCLK	TD	-	-	-	100	ns
Output delay	DATA	TDA	CL=15pF	-	-	60	ns
	DATA	TDA2	CL=15pF	-	-	60	Ns
Setup time	CSN	TCSS	-	40	-	-	ns
	DATA	TDAS	-	40	-	-	ns
Hold time	CSN	TCSH	-	80	-	-	ns
	DATA	TDAH	-	40	-	-	ns

Data write cycle



Data read cycle



Absolute Gain (AK2307:VDD=5.0V +/-5%, AK2307LV:VDD=3.3V +/-0.3V)

Parameter	Conditions		Min	Typ	Max	Units
Analog Input Level	HANDT4 to DX MIC3 to DX 1020Hz 0dBm0 input	AK2307LV		0.101		Vrms
		AK2307		0.162		
Absolute Transmit Gain		u/A-law	-1.5	-	+1.5	dB
Analog Output Level	DR to DAOUT 1020Hz 0dBm0 input	AK2307LV		0.482		Vrms
		AK2307		0.771		
Absolute Receive Gain		u/A-law	-1.5	-	+1.5	dB
Maximum Overload Level	DR to DAOUT +3.14dBm0 input	AK2307LV		0.694		Vrms
		AK2307		1.107		

Gain Tracking

Parameter	Conditions		Min	Typ	Max	Units
Transmit Gain Tracking Error	Reference Level:	-51dBm0 ~-46dBm0	-0.9	-	0.9	
(A to D)	-10dBm0	-46dBm0 ~-36dBm0	-0.6	-	0.6	dB
	1020Hz Tone	-36dBm0 ~ 0dBm0	-0.4	-	0.4	
Receive Gain Tracking Error	Reference Level:	-51dBm0 ~-46dBm0	-0.9	-	0.9	
(D to A)	-10dBm0	-46dBm0 ~-36dBm0	-0.6	-	0.6	dB
	1020Hz Tone	-36dBm0 ~ 0dBm0	-0.4	-	0.4	

The characteristics from MIC3 to DR path is guaranteed by the design.

Frequency Response

Parameter	Conditions		Min	Typ	Max	Units
Transmit Frequency Response	Relative to:	0.06kHz	24	-	-	
(A to D)	0dBm0@1020Hz	0.2kHz	0	-	2.5	
		0.3 ~3.0kHz	-0.3	-	0.3	dB
HANDT4 to DX		3.4kHz	0	-	0.8	
MIC3 to DX		3.78kHz	6.5	-	-	
Receive Frequency Response	Relative to:	0.3K ~3.0kHz	-0.3	-	0.3	
(D to A)	0dBm0@1020Hz	3.4kHz	0	-	0.8	dB
DR to DAOUT		3.78kHz	6.5	-	-	

Distortion

Parameter	Conditions		Min	Typ	Max	Units
Transmit Signal to Distortion	1020Hz Tone	-36dBm0 ~-41dBm0	24	-	-	
(D to A)		-26dBm0 ~-36dBm0	29	-	-	dB
HANDT4 to DX MIC3 to DX		0dBm0 ~-26dBm0	35	-	-	
Receive Signal to Distortion	1020Hz Tone	-36dBm0 ~-41dBm0	24	-	-	
(A to D)		-26dBm0 ~-36dBm0	29	-	-	dB
DR to DAOUT		0dBm0 ~-26dBm0	35	-	-	

Note) C-message Weighted for u-Law, Psophometric Weighted for A-Law
Note) The characteristics from MIC3 to DR path is guaranteed by the design.

Noise

Parameter	Conditions	Min	Typ	Max	Units
Idle Channel Noise [1)]	u-law, C-message	-	8	16	dBrnC0
A!D					
HANDT2,3 to DX	A-law, Psophometric	-	-82	-74	dBm0p
MIC2 to DX					
Idle Channel Noise [2)]	u-law, C-message	-	2	9	dBrnC0
D!A	A-law, Psophometric	-	-88	-81	dBm0p
DR to DAOUT					
Idle Channel Noise [2)]	u-law, C-message	-	3	16	dBrnC0
D!A	A-law, Psophometric	-	-87	-74	dBm0p
DR to HANDR1					

Note 1) Analog Input = Analog Ground. The gain of Handset MIC and MIC input is assumed as +25dB.
SCLK is not supplied. The specification of MIC to DX pass is guaranteed by the design.
Note 2) Digital Input(DR) = +0 Code

Interchannel Crosstalk

Parameter	Conditions	Min	Typ	Max	Units
Transmit to Receive	0dBm0@HANDT4, Idle PCM code@DR	-	-70	-	dB
HANDT4 to DAOUT					
MIC3 to DAOUT					
Receive to Transmit	0dBm0 code@DR, HANDT4 = 0 Vrms	-	-70	-	dB

RX voice path Volume

Parameter	Volume	Conditions	Min	typ	max	Unit
Step margin	VOL2	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0*)	dB
	VOL3	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0*)	dB
	VOL5 0 to –22dB	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0	dB
	VOL5 -22 to –30dB	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.5	0	+1.5*)	dB

*)Monotonus increase/decrease is guaranteed

TX voice path Volume

Parameter	Volume	Conditions	Min	typ	max	Unit
Step margin	VOL1	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0*)	dB

*)Monotonus increase/decrease is guaranteed

Tone Volume

Parameter	Volume	Conditions		Min	typ	max	Unit
Step margin	VOL4	Output; HANDR1 1600Hz tone , Ref level;VOL4=0dB	0 to –24dB	-1.0	0	+1.0	dB
			-27 to –45dB	-2.0	0	+2.0*)	dB
Gain error	L-ATT	L-ATT=-2.5dB		-1.0	0	+1.0	dB

*)Monotonus increase/decrease is guaranteed

OP-AMPs

Note) Otherwise specified, the VOL2 ,3 and 5 is 0dB gain.

RX Amp for Handset receiver

		Conditions	MIN	TYP	MAX	Unit
Maximum output level	RAIN →HANDR1 SINAD<40dB, 1020Hz	AK2307LV (150ohm load)	2.0	-	-	Vp-p
		(75ohm load)	1.5	-	-	
		AK2307 (150ohm load)	3.2	-	-	
		(75ohm load)	2.4	-	-	

Note) when HANDR1 and HEADO are used as a differential output for 150 ohm receiver, the load impedance for the each output is calculated as 75 ohm.

RX Amp for Headset receiver

		Conditions	MIN	TYP	MAX	Unit
Maximum output level	RAIN →HEADO SINAD<40dB, 1020Hz	AK2307LV (150ohm load)	2.0	-	-	Vp-p
		(75ohm load)	1.5	-	-	
		AK2307 (150ohm load)	3.2	-	-	
		(75ohm load)	2.4	-	-	

Note) when HANDR1 and HEADO are used as a differential output for 150 ohm receiver, the load impedance for the each output is calculated as 75 ohm.

RX Amp for Speaker output

		Conditions	MIN	TYP	MAX	Unit
Maximum output level	RAIN, EXRIN →SPO*) SINAD<40dB, 1020Hz	AK2307LV	2.0	-	-	Vp-p
		AK2307	3.2	-	-	

*Note） A Characteristics from EXRIN input is guaranteed by the design.

TX Amp for Handset MIC input

		Conditions	MIN	TYP	MAX	Unit
Maximum output level	HANDT1 SINAD<40 dB Mic gain=25dB at 1020Hz	AK2307LV	0.411	-	-	Vp-p
		AK2307	0.660	-	-	
Maximum gain		Inverting amplify	0	-	25	dB

TX Amp for MIC input

		Conditions	MIN	TYP	MAX	Unit
Maximum output level	MIC1 SINAD<40 dB Gain=25dB at 1020Hz	AK2307LV	0.411	-	-	Vp-p
		AK2307	0.660	-	-	
Maximum gain		Inverting amplify	0	-	25	dB

Tone signal

Output level

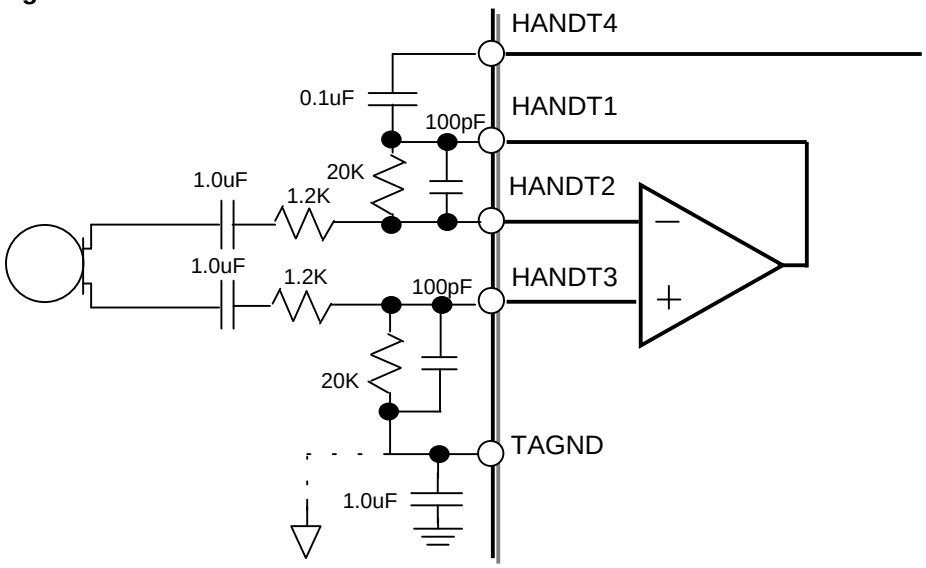
	Conditions		MIN	TYP	MAX	Unit
Output level to RX path	HANDR HEADO SPO 1600Hz VOL4=0dB	AK2307LV	420	500	595	mVrms
		AK2307	672	800	952	
Output level to TX path	DX 1049Hz VOL4=0dB	AK2307/LV		0		dBm0

Input Impedance

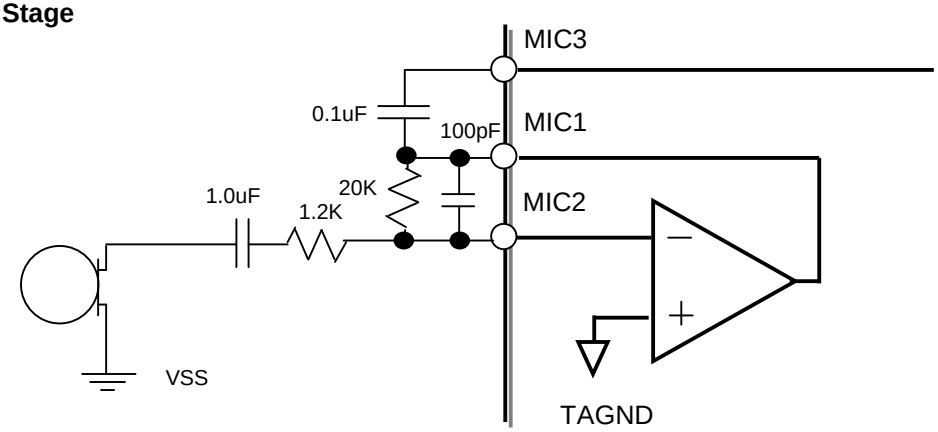
Pin	MIN	TYP	MAX	Unit
EXRIN、RAIN	70K	100K	150K	ohm
HANDT4、MIC3	7K	10K	15K	

APPLICATION CIRCUIT EXAMPLE

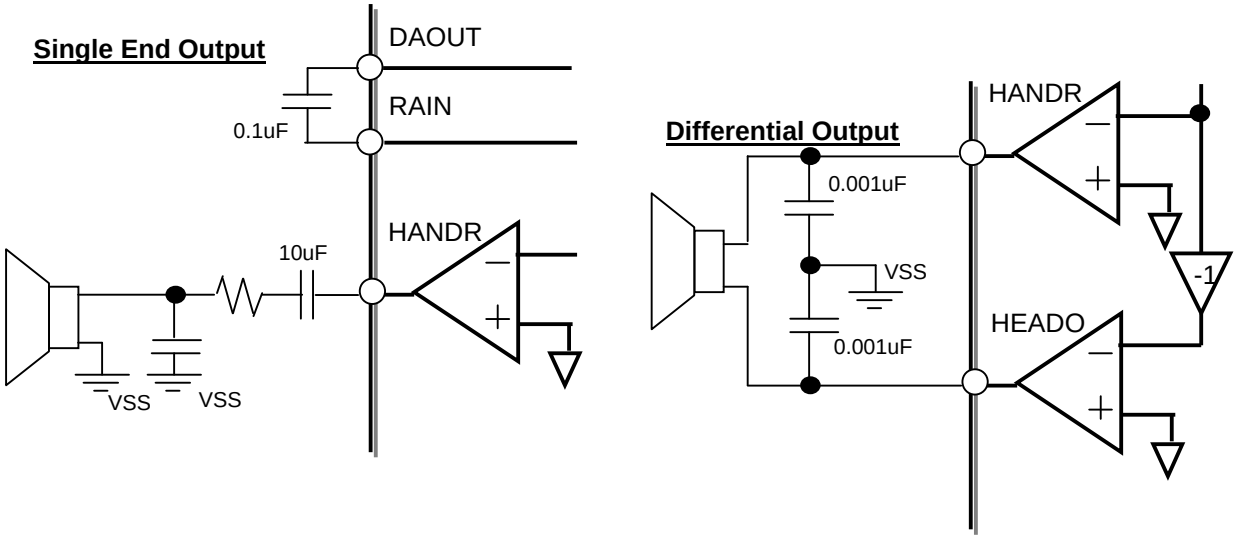
I Handset Input Stage



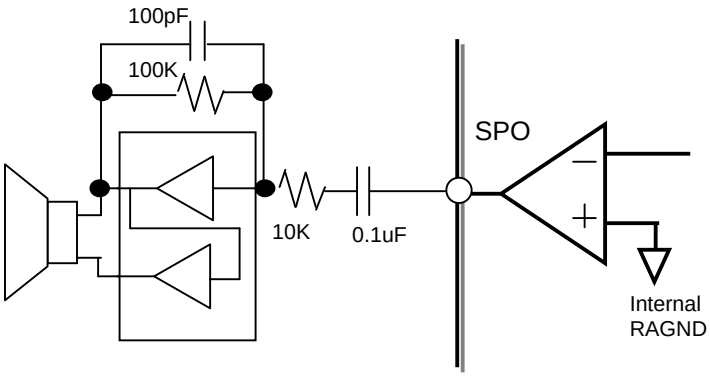
I MIC amp Input Stage



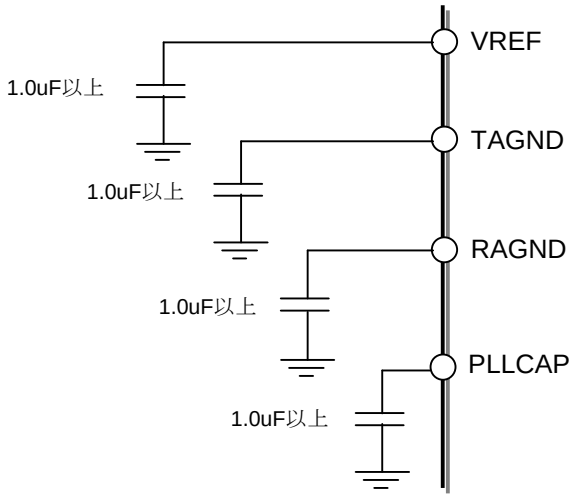
I Handset Receiver output Stage



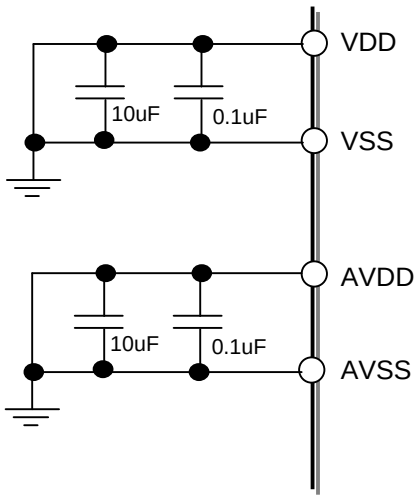
Speaker Amp Output Stage



l Analog Ground, PLLCAP



l Power Supplies

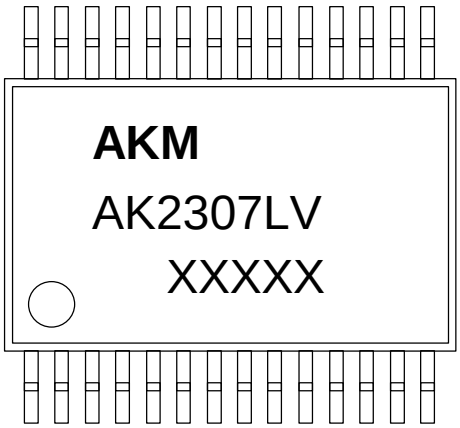


PACKAGE

28pin VSOP
Marking

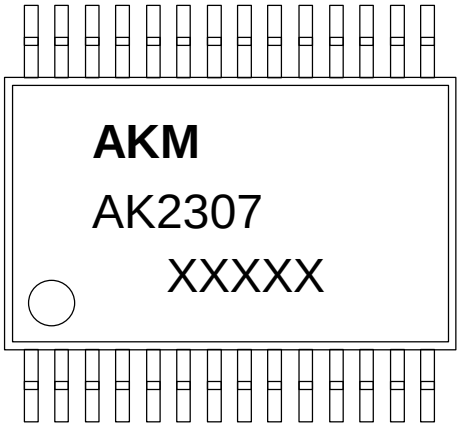
(1) Pin#1 indicator
(2) Date code: XXXXX（5digit）
(3) Marketing code: AK2307LV/AK2307
(4) AKM Logo

AK2307LV



XXXXX: Date Code and Lot#

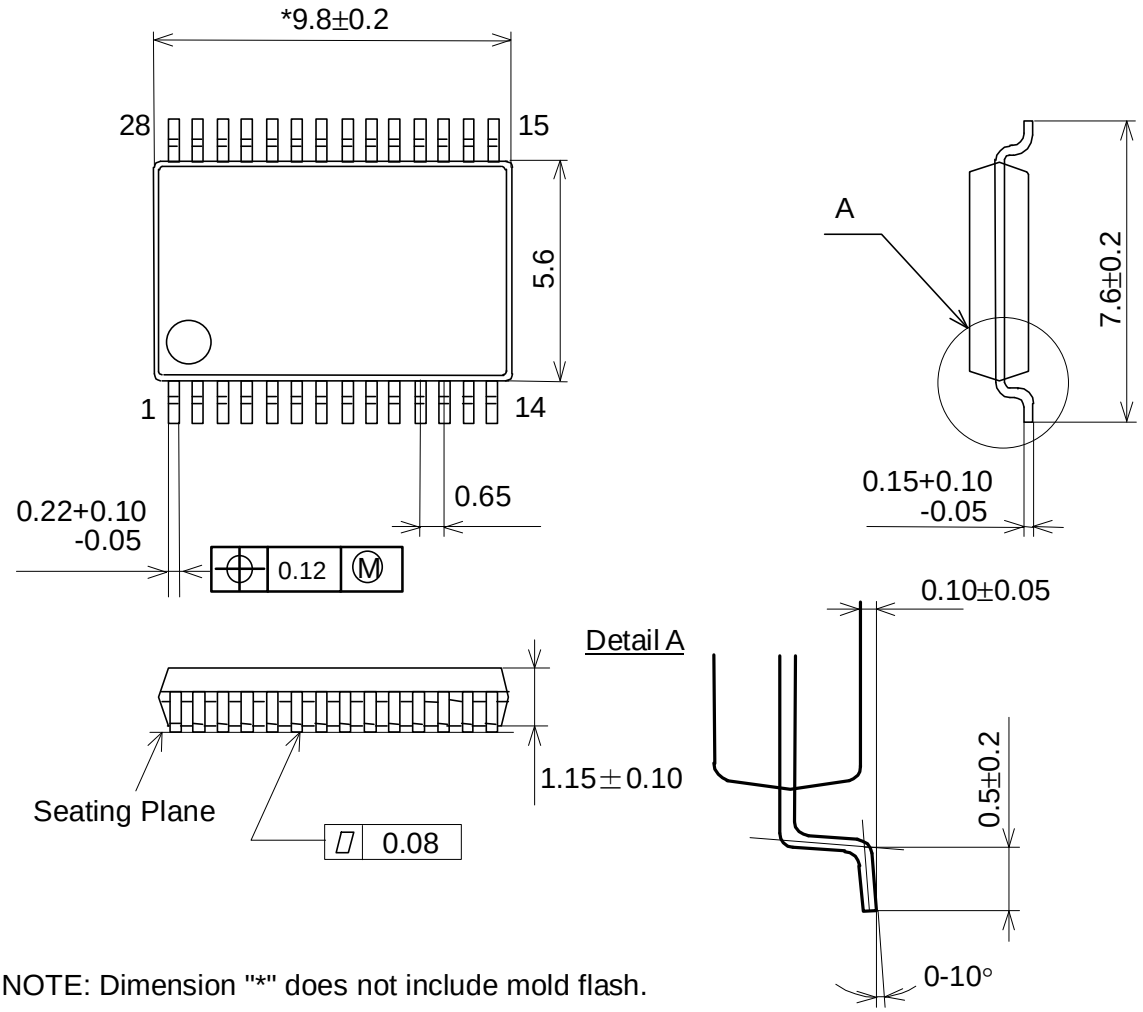
AK2307



XXXXX: Date Code and Lot#

Package dimensions

28pin VSOP (Unit: mm)



NOTE: Dimension "*" does not include mold flash.

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