QPRO™ Family of XC1700D QML Serial Configuration PROMs

February 8, 1999 (Version 2.0)

Product Specification

Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing.)
- Also available under the following Standard Microcircuit Drawings (SMD): 5962-94717 and 5962-95617.
- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- The XQ1701L device is specified on a different datasheet. It supports the XQ4000EX/XL/XLA fast configuration mode (15.0 MHz).
- Low-power CMOS EPROM process
- Available in 5 V version only, the XQ1701L is available in 3.3V only
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The XC1700D Hi-rel family of serial configuration PROMs (SPROMs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When the FPGA is in Slave Serial mode, the SPROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the FPGA design file into a standard HEX format which is then transferred to most commercial PROM programmers.

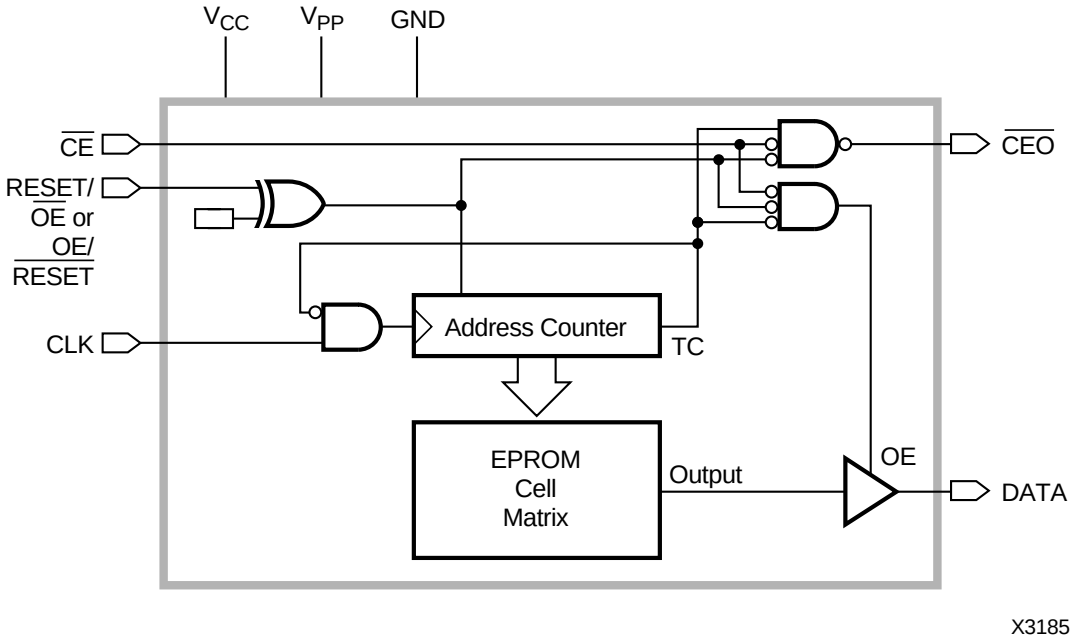


Figure 1: Simplified Block Diagram (does not show programming circuit)

Pin Description

DATA

Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGA's $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.

$\overline{CE}$

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next SPROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave VPP floating!*

V_{CC} and GND

V_{CC} is positive supply pin and GND is ground pin.

Serial PROM Pinouts

Pin Name	8-Pin
DATA	1
CLK	2
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3
$\overline{CE}$	4
GND	5
$\overline{CEO}$	6
V_{PP}	7
V_{CC}	8

Capacity

Device	Configuration Bits
XC1736D	36,288
XC1765D	65,536
XC17128D	131,072
XC17256D	262,144
XQ1701L	1,048,576

Note: The XQ1701L SPROMs are specified in a separate datasheet.

Number of Configuration Bits, Including Header for Xilinx FPGAs and Compatible SPROMs

Device	Configuration Bits	SPROM
XC3000/A series	14,819 to 94,984	XC1765D to XC17128D
XC4000 series	95,008 to 247,968	XC17128D to XC17256D
XQ4005E	95,008	XC17128D
XQ4010E	178,144	XC17256D
XQ4013E	247,968	XC17256D
XQ4025E	422,176	XQ1701L
XQ4013XL	393,632	XQ1701L
XQ4028EX	668,184	XQ1701L
XQ4036XL	832,528	XQ1701L
XQ4062XL	1,433,864	XQ1701L x 2

Note: The XQ1701L SPROMs are specified in a separate datasheet.

Controlling Serial PROMs

Connecting the FPGA device with the SPROM.

- The DATA output(s) of the SPROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the SPROM(s).
- The $\overline{CEO}$ output of a SPROM drives the $\overline{CE}$ input of the next SPROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all SPROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the SPROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods – such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset – assume the SPROM internal power-on-reset is always in step with the FPGA's internal power-on-reset. This may not be a safe assumption.
- The SPROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the DIN pin.
- The $\overline{CE}$ input of the lead (or only) SPROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx SPROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the SPROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the SPROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. Xilinx FPGAs take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a SPROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the SPROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Serial Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded SPROMs provide additional memory. After the last bit from the first SPROM is read, the next clock signal to the SPROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SPROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SPROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the SPROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

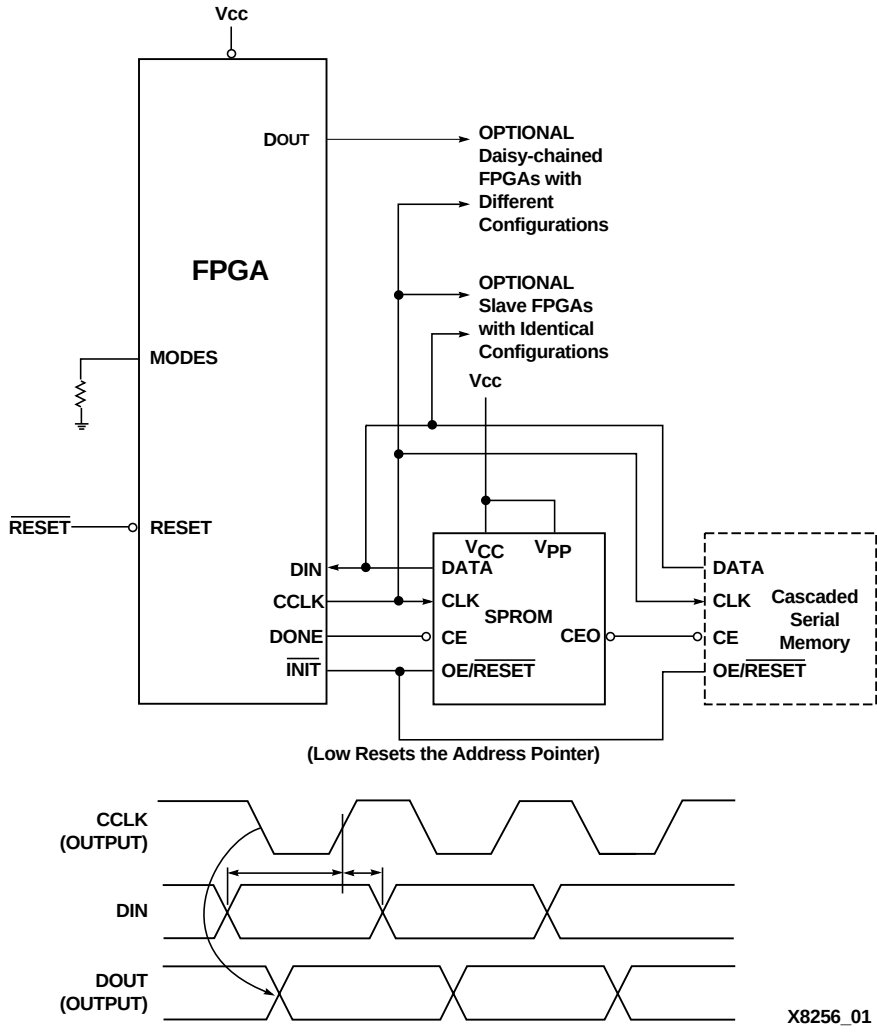


Figure 2: Master Serial Mode. The one-time-programmable SPROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the SPROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The SPROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 1: Truth Table for XC1700 Control Inputs

Control Inputs		Internal Address	Outputs		
RESET	CE		DATA	CEO	I_{cc}
Inactive	Low	if address ≤ TC: increment if address > TC: don't change	active 3-state	High Low	active reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

Notes: 1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC+1 = address 0.

Important: Always tie the V_{PP} pin to V_{CC} in your application. Never leave V_{PP} floating.

XC1736D, XC1765D, XC17128D and XC17256D

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

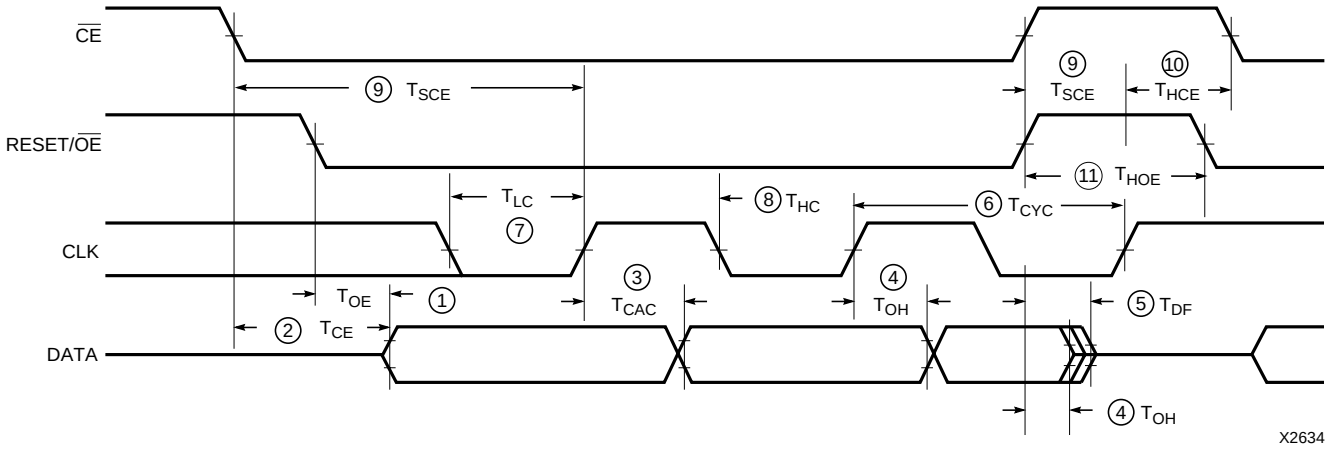
Symbol	Description		Min	Max	Units
V_{CC}	Military	Supply voltage relative to GND (T_C = -55°C to +125°C)	4.50	5.50	V

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)			10.0	mA
I_{CCS}	Supply current, standby mode	XC17128D, XC17256D		50.0	µA
		XC1736D, XC1765D		1.5	mA
I_L	Input or output leakage current		-10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0MHz) Sample tested			10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0MHz) Sample tested			10.0	pF

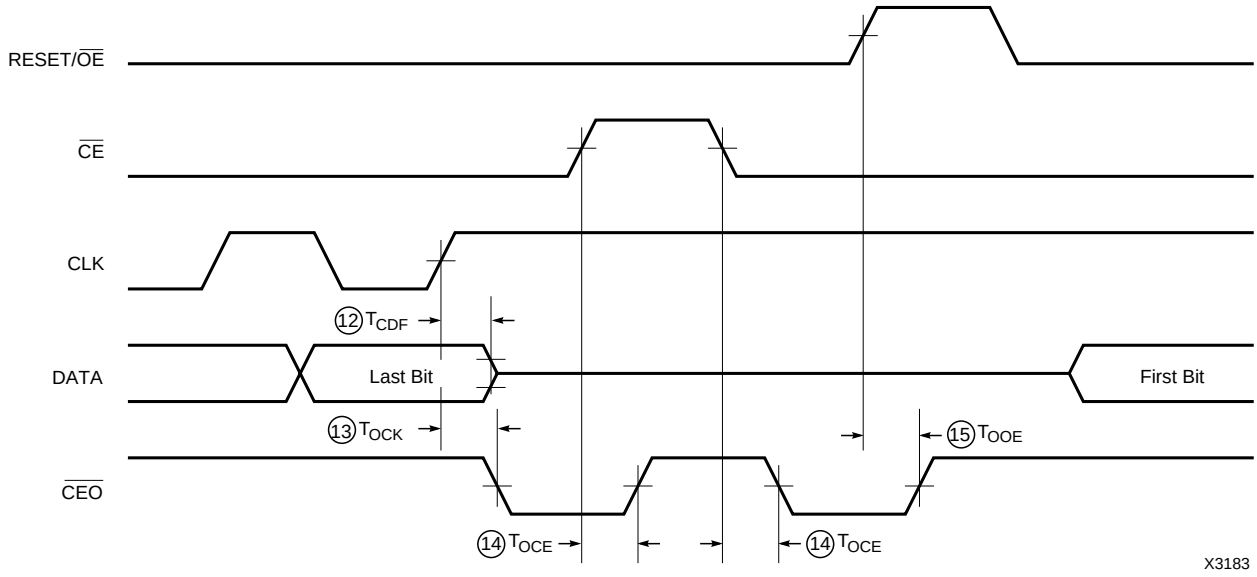
AC Characteristics Over Operating Condition



Symbol		Description	XC1736D XC1765D		XC17128D XC17256D		Units
			Min	Max	Min	Max	
1	T_{OE}	$\overline{OE}$ to Data Delay		45		25	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60		45	ns
3	T_{CAC}	CLK to Data Delay		150		50	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK[3]	0		0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2 & 3]		50		50	ns
6	T_{CYC}	Clock Periods	200		80		ns
7	T_{LC}	CLK Low Time[3]	100		20		ns
8	THC	CLK High Time[3]	100		20		ns
9	TSCE	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		20		ns
10	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		ns
11	T_{HOE}	$\overline{OE}$ Hold Time (guarantees counters are reset)	100		20		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

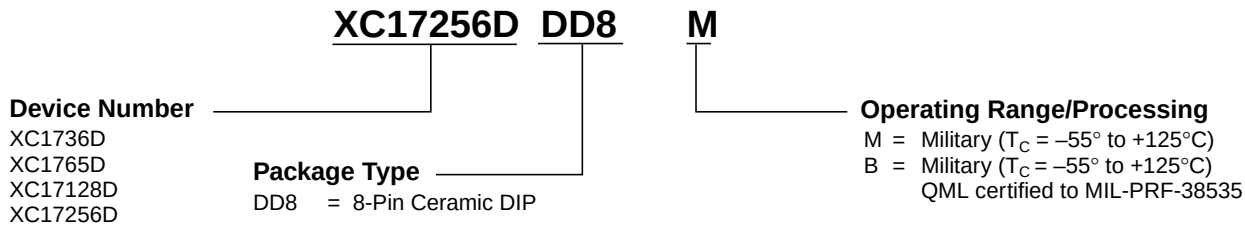
AC Characteristics Over Operating Condition When Cascading



Symbol		Description	XC1736D XC1765D		XC17128D XC17256D		Units
			Min	Max	Min	Max	
12	T_{CDF}	CLK to Data Float Delay[2, 3]		50		50	ns
13	T_{OCK}	CLK to $\overline{CEO}$ Delay[3]		65		30	ns
14	T_{OCE}	CE to $\overline{CEO}$ Delay[3]		45		35	ns
15	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay[3]		40		30	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

Ordering Information



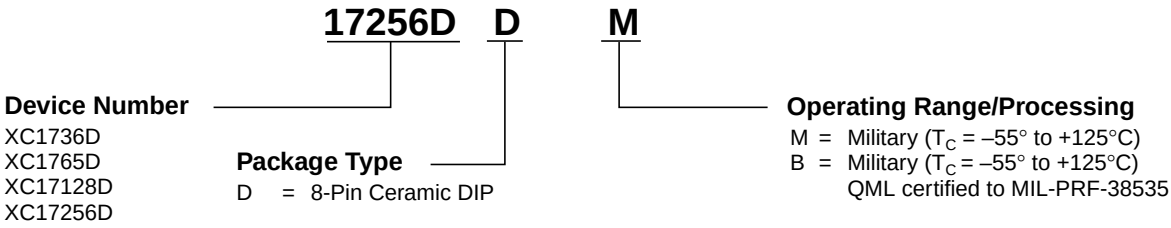
Valid Ordering Combinations

XC17128DDD8M	XC17256DDD8M	XC1736DDD8M	XC1765DDD8M	XQ1701LCC44M
	5962-9561701MPA		5962-9471701MPA	XQ1701LSO20N

Note: The XQ1701L products are specified in the XC1700L High Density datasheet.

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.



Revision Control

Date	Revision
2/8/99	Removed the now obsolete Commercial and Industrial Grade part numbers and design support.