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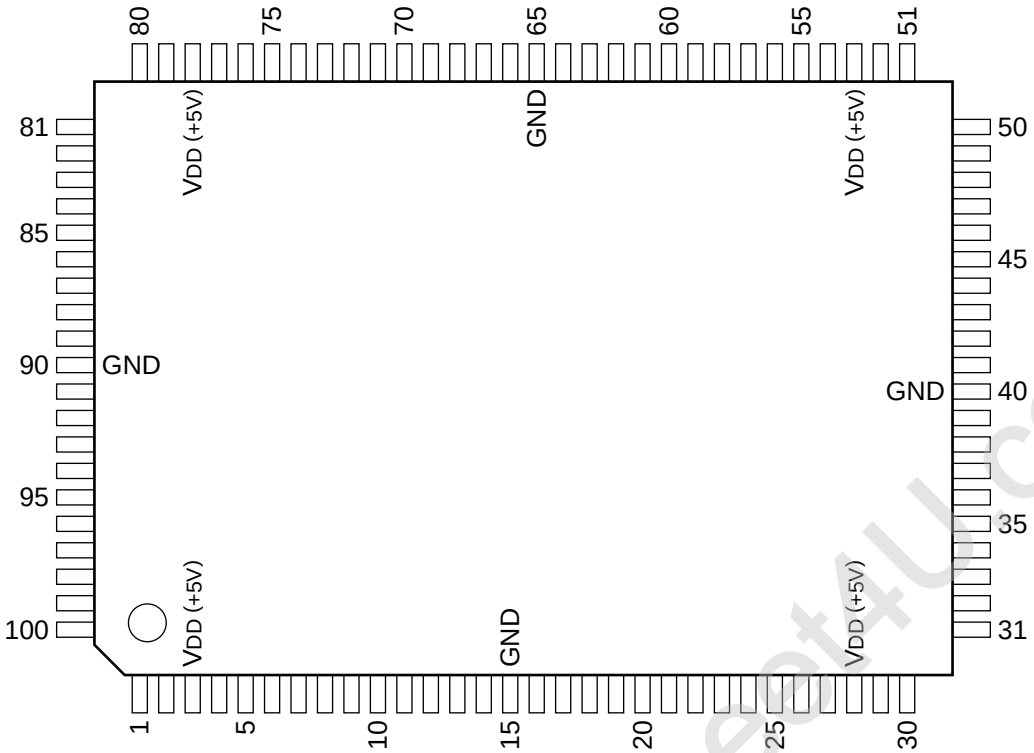
IL22

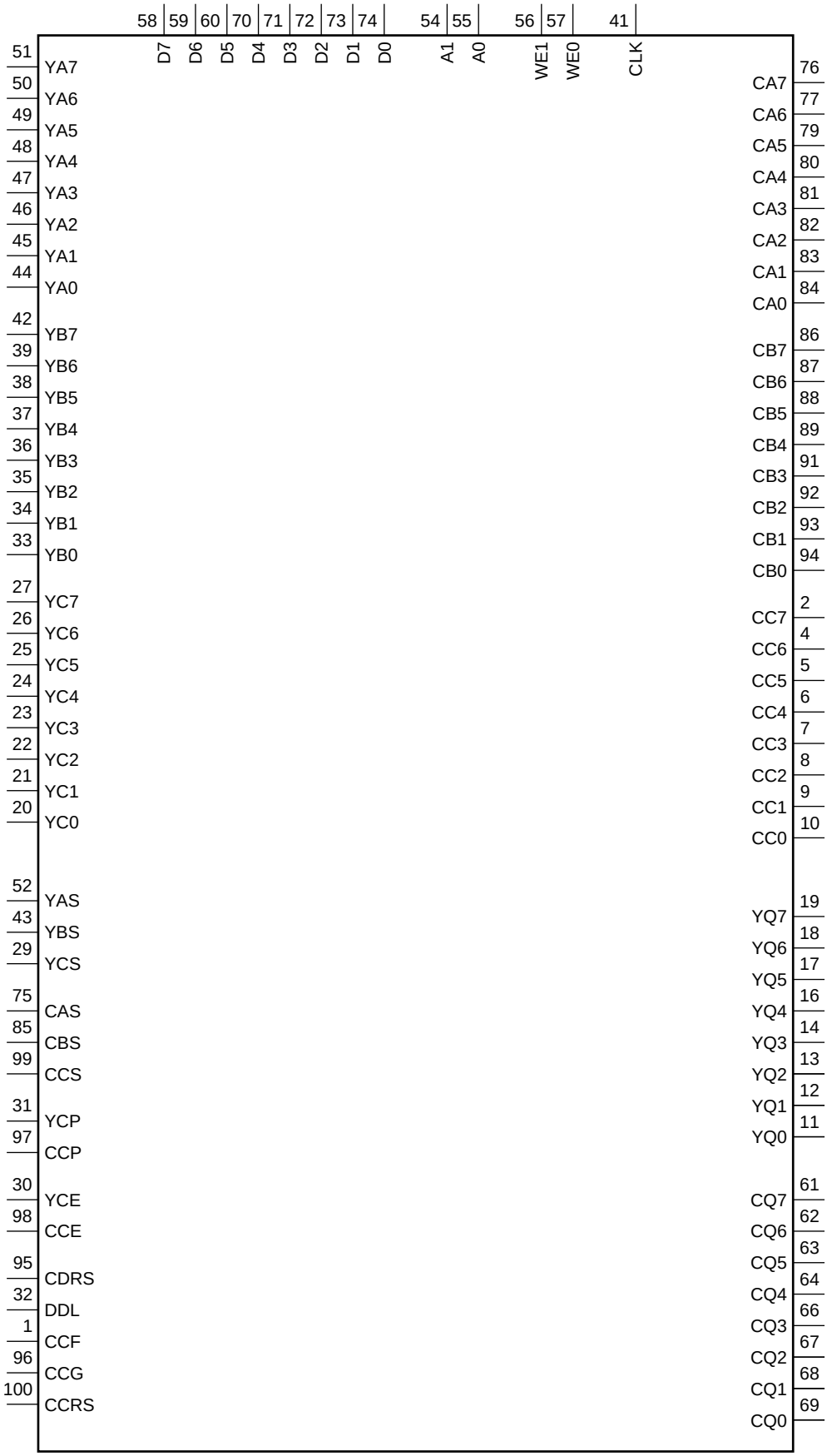
C-MOS DIGITAL MIX EFFECTS

-TOP VIEW-



(VDD = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	CCF	21	I	YC1	41	I	CLK	61	O	CQ7	81	I	CA3
2	I	CC7	22	I	YC2	42	I	YB7	62	O	CQ6	82	I	CA2
3	—	VDD	23	I	YC3	43	I	YBS	63	O	CQ5	83	I	CA1
4	I	CC6	24	I	YC4	44	I	YA0	64	O	CQ4	84	I	CA0
5	I	CC5	25	I	YC5	45	I	YA1	65	—	GND	85	I	CBS
6	I	CC4	26	I	YC6	46	I	YA2	66	O	CQ3	86	I	CB7
7	I	CC3	27	I	YC7	47	I	YA3	67	O	CQ2	87	I	CB6
8	I	CC2	28	—	VDD	48	I	YA4	68	O	CQ1	88	I	CB5
9	I	CC1	29	I	YCS	49	I	YA5	69	O	CQ0	89	I	CB4
10	I	CC0	30	I	YCE	50	I	YA6	70	I	D4	90	—	GND
11	O	YQ0	31	I	YCP	51	I	YA7	71	I	D3	91	I	CB3
12	O	YQ1	32	I	DDL	52	I	YAS	72	I	D2	92	I	CB2
13	O	YQ2	33	I	YB0	53	—	VDD	73	I	D1	93	I	CB1
14	O	YQ3	34	I	YB1	54	I	A1	74	I	D0	94	I	CB0
15	—	GND	35	I	YB2	55	I	A0	75	I	CAS	95	I	CDRS
16	O	YQ4	36	I	YB3	56	I	WE1	76	I	CA7	96	I	CCG
17	O	YQ5	37	I	YB4	57	I	WE0	77	I	CA6	97	I	CCP
18	O	YQ6	38	I	YB5	58	I	D7	78	—	VDD	98	I	CCE
19	O	YQ7	39	I	YB6	59	I	D6	79	I	CA5	99	I	CCS
20	I	YC0	40	—	GND	60	I	D5	80	I	CA4	100	I	CCRS

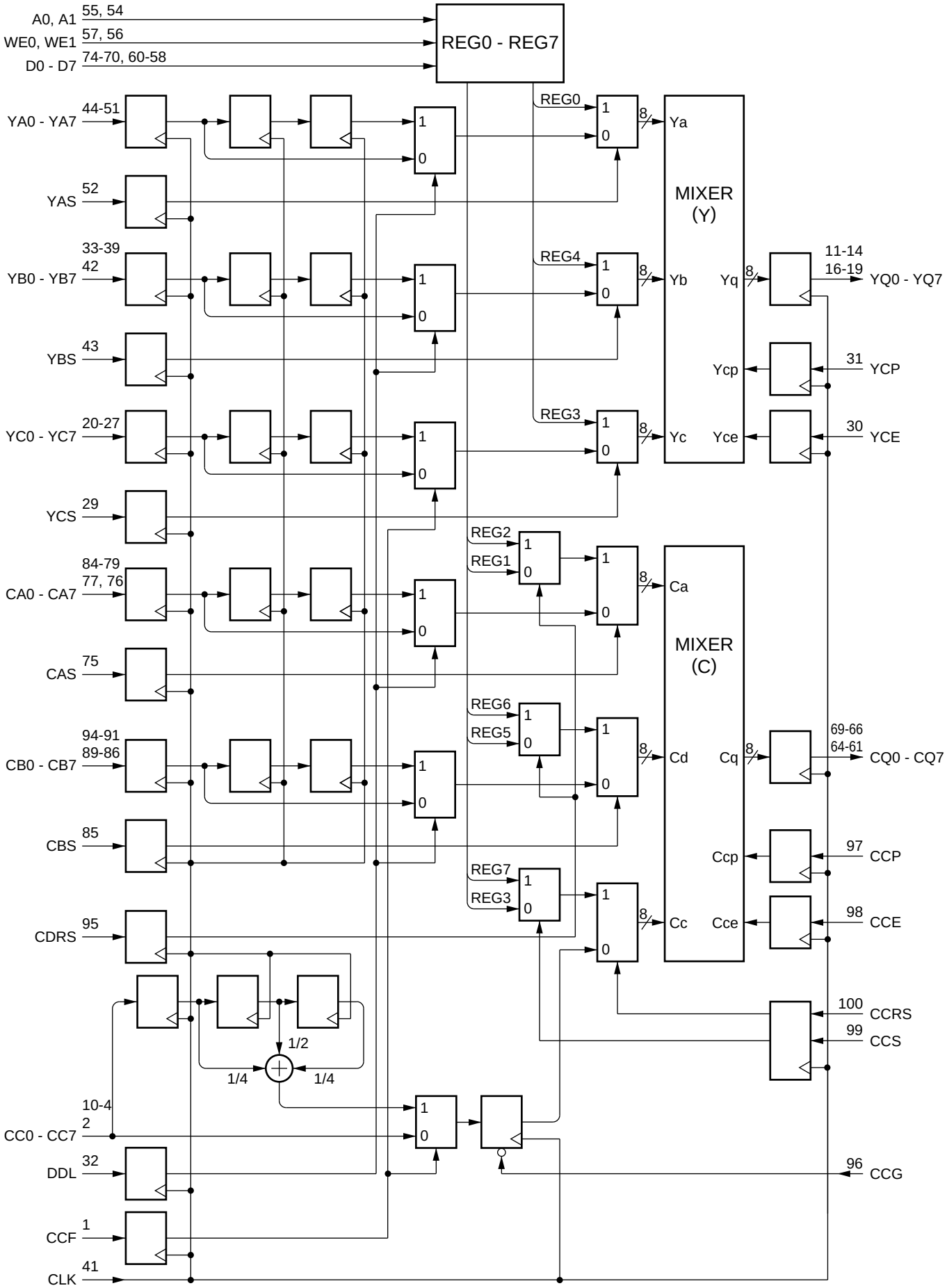

58 D7
59 D6
60 D5
70 D4
71 D3
72 D2
73 D1
74 D0
54 A1
55 A0
56 WE1
57 WE0
41 CLK
51 YA7
50 YA6
49 YA5
48 YA4
47 YA3
46 YA2
45 YA1
44 YA0
42 YB7
39 YB6
38 YB5
37 YB4
36 YB3
35 YB2
34 YB1
33 YB0
27 YC7
26 YC6
25 YC5
24 YC4
23 YC3
22 YC2
21 YC1
20 YC0
52 YAS
43 YBS
29 YCS
75 CAS
85 CBS
99 CCS
31 YCP
97 CCP
30 YCE
98 CCE
95 CDRS
32 DDL
1 CCF
96 CCG
100 CCRS
76 CA7
77 CA6
79 CA5
80 CA4
81 CA3
82 CA2
83 CA1
84 CA0
86 CB7
87 CB6
88 CB5
89 CB4
91 CB3
92 CB2
93 CB1
94 CB0
2 CC7
4 CC6
5 CC5
6 CC4
7 CC3
8 CC2
9 CC1
10 CC0
19 YQ7
18 YQ6
17 YQ5
16 YQ4
14 YQ3
13 YQ2
12 YQ1
11 YQ0
61 CQ7
62 CQ6
63 CQ5
64 CQ4
66 CQ3
67 CQ2
68 CQ1
69 CQ0

INPUT

A0, A1	;	INTERNAL REGISTER ADDRESS
CA0 - CA7	;	MIXER (C) A DATA
CAS	;	MIXER (C) A DATA SELECTOR
CB0 - CB7	;	MIXER (C) B DATA
CBS	;	MIXER (C) B DATA SELECTOR
CC0 - CC7	;	MIXER (C) C DATA
CCE	;	MIXER (C) C ENABLE
CCF	;	MIXER (C) PRE FILTER CONTROL
CCG	;	MIXER (C) C GATE
CCP	;	MIXER (C) C POLARITY
CCRS	;	MIXER (C) C REGISTER SELECTOR
CCS	;	MIXER (C) C DATA SELECTOR
CDRS	;	C DATA REGISTER SELECTOR
CLK	;	CLOCK
D0 - D7	;	INTERNAL REGISTER DATA
DDL	;	DATA DELAY CONTROL
WE0, WE1	;	INTERNAL REGISTER WRITE ENABLE
YA0 - YA7	;	MIXER (Y) A DATA
YAS	;	MIXER (Y) A DATA SELECTOR
YB0 - YB7	;	MIXER (Y) B DATA
YBS	;	MIXER (Y) B DATA SELECTOR
YC0 - YC7	;	MIXER (Y) C DATA
YCE	;	MIXER (Y) C ENABLE
YCP	;	MIXER (Y) C POLARITY
YCS	;	MIXER (Y) C DATA SELECTOR

OUTPUT

CQ0 - CQ7	;	MIXER (C) DATA OUTPUT
YQ0 - YQ7	;	MIXER (Y) DATA OUTPUT


A0, A1
55, 54
WE0, WE1
57, 56
D0 - D7
74-70, 60-58
REG0 - REG7
YA0 - YA7
44-51
YAS
52
YB0 - YB7
33-39
42
YBS
43
YC0 - YC7
20-27
YCS
29
CA0 - CA7
84-79
77, 76
CAS
75
CB0 - CB7
94-91
89-86
CBS
85
CDRS
95
CC0 - CC7
10-4
2
DDL
32
CCF
1
CLK
41
REG0
REG4
REG3
REG2
REG1
REG6
REG5
REG7
REG3
MIXER
(Y)
Ya
Yb
Yc
Yq
Ycp
Yce
MIXER
(C)
Ca
Cd
Cc
Cq
Ccp
Cce
11-14
16-19
YQ0 - YQ7
31
YCP
30
YCE
69-66
64-61
CQ0 - CQ7
97
CCP
98
CCE
100
CCRS
99
CCS
96
CCG
1/2
1/4
1/4