M16C/62 Group (M16C/62P, M16C/62PT)

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0001-0210Z
Rev.2.10
Nov. 07, 2003

1. Overview

The M16C/62 group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, office/communications/portable/industrial equipment, automobile, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 to table 1.3 list performance outline of M16C/62 group (M16C/62P, M16C/62PT).

Table 1.1 Performance outline of M16C/62 group (M16C/62P) (128-pin version)

	Item	Performance
		M16C/62P
CPU	Number of basic instructions	91 instructions
	Shortest instruction execution time	41.7ns(f(BCLK)=24MHz, VCC1=3.0 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)
	Operation mode	Single-chip, memory expansion and microprocessor mode
	Memory space	1 Mbyte (Available to 4M bytes by memory space expansion function)
	Memory capacity	See **table 1.4 and 1.5 Product List**
Peripheral function	Port	Input/Output : 113 pins, Input : 1 pin
	Multifunction timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels Three phase motor control circuit
	Serial I/O	3 channels Clock synchronous, UART, I^2C bus (1), IEBus (2) 2 channels Clock synchronous
	A-D converter	10-bit A-D converter: 1 circuit, 26 channels
	D-A converter	8 bits x 2 channels
	DMAC	2 channels
	CRC calculation circuit	CCITT-CRC
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels
	Clock generating circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), Ring oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.
	Oscillation stop detection function	Stop detection of main clock oscillation, re-oscillation detection function
	Voltage detection circuit	Available (option (4))
Electric characteris-tics	Supply voltage	VCC1=3.0 to 5.5V, VCC2=2.7V to VCC1 (f(BCLK)=24MHz) VCC1=2.7 to 5.5V, VCC2=2.7V to VCC1 (f(BCLK)=10MHz)
	Power consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8 µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7 µ A (VCC1=VCC2=3V, stop mode)
Flash memory Version	Program/erase supply voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V
	Program and erase endurance	100 times (all area) or 1,000 times (user ROM area without block 1) / 10,000 times (block A, block 1) (3)
Operating ambient temperature		–20 to 85°C –40 to 85°C (3)
Package		128-pin plastic mold QFP

NOTES:

1. I^2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Oct., 2003. Please inquire about a release schedule.
4. All options are on request basis.

Table 1.2 Performance outline of M16C/62 group (M16C/62P, M16C/62PT) (100-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT (Note 4)
CPU	Number of basic instructions	91 instructions	
	Shortest instruction execution time	41.7ns(f(BCLK)=24MHz, VCC1=3.0 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operation mode	Single-chip, memory expansion and microprocessor mode	Single-chip mode
	Memory space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1M byte
	Memory capacity	See **table 1.4 to 1.7 Product List**	
Peripheral function	Port	Input/Output : 87 pins, Input : 1pin	
	Multifunction timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels Three phase motor control circuit	
	Serial I/O	3 channels Clock synchronous, UART, I^2C bus (1), IEBus (2) 2 channels Clock synchronous	
	A-D converter	10-bit A-D converter: 1 circuit, 26 channels	
	D-A converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC calculation circuit	CCITT-CRC	
	Watchdog timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels	
	Clock generating circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), Ring oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation stop detection function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage detection circuit	Available (option (5))	Absent
Electric characteris-tics	Supply voltage	VCC1=3.0 to 5.5V, VCC2=2.7V to VCC1 (f(BCLK)=24MHz) VCC1=2.7 to 5.5V, VCC2=2.7V to VCC1 (f(BCLK)=10MHz)	VCC1=VCC2=4.0V to 5.5 V (f(BCLK)=24MHz)
	Power consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8 µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7 µ A (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0 µA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8 µ A (VCC1=VCC2=5V, stop mode)
Flash memory Version	Program/erase supply voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and erase endurance	100 times (all area) or 1,000 times (user ROM area without block 1) / 10,000 times (block A, block 1) (3)	
Operating ambient temperature		–20 to 85°C –40 to 85°C (3)	T version : –40 to 85°C V version : –40 to 125°C
Package		100-pin plastic mold QFP, LQFP	

NOTES:
1. I^2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Oct., 2003. Please inquire about a release schedule.
4. Use the high reliability version on VCC1 = VCC2.
5. All options are on request basis.

Table 1.3 Performance outline of M16C/62 group (M16C/62P, M16C/62PT) (80-pin version)

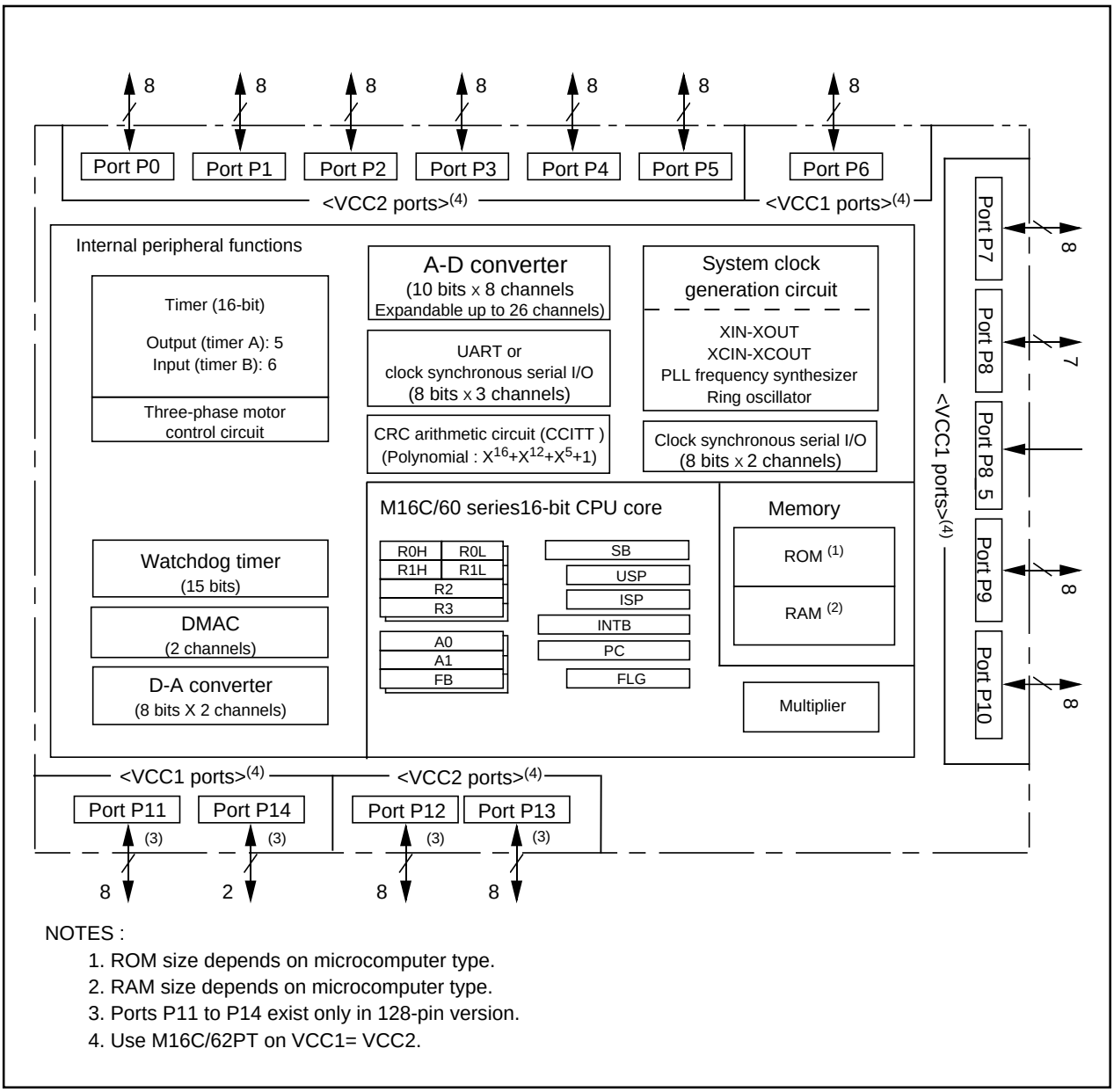
	Item	Performance	
		M16C/62P	M16C/62PT
CPU	Number of basic instructions	91 instructions	
	Shortest instruction execution time	41.7ns(f(BCLK)=24MHz, VCC1=3.0 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operation mode	Single-chip mode	
	Memory space	1M byte	
	Memory capacity	See t**able 1.4 to 1.7 Product List**	
Peripheral function	Port	Input/Output : 70 pins, Input : 1pin	
	Multifunction timer	Timer A : 16 bits x 5 channels (Timer A1 and A2 are internal timer) Timer B : 16 bits x 6 channels (Timer B1 is internal timer)	
	Serial I/O	2 channels Clock synchronous, UART, I^2C bus(1), IEBus(2) 1 channel Clock synchronous, I^2C bus(1), IEBus(2) 2 channels Clock synchronous (1 channel is only for transmission)	
	A-D converter	10-bit A-D converter: 1 circuit, 26 channels	
	D-A converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC calculation circuit	CCITT-CRC	
	Watchdog timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels	
	Clock generating circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), Ring oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation stop detection function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage detection circuit	Available (option (4))	Absent
Electric characteris-tics	Supply voltage	VCC1=3.0 to 5.5V, (f(BCLK)=24MHz) VCC1=2.7 to 5.5V, (f(BCLK)=10MHz)	VCC1=4.0 to 5.5V, (f(BCLK)=24MHz)
	Power consumption	14 mA (VCC1=5V, f(BCLK)=24MHz) 8 mA (VCC1=3V, f(BCLK)=10MHz) 1.8 µA (VCC1=3V, f(XCIN)=32kHz, wait mode) 0.7 µ A (VCC1=3V, stop mode)	14 mA (VCC1=5V, f(BCLK)=24MHz) 2.0 µA (VCC1=5V, f(XCIN)=32kHz, wait mode) 0.8 µ A (VCC1=5V, stop mode)
Flash memory Version	Program/erase supply voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and erase endurance	100 times (all area) or 1,000 times (user ROM area without block 1) / 10,000 times (block A, block 1) (3)	
Operating ambient temperature		–20 to 85°C –40 to 85°C(option)	T version : –40 to 85°C V version : –40 to 125°C
Package		80-pin plastic mold QFP	

NOTES :

1. I^2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Oct., 2003. Please inquire about a release schedule.
4. All options are on request basis.

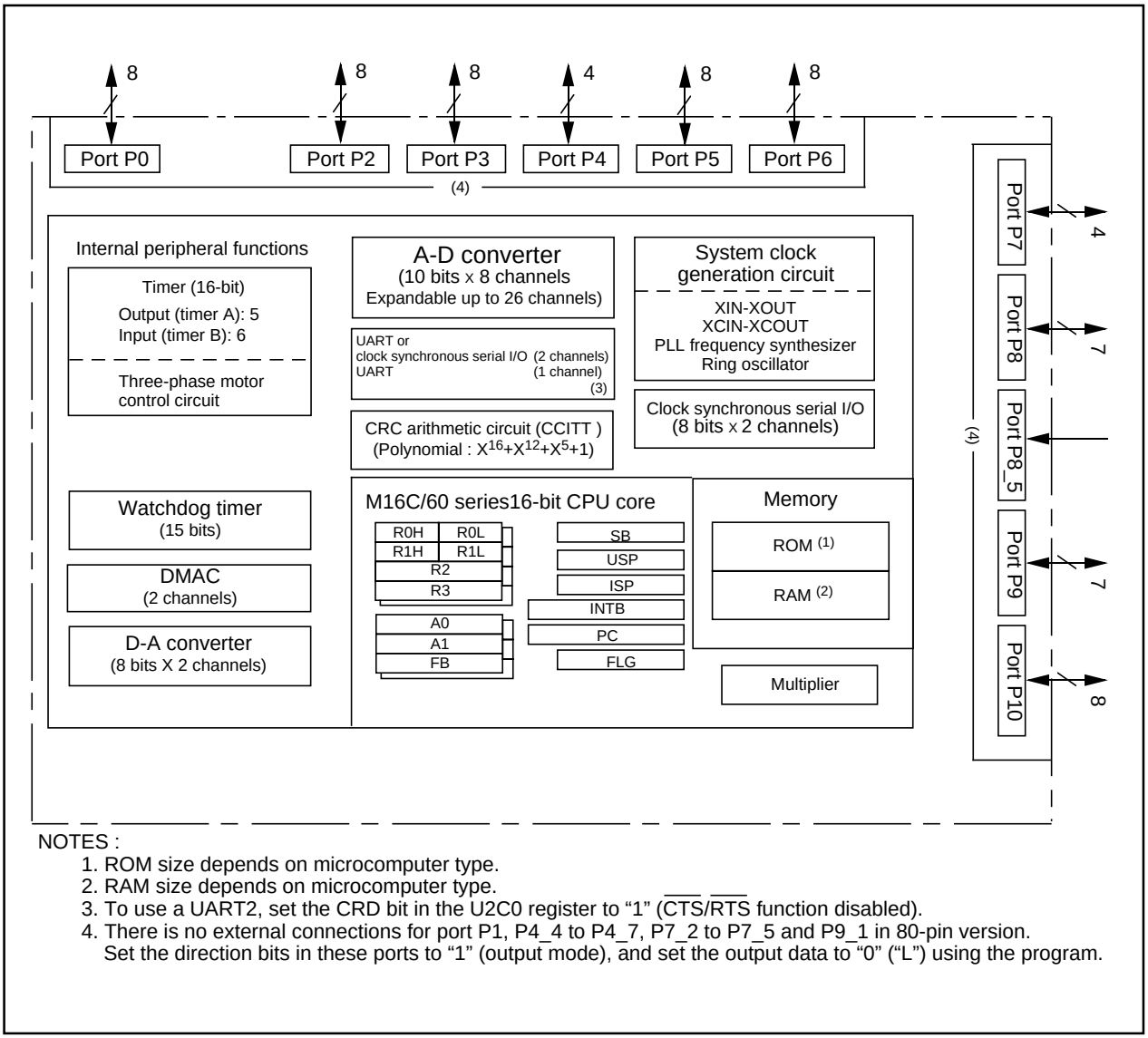
1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/62 group (M16C/62P, M16C/62PT) 128-pin and 100-pin version, figure 1.2 is a block diagram of the M16C/62 group (M16C/62P, M16C/62PT) 80-pin version.



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1= VCC2.

Figure 1.1 M16C/62 Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. To use a UART2, set the CRD bit in the U2C0 register to “1” ($\overline{CTS}/\overline{RTS}$ function disabled).
4. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version. Set the direction bits in these ports to “1” (output mode), and set the output data to “0” (“L”) using the program.

Figure 1.2 M16C/62 Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram

1.4 Product List

Tables 1.4 to 1.7 list the product list, figure 1.3 shows the type numbers, memory sizes and packages, table 1.8 lists the product code of flash memory version and external ROM version for M16C/62P. Figure 1.4 shows the marking diagram of flash memory version and external ROM version for M16C/62P. Please specify the mark of the mask ROM version at the time of ROM order.
Please ask separately marking of the flash memory version of M16C/62PT.

Table 1.4 Product List (1) (M16C/62P) As of Nov. 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30622M6P-XXXFP (D)	48K bytes	4K bytes	100P6S-A	MASK ROM version
M30622M6P-XXXGP (D)			100P6Q-A	
M30623M6P-XXXGP (D)			80P6S-A	
M30622M8P-XXXFP (D)	64K bytes	4K bytes	100P6S-A	
M30622M8P-XXXGP (D)			100P6Q-A	
M30623M8P-XXXGP (D)			80P6S-A	
M30622MAP-XXXFP	96K bytes	5K bytes	100P6S-A	
M30622MAP-XXXGP			100P6Q-A	
M30623MAP-XXXGP (D)			80P6S-A	
M30620MCP-XXXFP	128K bytes	10K bytes	100P6S-A	
M30620MCP-XXXGP			100P6Q-A	
M30621MCP-XXXGP (D)			80P6S-A	
M30622MEP-XXXFP (D)	192K bytes	12K bytes	100P6S-A	
M30622MEP-XXXGP (D)			100P6Q-A	
M30623MEP-XXXGP (D)			128P6Q-A	
M30622MGP-XXXFP (D)	256K bytes	12K bytes	100P6S-A	
M30622MGP-XXXGP (D)			100P6Q-A	
M30623MGP-XXXGP (D)			128P6Q-A	
M30624MGP-XXXFP		20K bytes	100P6S-A	
M30624MGP-XXXGP			100P6Q-A	
M30625MGP-XXXGP			128P6Q-A	
M30622MWP-XXXFP (D)	320K bytes	16K bytes	100P6S-A	
M30622MWP-XXXGP (D)			100P6Q-A	
M30623MWP-XXXGP (D)			128P6Q-A	
M30624MWP-XXXFP		24K bytes	100P6S-A	
M30624MWP-XXXGP			100P6Q-A	
M30625MWP-XXXGP			128P6Q-A	
M30626MWP-XXXFP		31K bytes	100P6S-A	
M30626MWP-XXXGP			100P6Q-A	
M30627MWP-XXXGP			128P6Q-A	
M30622MHP-XXXFP	384K bytes	16K bytes	100P6S-A	
M30622MHP-XXXGP			100P6Q-A	
M30623MHP-XXXGP			128P6Q-A	
M30624MHP-XXXFP		24K bytes	100P6S-A	
M30624MHP-XXXGP			100P6Q-A	
M30625MHP-XXXGP			128P6Q-A	
M30626MHP-XXXFP		31K bytes	100P6S-A	
M30626MHP-XXXGP			100P6Q-A	
M30627MHP-XXXGP			128P6Q-A	

(D): Under development
(P): Under planning

Table 1.5 Product List (2) (M16C/62P)

As of Nov. 2003

Type No.	ROM capacity	ROM capacity	Package type	Remarks
M30626MJP-XXXFP (P)	512K bytes	31K bytes	100P6S-A	MASK ROM version
M30626MJP-XXXGP (P)			100P6Q-A	
M30627MJP-XXXGP (P)			128P6Q-A	
M30622F8PFP	64K+4K bytes	4K bytes	100P6S-A	Flash memory version
M30622F8PGP			100P6Q-A	
M30623F8PGP (D)			80P6S-A	
M30620FCPFP	128K+4K bytes	10K bytes	100P6S-A	
M30620FCPGP			100P6Q-A	
M30621FCPGP (D)			80P6S-A	
M30624FGPFP	256K+4K bytes	20K bytes	100P6S-A	
M30624FGPGP			100P6Q-A	
M30625FGPGP			128P6Q-A	
M30626FHPFP	384K+4K bytes	31K bytes	100P6S-A	
M30626FHPGP			100P6Q-A	
M30627FHPGP			128P6Q-A	
M30626FJPFP (P)	512K+4K bytes	31K bytes	100P6S-A	
M30626FJPGP (P)			100P6Q-A	
M30627FJPGP (P)			128P6Q-A	
M30622SPFP (D)	———	4K bytes	100P6S-A	External ROM version
M30622SPGP (D)			100P6Q-A	
M30620SPFP (D)		10K bytes	100P6S-A	
M30620SPGP (D)			100P6Q-A	

(D): Under development
(P): Under planning

Table 1.6 Product List (3) (T version (M16C/62PT))

As of Nov. 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks	
M3062CM6T-XXXFP (D)	48K bytes	4K bytes	100P6S-A	MASK ROM version	T Version (High reliability 85 °C Version)
M3062CM6T-XXXGP (D)			100P6Q-A		
M3062EM6T-XXXGP (P)			80P6S-A		
M3062CM8T-XXXFP (D)	64K bytes	4K bytes	100P6S-A		
M3062CM8T-XXXGP (D)			100P6Q-A		
M3062EM8T-XXXGP (P)			80P6S-A		
M3062CMAT-XXXFP (D)	96K bytes	5K bytes	100P6S-A		
M3062CMAT-XXXGP (D)			100P6Q-A		
M3062EMAT-XXXGP (P)			80P6S-A		
M3062AMCT-XXXFP (D)	128K bytes	10K bytes	100P6S-A		
M3062AMCT-XXXGP (D)			100P6Q-A		
M3062BMCT-XXXGP (P)			80P6S-A		
M3062CF8TGP (D)	64K bytes	4K bytes	100P6Q-A	Flash memory version	
M3062AFCTFP (D)	128K+4K bytes	10K bytes	100P6S-A		
M3062AFCTGP (D)			100P6Q-A		
M3062BFCTGP (P)			80P6S-A		
M3062JFHTFP (D)	384K+4K bytes	31K bytes	100P6S-A		
M3062JFHTGP (D)			100P6Q-A		

(D): Under development
(P): Under planning

Table 1.7 Product List (4) (V version (M16C/62PT))

As of Nov. 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks	
M3062CM6V-XXXFP (P)	48K bytes	4K bytes	100P6S-A	MASK ROM version	V Version (High reliability 125 °C Version)
M3062CM6V-XXXGP (P)			100P6Q-A		
M3062EM6V-XXXGP (P)			80P6S-A		
M3062CM8V-XXXFP (P)	64K bytes	4K bytes	100P6S-A		
M3062CM8V-XXXGP (P)			100P6Q-A		
M3062EM8V-XXXGP (P)			80P6S-A		
M3062CMAV-XXXFP (P)	96K bytes	5K bytes	100P6S-A		
M3062CMAV-XXXGP (P)			100P6Q-A		
M3062EMAV-XXXGP (P)			80P6S-A		
M3062AMCV-XXXFP (D)	128K bytes	10K bytes	100P6S-A		
M3062AMCV-XXXGP (D)			100P6Q-A		
M3062BMCV-XXXGP (P)			80P6S-A		
M3062AFCVFP (D)	128K+4K bytes	10K bytes	100P6S-A	Flash memory version	
M3062AFCVGP (D)			100P6Q-A		
M3062BFCVGP (P)			80P6S-A		
M3062JFHVFP (P)	384K+4K bytes	31K bytes	100P6S-A		
M3062JFHVGP (P)			100P6Q-A		

(D): Under development
(P): Under planning

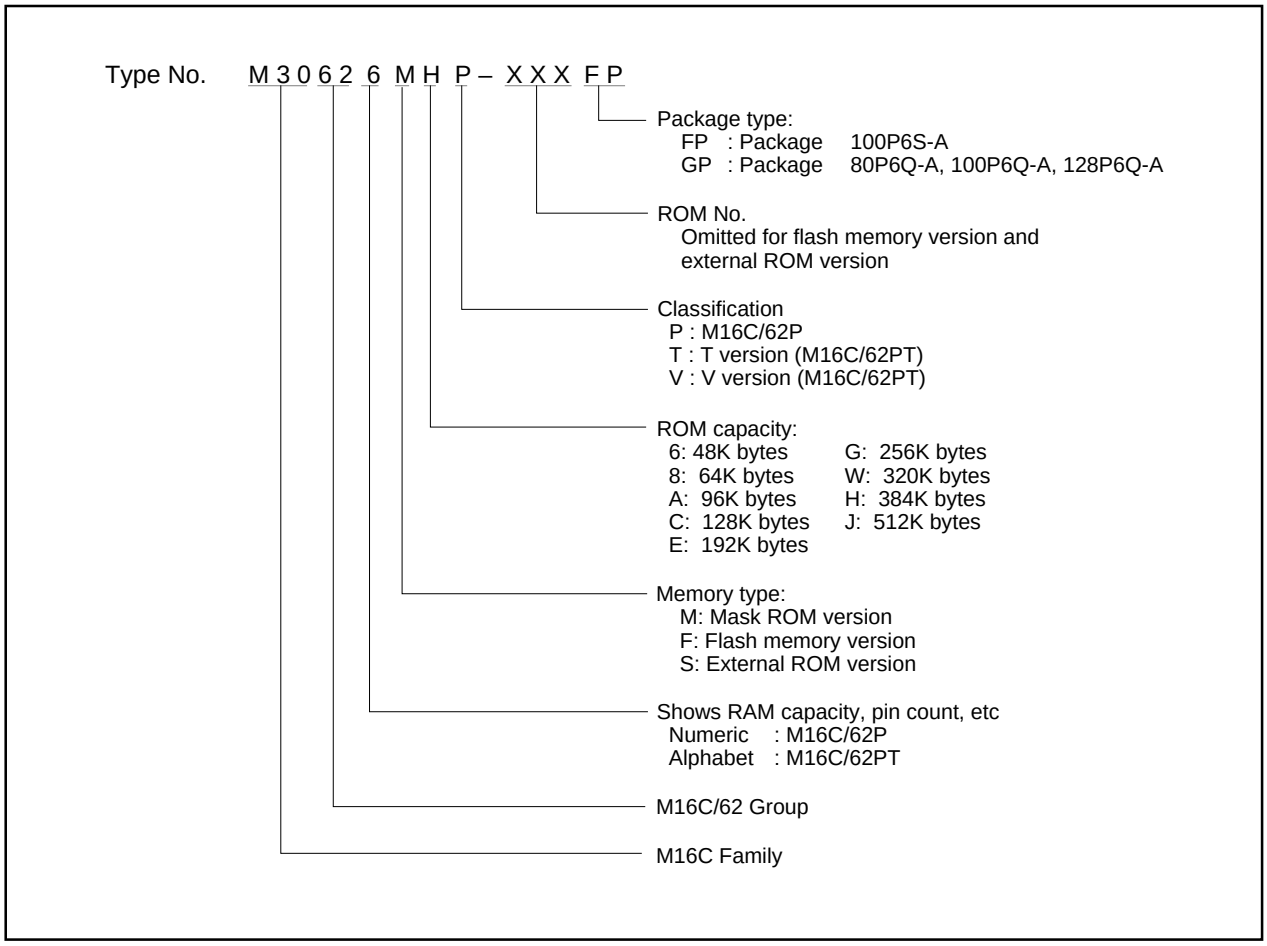


Figure 1.3 Type No., Memory Size, and Package

Table 1.8 Product Code of Flash Memory version and External ROM version for M16C/62P

	product code	Package	Internal ROM (user ROM area without block 1)		Internal ROM (block A, block 1)		Operating ambient temperature
			Program and erase endurance	Temperature range	Program and erase endurance	Temperature range	
Flash memory version	D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	D5						-20°C to 85°C
	D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	D9					-20°C to 85°C	-20°C to 85°C
	U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	U5						-20°C to 85°C
	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	U9					-20°C to 85°C	-20°C to 85°C
External ROM version	D3	Lead-included	—	—	—	—	-40°C to 85°C
	D5						-20°C to 85°C
	U3	Lead-free	—	—	—	—	-40°C to 85°C
	U5						-20°C to 85°C

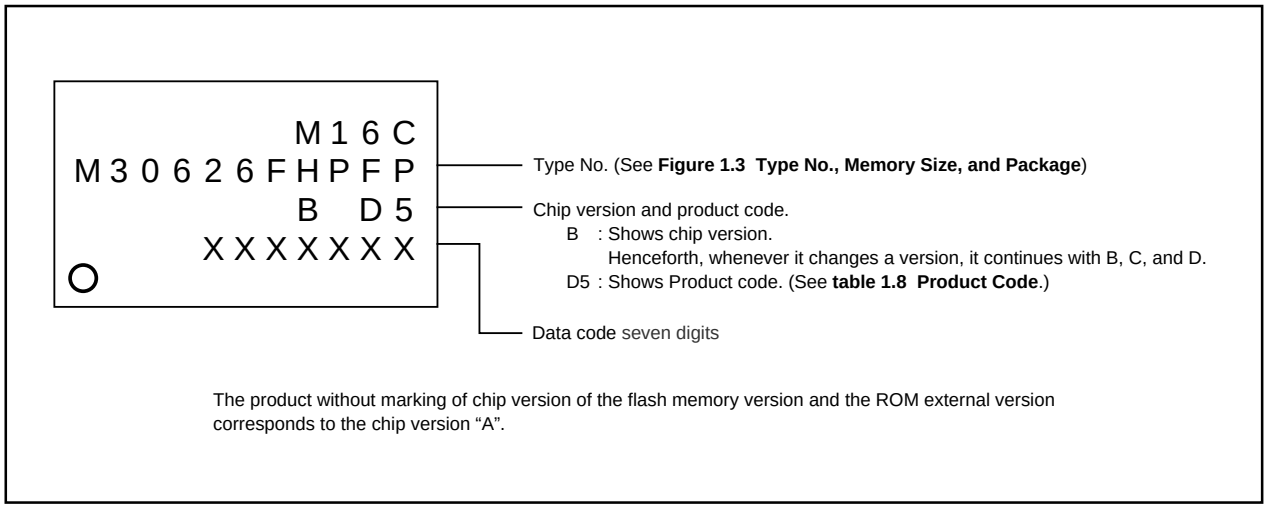


Figure 1.4 Marking Diagram of Flash Memory version and External ROM version for M16C/62P (Top View)

1.5 Pin Configuration

Figures 1.5 to 1.8 show the pin configurations (top view).

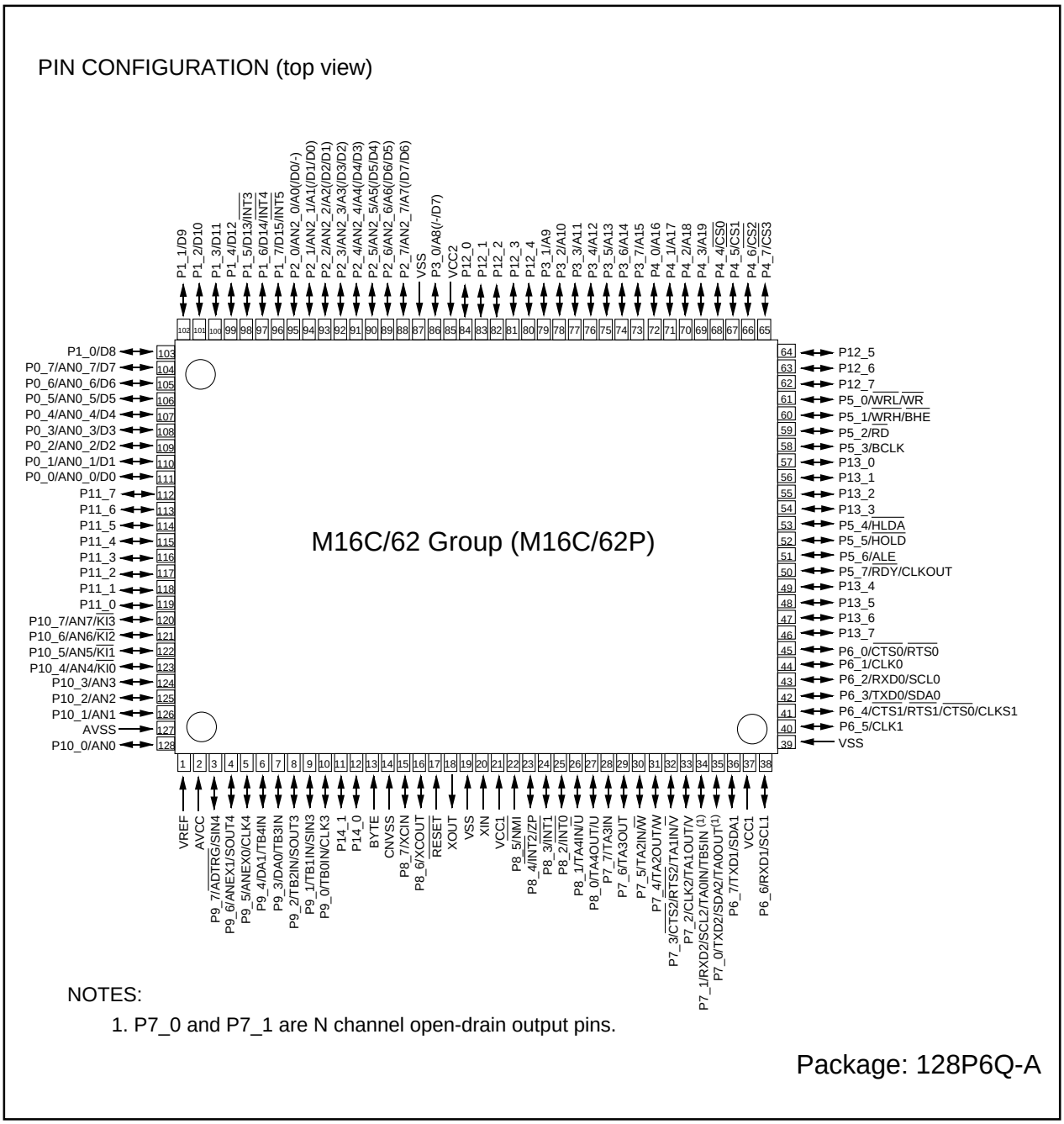
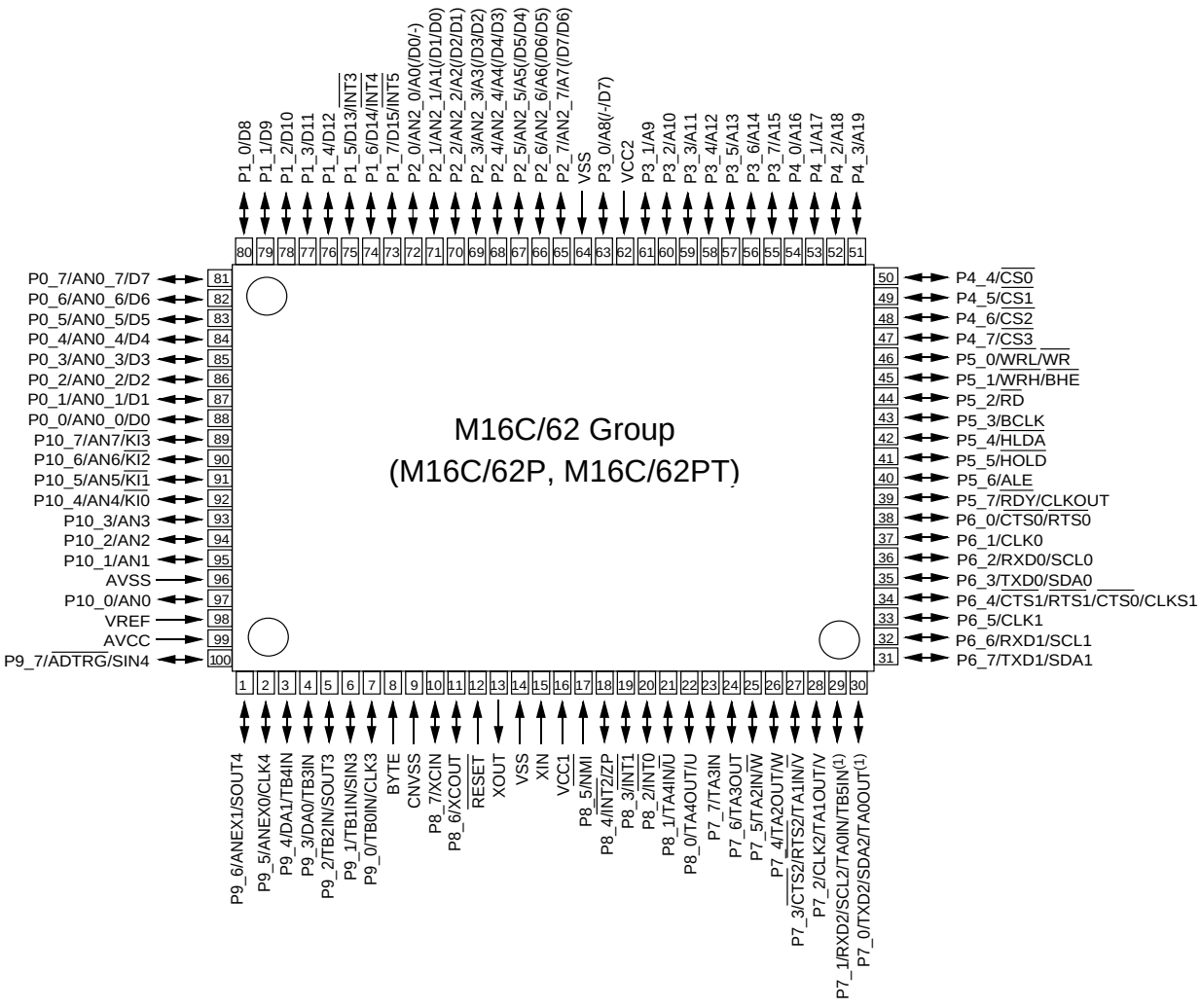


Figure 1.5 Pin Configuration (Top View)

PIN CONFIGURATION (top view)



NOTES:

1. P7_0 and P7_1 are N channel open-drain output pins.

Package: 100P6S-A

Figure 1.6 Pin Configuration (Top View)

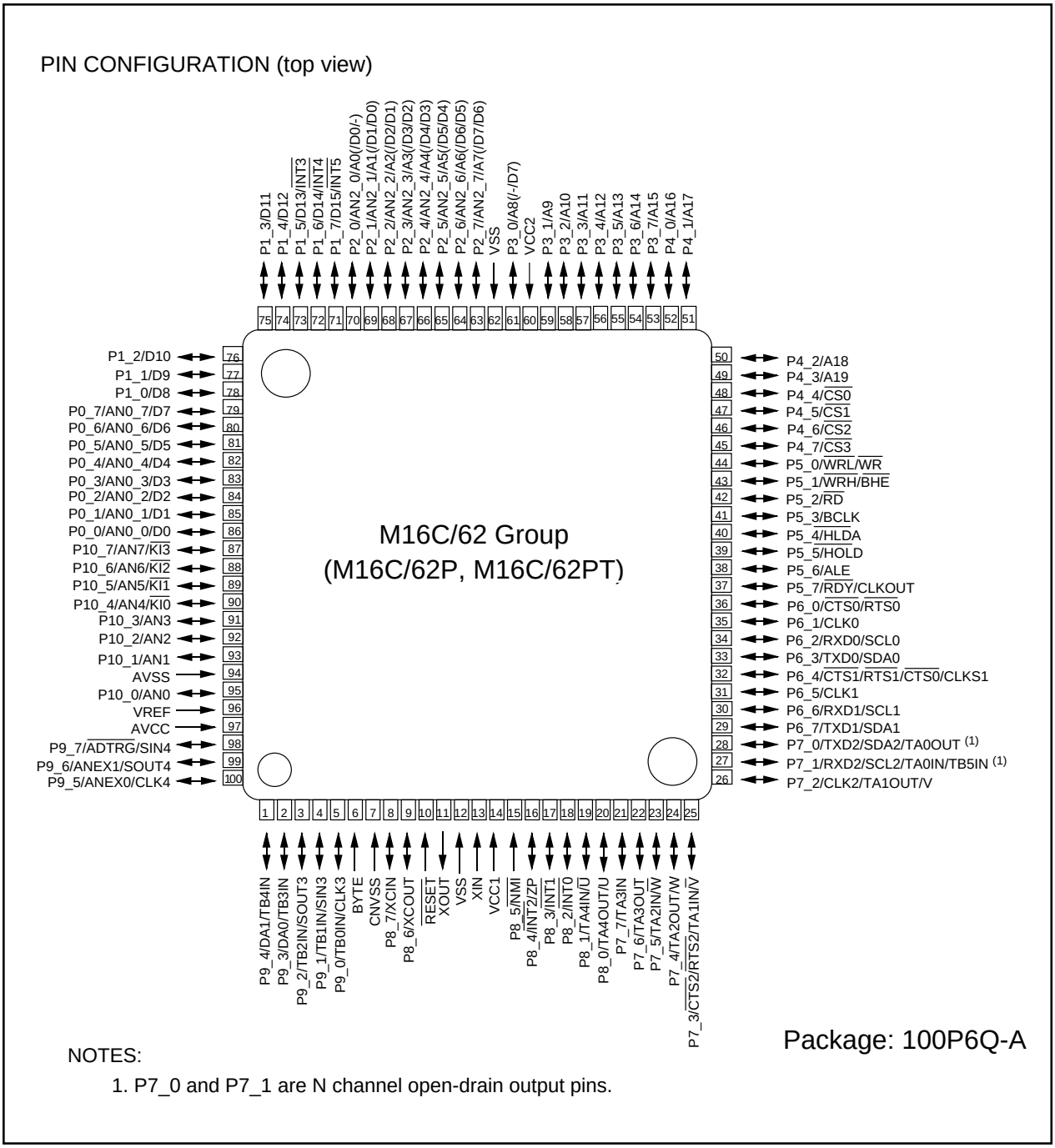
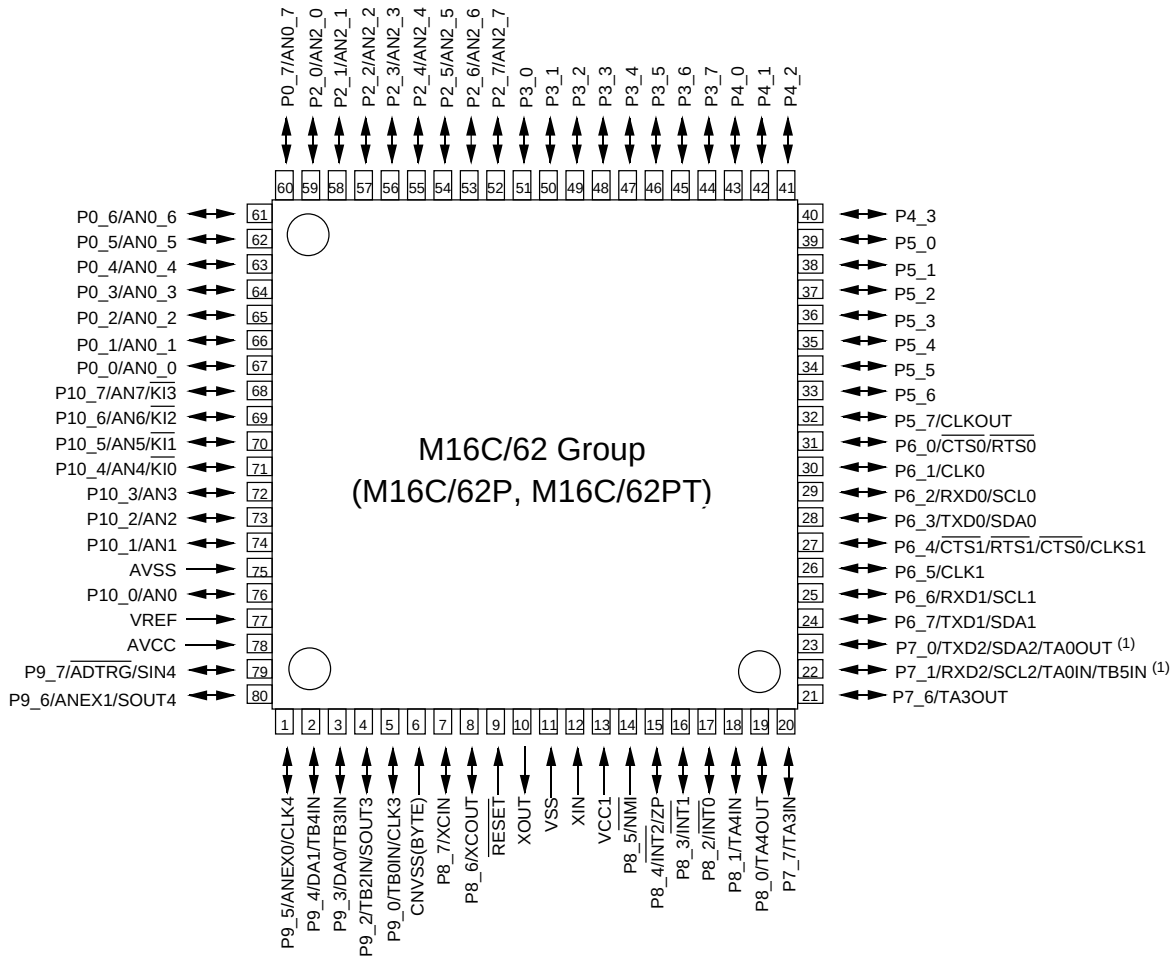


Figure 1.7 Pin Configuration (Top View)

PIN CONFIGURATION (top view)



Package: 80P6S-A

NOTES:

1. P7_0 and P7_1 are N channel open-drain output pins.

Figure 1.8 Pin Configuration (Top View)

1.6 Pin Description

Table 1.9 Pin Description (100-pin and 128-pin Version) (1)

Signal name	Pin name	I/O type	Power supply	Description
Power supply input	VCC1, VCC2 VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 ≥ VCC2.(2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A-D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode.
External data bus width select input	BYTE	I	VCC1	Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode.
Bus control pins(4)	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus.
	A0 to A19	O	VCC2	Output address bits (A0 to A19).
	A0/D0 to A7/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A0 to A7) by time-sharing when external 8-bit data bus are set as the multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A8 to A15) by time-sharing when external 16-bit data bus are set as the multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Output $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ or $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ can be switched by program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WRL}}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{\text{WRH}}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{\text{RD}}$ pin signal becomes "L" by reading data in an external memory space. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WR}}$ signal becomes "L" by writing data in an external memory space. The $\overline{\text{RD}}$ signal becomes "L" by reading data in an external memory space. The $\overline{\text{BHE}}$ signal becomes "L" by accessing an odd address. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for an external 8-bit data bus.
	ALE	O	VCC2	ALE is a signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is placed in a hold state.
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a "L" signal.
	$\overline{\text{RDY}}$	I	VCC2	While applying a "L" signal to the $\overline{\text{RDY}}$ pin, the microcomputer is placed in a wait state.

I : Input O : Output I/O : Input and output

Power supply : Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1.

NOTES:
1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 2.7 to 5.5 V to the VCC1 and VCC2 pins. Also the apply condition is that VCC1 ≥ VCC2.
3. When use VCC1 ≥ VCC2, contacts due to some points or restrictions to be checked.
4. This pin function is not in M16C/62PT.

Table 1.10 Pin Description (100-pin and 128-pin Version) (2)

Signal name	Pin name	I/O type	Power supply	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output (2)	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	These are timer A0 to timer A4 I/O pins. (except the output of TAOUT for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	These are timer A0 to timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	These are Three-phase motor control output pins.
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	VCC1	These are send control input pins.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	VCC1	These are receive control output pins.
	CLK0 to CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN3, SIN4	I	VCC1	These are serial data input pins.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (except TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (except SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (except SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 ≥ VCC2, contacts due to some points or restrictions to be checked.
2. This pin function is not in M16C/62PT.
3. Ask the oscillator maker the oscillation characteristic.

Table 1.11 Pin Description (100-pin and 128-pin Version) (3)

Signal name	Pin name	I/O type	Power supply	Description
Reference voltage input	VREF	I	VCC1	Applies the reference voltage for the A-D converter and D-A converter.
A-D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A-D converter
	$\overline{\text{ADTRG}}$	I	VCC1	This is an A-D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A-D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A-D converter.
D-A converter	DA0, DA1	O	VCC1	This is the Input pin for the D-A converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 (2), P13_0 to P13_7 (2)	I/O	VCC2	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 (2)	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. (except P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1 (2)	I/O	VCC1	I/O ports having equivalent functions to P0.
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 ≥ VCC2, contacts due to some points or restrictions to be checked.
2. Ports P11 to P14 are provided in the 128-pin version only.

Table 1.12 Pin Description (80-pin Version) (1)

Signal name	Pin name	I/O type	Power supply	Description
Power supply input	VCC1, VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. (2)
Analog power supply input	AVCC, AVSS	I	VCC1	Applies the power supply for the A-D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS (BYTE)	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer.
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	These are timer A0, timer A3 and Timer A4 I/O pins. (except the output of TAOUT for the N-channel open drain output.)
	TA0IN, TA3IN, TA4IN	I	VCC1	These are timer A0, timer A3 and Timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	These are timer B0, timer B2 to timer B5 input pins.
Serial I/O	$\overline{\text{CTS0}}$, $\overline{\text{CTS2}}$	I	VCC1	These are send control input pins.
	$\overline{\text{RTS0}}$, $\overline{\text{RTS2}}$	O	VCC1	These are receive control output pins.
	CLK0, CLK1, CLK3, CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN4	I	VCC1	These are serial data input pins.
	TXD0 to TXD4	O	VCC1	These are serial data output pins. (except TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (except SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (except SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:
1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.
3. Ask the oscillator maker the oscillation characteristic.

Table 1.13 Pin Description (80-pin Version) (2)

Signal name	Pin name	I/O type	Power supply	Description
Reference voltage input	VREF	I	VCC1	Applies the reference voltage for the A-D converter and D-A converter.
A-D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A-D converter
	$\overline{\text{ADTRG}}$	I	VCC1	This is an A-D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A-D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A-D converter.
D-A converter	DA0, DA1	O	VCC1	This is the Input pin for the D-A converter
I/O port	P0_0 to P0_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_7, P6_0 to P6_7, P10_0 to P10_7	I/O	VCC1	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7	I/O	VCC1	I/O ports having equivalent functions to P0.
	P4_0 to P4_3, P7_0, P7_1, P7_6, P7_7	I/O	VCC1	I/O ports having equivalent functions to P0. (except P7_0 and P7_1 for the N-channel open drain output.)
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

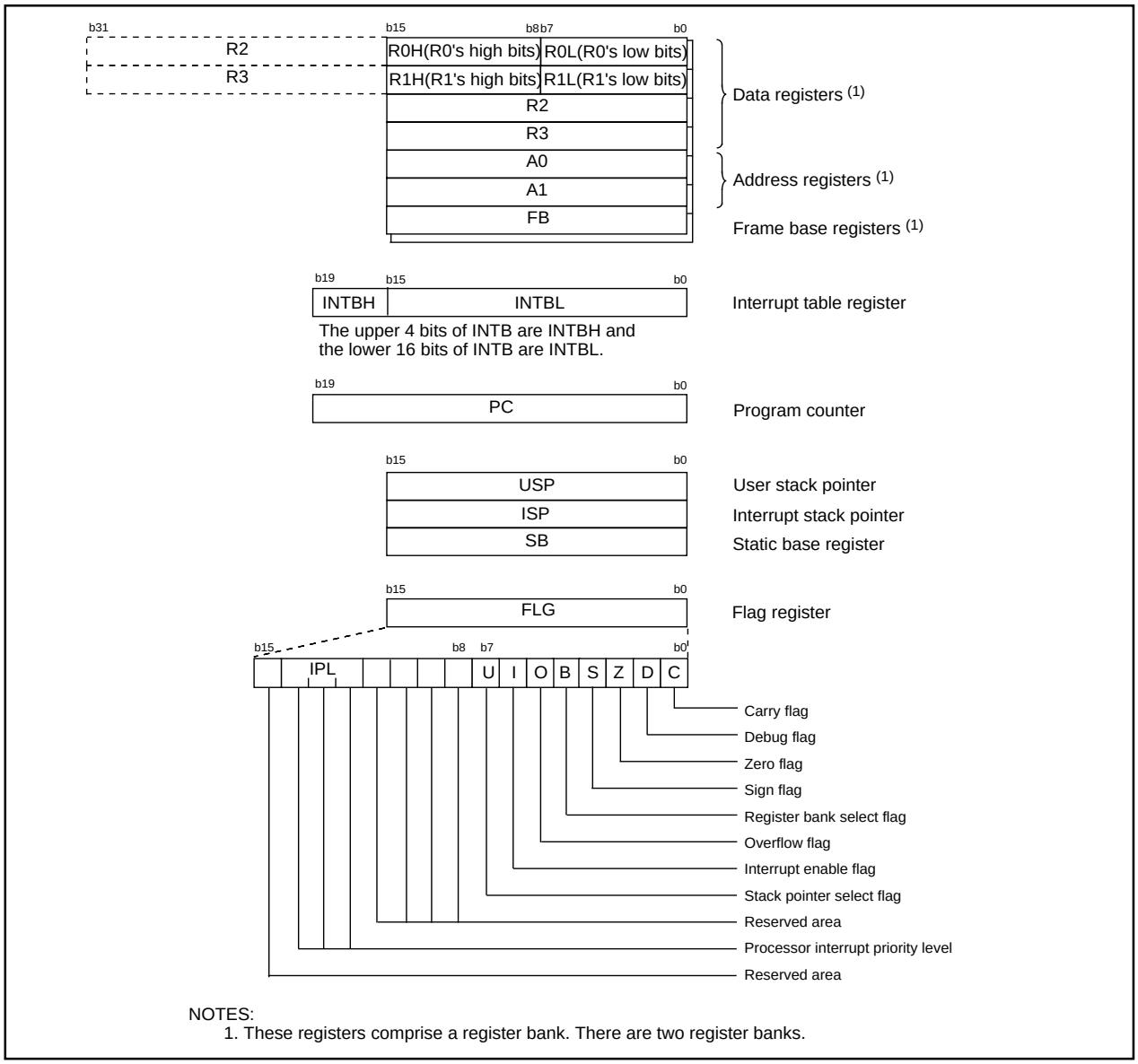
I : Input O : Output I/O : Input and output

NOTES:

1. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
   Set the direction bits in these ports to “1” (input mode), and set the output data to “0” (“L”) using the program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



NOTES:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/62P group. The address space extends the 1M bytes from address 00000h to FFFFFh.

The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

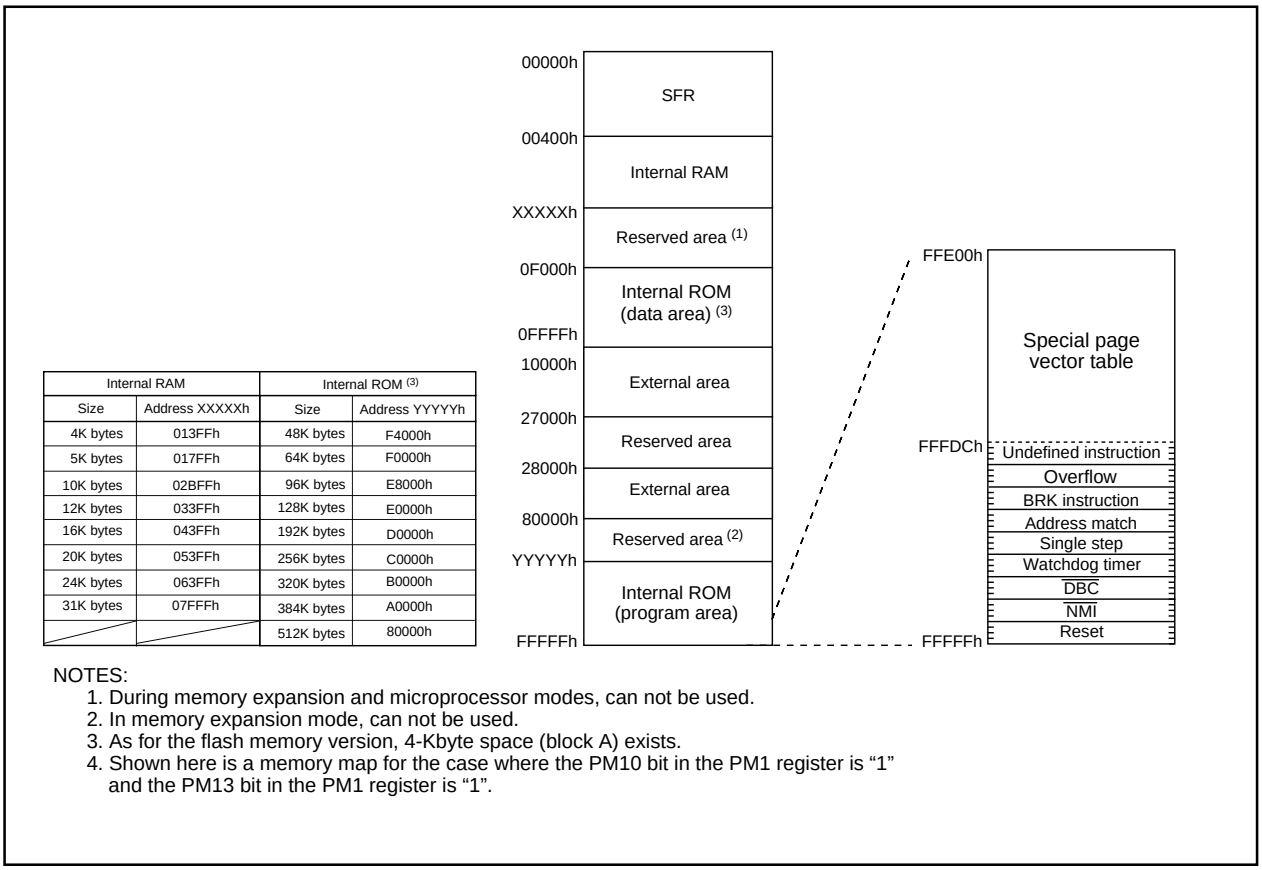
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 10-Kbyte internal RAM is allocated to the addresses from 00400h to 02BFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SRF is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users. Use M16C/62P (80-pin version) and M16C/62PT in single-chip mode. The memory expansion and microprocessor modes cannot be used.



Internal RAM		Internal ROM (3)	
Size	Address XXXXXh	Size	Address YYYYYh
4K bytes	013FFh	48K bytes	F4000h
5K bytes	017FFh	64K bytes	F0000h
10K bytes	02BFFh	96K bytes	E8000h
12K bytes	033FFh	128K bytes	E0000h
16K bytes	043FFh	192K bytes	D0000h
20K bytes	053FFh	256K bytes	C0000h
24K bytes	063FFh	320K bytes	B0000h
31K bytes	07FFFh	384K bytes	A0000h
		512K bytes	80000h

NOTES:
1. During memory expansion and microprocessor modes, can not be used.
2. In memory expansion mode, can not be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” and the PM13 bit in the PM1 register is “1”.

Figure 3.1 Memory Map

4. SFR

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor mode register 0 (2)	PM0	00000000b(CNVSS pin is "L") 00000011b(CNVSS pin is "H")
0005h	Processor mode register 1	PM1	00001000b
0006h	System clock control register 0	CM0	01001000b
0007h	System clock control register 1	CM1	00100000b
0008h	Chip select control register (6)	CSR	00000001b
0009h	Address match interrupt enable register	AIER	XXXXXX00b
000Ah	Protect register	PRCR	XX000000b
000Bh	Data bank register (6)	DBR	00h
000Ch	Oscillation stop detection register (3)	CM2	0000X000b
000Dh			
000Eh	Watchdog timer start register	WDTS	XXh
000Fh	Watchdog timer control register	WDC	00XXXXXXb (4)
0010h 0011h 0012h	Address match interrupt register 0	RMAD0	00h 00h X0h
0013h			
0014h 0015h 0016h	Address match interrupt register 1	RMAD1	00h 00h X0h
0017h			
0018h			
0019h	Voltage detection register 1 (5, 6)	VCR1	00001000b
001Ah	Voltage detection register 2 (5, 6)	VCR2	00h
001Bh	Chip select expansion control register (6)	CSE	00h
001Ch	PLL control register 0	PLC0	0001X010b
001Dh			
001Eh	Processor mode register 2	PM2	XXX00000b
001Fh	Voltage down detection interrupt register (6)	D4INT	00h
0020h 0021h 0022h	DMA0 source pointer	SAR0	XXh XXh XXh
0023h			
0024h 0025h 0026h	DMA0 destination pointer	DAR0	XXh XXh XXh
0027h			
0028h 0029h	DMA0 transfer counter	TCR0	XXh XXh
002Ah			
002Bh			
002Ch	DMA0 control register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h 0031h 0032h	DMA1 source pointer	SAR1	XXh XXh XXh
0033h			
0034h 0035h 0036h	DMA1 destination pointer	DAR1	XXh XXh XXh
0037h			
0038h 0039h	DMA1 transfer counter	TCR1	XXh XXh
003Ah			
003Bh			
003Ch	DMA1 control register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES :
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
3. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
4. The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program. It is set to "0" when the input voltage at the V_{CC1} pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (RAM retention limit detection circuit enabl
5. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
6. This register cannot be used by M16C/62PT.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h	INT3 interrupt control register	INT3IC	XX00X000b
0045h	Timer B5 interrupt control register	TB5IC	XXXXX000b
0046h	Timer B4 interrupt control register, UART1 BUS collision detection interrupt control register	TB4IC, U1BCNIC	XXXXX000b
0047h	Timer B3 interrupt control register, UART0 BUS collision detection interrupt control register	TB3IC, U0BCNIC	XXXXX000b
0048h	SI/O4 interrupt control register (S4IC), INT5 interrupt control register	S4IC, INT5IC	XX00X000b
0049h	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X000b
004Ah	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000b
004Bh	DMA0 interrupt control register	DM0IC	XXXXX000b
004Ch	DMA1 interrupt control register	DM1IC	XXXXX000b
004Dh	Key input interrupt control register	KUPIC	XXXXX000b
004Eh	A-D conversion interrupt control register	ADIC	XXXXX000b
004Fh	UART2 transmit interrupt control register	S2TIC	XXXXX000b
0050h	UART2 receive interrupt control register	S2RIC	XXXXX000b
0051h	UART0 transmit interrupt control register	S0TIC	XXXXX000b
0052h	UART0 receive interrupt control register	S0RIC	XXXXX000b
0053h	UART1 transmit interrupt control register	S1TIC	XXXXX000b
0054h	UART1 receive interrupt control register	S1RIC	XXXXX000b
0055h	Timer A0 interrupt control register	TA0IC	XXXXX000b
0056h	Timer A1 interrupt control register	TA1IC	XXXXX000b
0057h	Timer A2 interrupt control register	TA2IC	XXXXX000b
0058h	Timer A3 interrupt control register	TA3IC	XXXXX000b
0059h	Timer A4 interrupt control register	TA4IC	XXXXX000b
005Ah	Timer B0 interrupt control register	TB0IC	XXXXX000b
005Bh	Timer B1 interrupt control register	TB1IC	XXXXX000b
005Ch	Timer B2 interrupt control register	TB2IC	XXXXX000b
005Dh	INT0 interrupt control register	INT0IC	XX00X000b
005Eh	INT1 interrupt control register	INT1IC	XX00X000b
005Fh	INT2 interrupt control register	INT2IC	XX00X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

NOTES :
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h to 01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h	Flash identification register (2)	FIDR	XXXXXX00b
01B5h	Flash memory control register 1 (2)	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash memory control register 0 (2)	FMR0	XX000001b
01B8h 01B9h 01BAh	Address match interrupt register 2	RMAD2	00h 00h X0h
01BBh	Address match interrupt enable register 2	AIER2	XXXXXX00b
01BCh 01BDh 01BEh	Address match interrupt register 3	RMAD3	00h 00h X0h
01BFh			
00C0h to 02AFh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral clock select register	PCLKR	00000011b
025Fh			
0260h to 032Fh			
0330h			
0331h			
0332h			
0333h			
0334h			
0335h			
0336h			
0337h			
0338h			
0339h			
033Ah			
033Bh			
033Ch			
033Dh			
033Eh			
033Fh			

NOTES :
1. The blank areas are reserved and cannot be accessed by users.
2. This register is included in the flash memory version.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0340h	Timer B3, 4, 5 count start flag	TBSR	000XXXXXb
0341h			
0342h 0343h	Timer A1-1 register	TA11	XXh XXh
0344h 0345h	Timer A2-1 register	TA21	XXh XXh
0346h 0347h	Timer A4-1 register	TA41	XXh XXh
0348h	Three-phase PWM control register 0	INVC0	00h
0349h	Three-phase PWM control register 1	INVC1	00h
034Ah	Three-phase output buffer register 0	IDB0	00h
034Bh	Three-phase output buffer register 1	IDB1	00h
034Ch	Dead time timer	DTT	XXh
034Dh	Timer B2 interrupt occurrence frequency set counter	ICTB2	XXh
034Eh			
034Fh			
0350h 0351h	Timer B3 register	TB3	XXh XXh
0352h 0353h	Timer B4 register	TB4	XXh XXh
0354h 0355h	Timer B5 register	TB5	XXh XXh
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 mode register	TB3MR	00XX0000b
035Ch	Timer B4 mode register	TB4MR	00XX0000b
035Dh	Timer B5 mode register	TB5MR	00XX0000b
035Eh	Interrupt cause select register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt cause select register	IFSR	00h
0360h	SI/O3 transmit/receive register	S3TRR	XXh
0361h			
0362h	SI/O3 control register	S3C	01000000b
0363h	SI/O3 bit rate generator	S3BRG	XXh
0364h	SI/O4 transmit/receive register	S4TRR	XXh
0365h			
0366h	SI/O4 control register	S4C	01000000b
0367h	SI/O4 bit rate generator	S4BRG	XXh
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 special mode register 4	U0SMR4	00h
036Dh	UART0 special mode register 3	U0SMR3	000X0X0Xb
036Eh	UART0 special mode register 2	U0SMR2	X0000000b
036Fh	UART0 special mode register	U0SMR	X0000000b
0370h	UART1 special mode register 4	U1SMR4	00h
0371h	UART1 special mode register 3	U1SMR3	000X0X0Xb
0372h	UART1 special mode register 2	U1SMR2	X0000000b
0373h	UART1 special mode register	U1SMR	X0000000b
0374h	UART2 special mode register 4	U2SMR4	00h
0375h	UART2 special mode register 3	U2SMR3	000X0X0Xb
0376h	UART2 special mode register 2	U2SMR2	X0000000b
0377h	UART2 special mode register	U2SMR	X0000000b
0378h	UART2 transmit/receive mode register	U2MR	00h
0379h	UART2 bit rate generator	U2BRG	XXh
037Ah 037Bh	UART2 transmit buffer register	U2TB	XXh XXh
037Ch	UART2 transmit/receive control register 0	U2C0	00001000b
037Dh	UART2 transmit/receive control register 1	U2C1	00000010b
037Eh 037Fh	UART2 receive buffer register	U2RB	XXh XXh

NOTES :
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0380h	Count start flag	TABSR	00h
0381h	Clock prescaler reset flag	CPSRF	0XXXXXXXb
0382h	One-shot start flag	ONSF	00h
0383h	Trigger select register	TRGSR	00h
0384h	Up-down flag	UDF	00h (2)
0385h			
0386h	Timer A0 register	TA0	XXh
0387h			XXh
0388h	Timer A1 register	TA1	XXh
0389h			XXh
038Ah	Timer A2 register	TA2	XXh
038Bh			XXh
038Ch	Timer A3 register	TA3	XXh
038Dh			XXh
038Eh	Timer A4 register	TA4	XXh
038Fh			XXh
0390h	Timer B0 register	TB0	XXh
0391h			XXh
0392h	Timer B1 register	TB1	XXh
0393h			XXh
0394h	Timer B2 register	TB2	XXh
0395h			XXh
0396h	Timer A0 mode register	TA0MR	00h
0397h	Timer A1 mode register	TA1MR	00h
0398h	Timer A2 mode register	TA2MR	00h
0399h	Timer A3 mode register	TA3MR	00h
039Ah	Timer A4 mode register	TA4MR	00h
039Bh	Timer B0 mode register	TB0MR	00XX0000b
039Ch	Timer B1 mode register	TB1MR	00XX0000b
039Dh	Timer B2 mode register	TB2MR	00XX0000b
039Eh	Timer B2 special mode register	TB2SC	XXXXXX00b
039Fh			
03A0h	UART0 transmit/receive mode register	U0MR	00h
03A1h	UART0 bit rate generator	U0BRG	XXh
03A2h	UART0 transmit buffer register	U0TB	XXh
03A3h			XXh
03A4h	UART0 transmit/receive control register 0	U0C0	00001000b
03A5h	UART0 transmit/receive control register 1	U0C1	00000010b
03A6h	UART0 receive buffer register	U0RB	XXh
03A7h			XXh
03A8h	UART1 transmit/receive mode register	U1MR	00h
03A9h	UART1 bit rate generator	U1BRG	XXh
03AAh	UART1 transmit buffer register	U1TB	XXh
03ABh			XXh
03ACh	UART1 transmit/receive control register 0	U1C0	00001000b
03ADh	UART1 transmit/receive control register 1	U1C1	00000010b
03AEh	UART1 receive buffer register	U1RB	XXh
03AFh			XXh
03B0h	UART transmit/receive control register 2	UCON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 request cause select register	DM0SL	00h
03B9h			
03BAh	DMA1 request cause select register	DM1SL	00h
03BBh			
03BCh	CRC data register	CRCD	XXh
03BDh			XXh
03BEh	CRC input register	CRCIN	XXh
03BFh			

NOTES :

1.The blank areas are reserved and cannot be accessed by users.

2. Bits 7 to 5 in the Up-down flag are "0" by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
03C0h 03C1h	A-D register 0	AD0	XXh XXh
03C2h 03C3h	A-D register 1	AD1	XXh XXh
03C4h 03C5h	A-D register 2	AD2	XXh XXh
03C6h 03C7h	A-D register 3	AD3	XXh XXh
03C8h 03C9h	A-D register 4	AD4	XXh XXh
03CAh 03CBh	A-D register 5	AD5	XXh XXh
03CCh 03CDh	A-D register 6	AD6	XXh XXh
03CEh 03CFh	A-D register 7	AD7	XXh XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A-D control register 2	ADCON2	00h
03D5h			
03D6h	A-D control register 0	ADCON0	00000XXXb
03D7h	A-D control register 1	ADCON1	00h
03D8h	D-A register 0	DA0	00h
03D9h			
03DAh	D-A register 1	DA1	00h
03DBh			
03DCh	D-A control register	DACON	00h
03DDh			
03DEh	Port P14 control register	PC14	XX00XXXXb
03DFh	Pull-up control register 3	PUR3	00h
03E0h	Port P0 register	P0	XXh
03E1h	Port P1 register	P1	XXh
03E2h	Port P0 direction register	PD0	00h
03E3h	Port P1 direction register	PD1	00h
03E4h	Port P2 register	P2	XXh
03E5h	Port P3 register	P3	XXh
03E6h	Port P2 direction register	PD2	00h
03E7h	Port P3 direction register	PD3	00h
03E8h	Port P4 register	P4	XXh
03E9h	Port P5 register	P5	XXh
03EAh	Port P4 direction register	PD4	00h
03EBh	Port P5 direction register	PD5	00h
03ECh	Port P6 register	P6	XXh
03EDh	Port P7 register	P7	XXh
03EEh	Port P6 direction register	PD6	00h
03EFh	Port P7 direction register	PD7	00h
03F0h	Port P8 register	P8	XXh
03F1h	Port P9 register	P9	XXh
03F2h	Port P8 direction register	PD8	00X00000b
03F3h	Port P9 direction register	PD9	00h
03F4h	Port P10 register	P10	XXh
03F5h	Port P11 register	P11	XXh
03F6h	Port P10 direction register	PD10	00h
03F7h	Port P11 direction register	PD11	00h
03F8h	Port P12 register	P12	XXh
03F9h	Port P13 register	P13	XXh
03FAh	Port P12 direction register	PD12	00h
03FBh	Port P13 direction register	PD13	00h
03FCh	Pull-up control register 0	PUR0	00h
03FDh	Pull-up control register 1	PUR1	00000000b 00000010b (2)
03FEh	Pull-up control register 2	PUR2	00h
03FFh	Port control register	PCR	00h

NOTES :

1. The blank areas are reserved and cannot be accessed by users.
2. At hardware reset 1 or hardware reset 2, the register is as follows:
   - "00000000b" where "L" is inputted to the CNVSS pin
   - "00000010b" where "H" is inputted to the CNVSS pin

   At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
   - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode)
   - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode)

X : Nothing is mapped to this bit

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

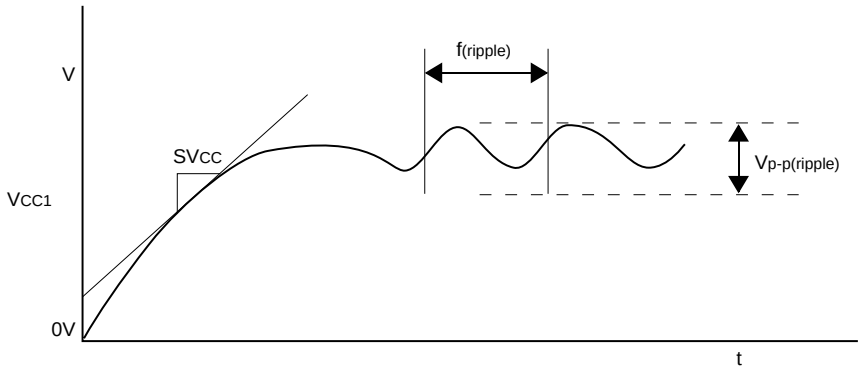
Symbol	Parameter		Condition	Rated value	Unit
V_{CC1}, V_{CC2}	Supply voltage		V_{CC1}=AVcc	-0.3 to 6.5	V
V_{CC2}	Supply voltage		V_{CC2}	-0.3 to V_{CC1}+0.1	V
AVcc	Analog supply voltage		V_{CC1}=AVcc	-0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		-0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		-0.3 to 6.5	V
V_O	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		-0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		-0.3 to 6.5	V
P_d	Power dissipation		-40 °C < T_{opr} ≤ 85 °C	300	mW
T_{opr}	Operating ambient temperature	When the microcomputer is operating		-20 to 85 / -40 to 85	°C
		Flash program erase		0 to 60	
T_{stg}	Storage temperature			-65 to 150	°C

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.2 Recommended Operating Conditions (1) (1)

Symbol	Parameter		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{CC1}, V_{CC2}	Supply voltage($V_{CC1} \geq V_{CC2}$)		2.7	5.0	5.5	V
AVcc	Analog supply voltage			V_{CC1}		V
$f_{(ripple)}$(2)	Power supply ripple allowable frequency				10	MHz
$V_{P-P(ripple)}$(2)	Power supply ripple allowable amplitude voltage	(V_{CC1}=5V)			0.5	V
		(V_{CC1}=3V)			0.3	V
$V_{CC(\lvert\Delta V / \Delta T\rvert)}$(2)	Power supply ripple rising / falling gradient	(V_{CC1}=5V)			0.3	V/ms
		(V_{CC1}=3V)			0.3	V/ms
SV_{CC}(2)	Power supply rising gradient		0.05			V/ms
Vss	Supply voltage			0		V
AVss	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor modes)	0.5V_{CC2}		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8V_{CC1}		V_{CC1}	V
		P7_0 , P7_1	0.8V_{CC1}		6.5	V
V_{IL}	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor modes)	0		0.16V_{CC2}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2V_{CC1}	V
$I_{OH (peak)}$	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
$I_{OH (avg)}$	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-5.0	mA
$I_{OL (peak)}$	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL (avg)}$	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. SV_{CC} indicates the minimum time gradient until V_{CC1} reaches 2.7V.

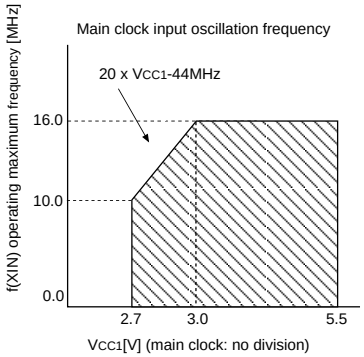


3. The mean output current is the mean value within 100ms.
4. The total $I_{OL (peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0 and P14_1 must be 80mA max. The total $I_{OL (peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH (peak)}$ for ports P0, P1, and P2 must be -40mA max. The total $I_{OH (peak)}$ for ports P3, P4, P5, P12, and P13 must be -40mA max. The total $I_{OH (peak)}$ for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total $I_{OH (peak)}$ for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.
5. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.3 Recommended Operating Conditions (2) (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f (XIN)	Main clock input oscillation frequency (2)	V_{CC1}=3.0 to 5.5V	0		16	MHz
		V_{CC1}=2.7 to 3.0V	0		20 X V_{CC1}-44	MHz
f (XCIN)	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	Ring oscillation frequency		0.5	1	2	MHz
f (PLL)	PLL clock oscillation frequency (2)	V_{CC1}=3.0 to 5.5V	10		24	MHz
		V_{CC1}=2.7 to 3.0V	10		46.67 X V_{CC1}-116	MHz
f (BCLK)	CPU operation clock		0		24	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	V_{CC1}=5.0V			20	ms
		V_{CC1}=3.0V			50	ms

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. Relationship between main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.



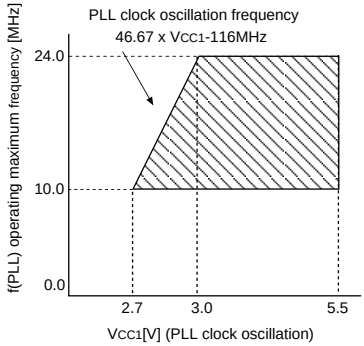


Table 5.4 A-D Conversion Characteristics (1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{REF} =V_{CC1}				10	Bits
INL	Integral non-linearity error	10 bit	V_{REF}= V_{CC1}= 5V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			V_{REF}= V_{CC1}= 3.3V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8 bit	V_{REF} =V_{CC1}=3.3V				±2	LSB
–	Absolute accuracy	10 bit	V_{REF}= V_{CC1}= 5V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			V_{REF}= V_{CC1}= 3.3V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8 bit	V_{REF} =V_{CC1}=3.3V				±2	LSB
–	Tolerance level impedance					3		kΩ
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R_{LADDER}	Ladder resistance		V_{REF} =V_{CC1}		10		40	kΩ
t_{CONV}	Conversion time(10bit), Sample & hold function available		V_{REF} =V_{CC1}=5V, øAD=12MHz		2.75			µs
t_{CONV}	Conversion time(8bit), Sample & hold function available		V_{REF} =V_{CC1}=5V, øAD=12MHz		2.33			µs
t_{SAMP}	Sampling time				0.25			µs
V_{REF}	Reference voltage				2.0		V_{CC1}	V
V_{IA}	Analog input voltage				0		V_{REF}	V

NOTES:
1. Referenced to V_{CC1}=AV$_{CC}$=V_{REF}=3.3 to 5.5V, V_{SS}=AV$_{SS}$=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. If V_{CC1} > V_{CC2}, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. AD operation clock frequency (øAD frequency) must be 12 MHz or less. And divide the fAD if V_{CC1} is less than 4.0V, and øAD frequency into 10 MHz or less.
4. A case without sample & hold function turn øAD frequency into 250 kHz or more in addition to a limit of Note 3.
   A case with sample & hold function turn øAD frequency into 1MHz or more in addition to a limit of Note 3.

Table 5.5 D-A Conversion Characteristics (1)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference power supply input current	(Note 2)			1.5	mA

NOTES:
1. Referenced to V_{CC1}=V_{REF}=3.3 to 5.5V, V_{SS}=AV$_{SS}$=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. This applies when using one D-A converter, with the D-A register for the unused D-A converter set to “00h”. The A-D converter’s ladder resistance is not included. Also, when D-A register contents are not “00h”, the current I_{VREF} always flows even though Vref may have been set to be unconnected by the A-D control register.

Table 5.6 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (D3, D5, U3, U5)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase endurance (3)		100			cycle
-	Word program time (V_{CC1}=5.0V, T_{opr}=25°C)			25	200	µs
-	Lock bit program time			25	200	µs
-	Block erase time (V_{CC1}=5.0V, T_{opr}=25 °C)	4K bytes block		0.3	4	s
		8K bytes block		0.3	4	s
		32K bytes block		0.5	4	s
		64K bytes block		0.8	4	s
-	Erase all unlocked blocks time (2)				4 X n	s
t_{PS}	Flash memory circuit stabilization wait time				15	µs
-	Data hold time (5)		10			year

Table 5.7 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (D7, D9, U7, U7) (Block A and Block 1 (7))

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase endurance (3, 8, 9)		10,000 (4)			cycle
-	Word program time (V_{CC1}=5.0V, T_{opr}=25°C)			25		µs
-	Lock bit program time			25		µs
-	Block erase time (V_{CC1}=5.0V, T_{opr}=25 °C)	4K bytes block		0.3		s
t_{PS}	Flash memory circuit stabilization wait time				15	µs
-	Data hold time (5)		10			year

NOTES :
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = 0 to 60 °C unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4K bytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. T_{opr} = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
6. Referenced to V_{CC1} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C (D9, U9) / -40 to 85 °C (D7, U7) unless otherwise specified.
7. Table 5.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.6.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary. Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.8 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60°C)

Flash program, erase voltage	Flash read operation voltage
V_{CC1} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V	V_{CC1}=2.7 to 5.5 V

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics (1)

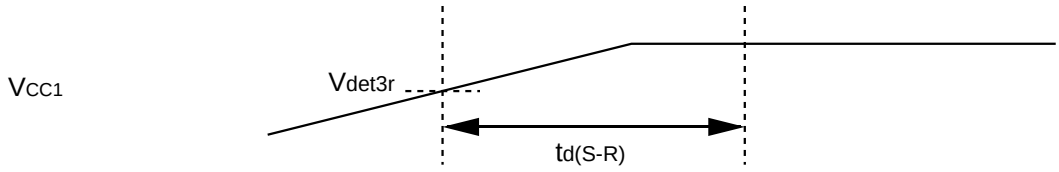
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det4}	Voltage down detection voltage (1)	V_{CC1}=0.8 to 5.5V	3.3	3.8	4.4	V
V_{det3}	Reset level detection voltage (1, 2)		2.2	2.8	3.6	V
V_{det3s}	Low voltage reset retention voltage		0.8			V
V_{det3r}	Low voltage reset release voltage (3)		2.2	2.9	4.0	V
V_{det2}	RAM retention limit detection voltage (1)		1.4	2.0	2.7	V

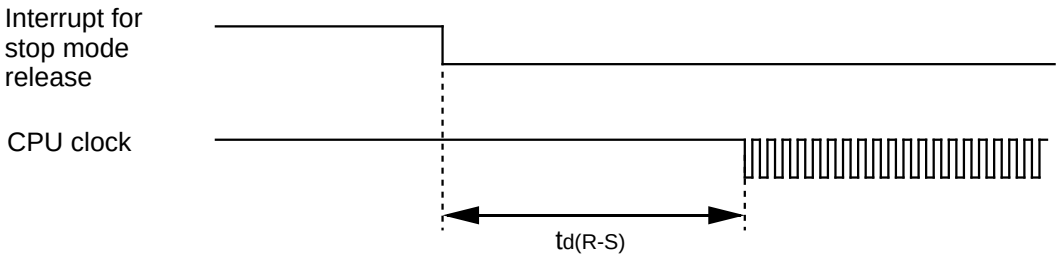
NOTES:
1. $V_{det4} > V_{det3} > V_{det2}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the operation at f(BCLK) ≤ 10MHz is guaranteed.
3. $V_{det3r} > V_{det3}$ is not guaranteed.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	V_{CC1}=2.7 to 5.5V			2	ms
$t_{d(R-S)}$	STOP release time				150	µs
$t_{d(W-S)}$	Low power dissipation mode wait mode release time				150	µs
$t_{d(M-L)}$	Time for internal power supply stabilization when main clock oscillation starts				50	µs
$t_{d(S-R)}$	Hardware reset 2 release wait time	V_{CC1}=V_{det3r} to 5.5V		6 (1)	20	ms
$t_{d(E-A)}$	Low voltage detection circuit operation start time	V_{CC1}=2.7 to 5.5V			20	µs

NOTES:
1. When V_{CC1} = 5V.





$V_{CC1} = V_{CC2} = 5V$

Table 5.11 Electrical Characteristics (1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=-5mA	V_{CC1}-2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=-5mA (2)	V_{CC2}-2.0		V_{CC2}	
V_{OH}	HIGH output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=-200µA	V_{CC1}-0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=-200µA (2)	V_{CC2}-0.3		V_{CC2}	
V_{OH}	HIGH output voltage XOUT	HIGHPOWER	I_{OH}=-1mA	V_{CC1}-2.0		V_{CC1}	V
		LOWPOWER	I_{OH}=-0.5mA	V_{CC1}-2.0		V_{CC1}	
	HIGH output voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=5mA (2)			2.0	
V_{OL}	LOW output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=200µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=200µA (2)			0.45	
V_{OL}	LOW output voltage XOUT	HIGHPOWER	I_{OL}=1mA			2.0	V
		LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW output voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL0 to SCL2, SDA0 TO SDA2, CLK0 to CLK4,TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SIN3, SIN4		0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	XIN		0.2		0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=5V			5.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback resistance	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistance	XCIN			15		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at V_{CC1} = 5 V and V_{CC2} = 3 V, refer to the 3 V version value for the pin specified value on the V_{CC2} port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1} = V_{CC2} = 5V$

Table 5.12 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC1}=4.0 to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=24MHz, No division, PLL operation		14	20	mA
				No division, Ring oscillation		1		mA
			Flash memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, Ring oscillation		1.8		mA
			Flash memory Program	f(BCLK)=10MHz, V_{CC1}=5.0V		15		mA
			Flash memory Erase	f(BCLK)=10MHz, V_{CC1}=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz, Low power dissipation mode, ROM (3)		25		µA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM (3)		25		µA
				f(BCLK)=32kHz Low power dissipation mode, Flash memory (3)		420		µA
				Ring oscillation, Wait mode		50		µA
			Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (2), Oscillation capacity High		7.5		µA
				f(BCLK)=32kHz, Wait mode (2), Oscillation capacity Low		2.0		µA
				Stop mode, T_{opr}=25°C		0.8	3.0	µA
I_{det4}	Voltage down detection dissipation current (4)					0.7	4	µA
I_{det3}	Reset area detection dissipation current (4)					1.2	8	µA
I_{det2}	RAM retention limit detection dissipation current (4)					1.1	6	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}= 4.2 to 5.5V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
   I_{det4}: VC27 bit of VCR2 register
   I_{det3}: VC26 bit of VCR2 register
   I_{det2}: VC25 bit of VCR2 register

$V_{CC1} = V_{CC2} = 5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.13 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	62.5		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 5.14 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	40		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 \quad [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 \quad [ns]$$

n is “2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

$V_{CC1} = V_{CC2} = 5V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.15 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	40		ns

Table 5.16 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	200		ns

Table 5.17 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 5.18 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 5.19 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

Table 5.20 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

$V_{CC1} = V_{CC2} = 5V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.21 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 5.22 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.23 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.24 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW pulse width	125		ns

Table 5.25 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	30		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.26 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input LOW pulse width	250		ns

$V_{CC1} = V_{CC2} = 5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.27 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See **Figure 5.1**		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(3)		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

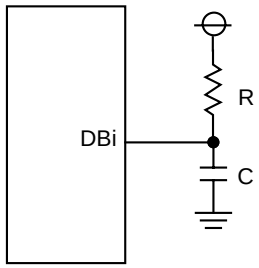
$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



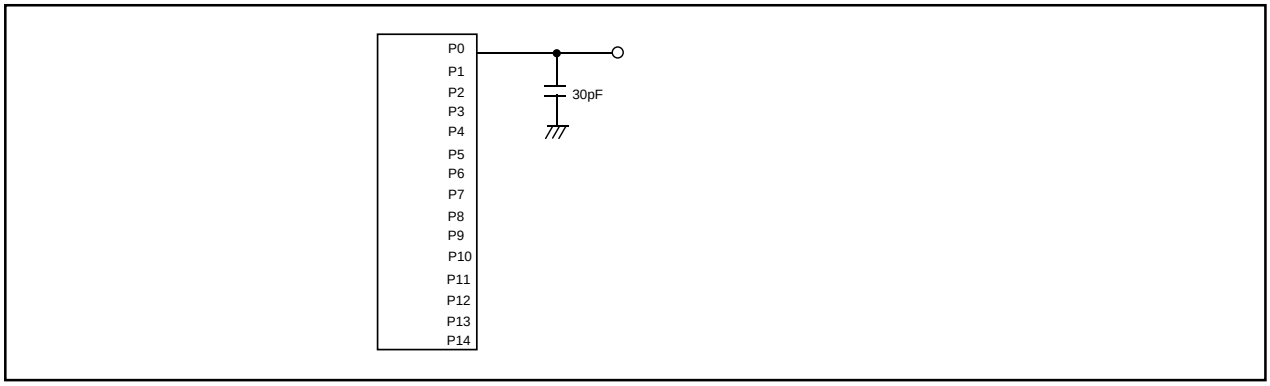


Figure 5.1 Ports P0 to P14 Measurement Circuit

$V_{CC1} = V_{CC2} = 5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion and Microprocessor Modes

(for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See **Figure 5.1**		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(3)		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n=1, f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

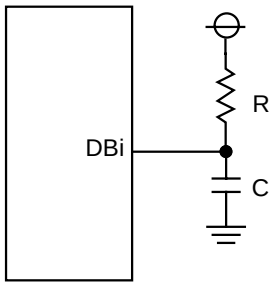
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$

by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output “L” level is

$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$

$= 6.7ns$.



$V_{CC1} = V_{CC2} = 5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion and Microprocessor Modes

(for 2- to 3-wait setting, external area access and multiplex bus selection)

$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)	See **Figure 5.1**	4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-HLDA)}$	HLDA output delay time			40	ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (refers to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (refers to BCLK)		– 4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (refers to Address)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (refers to Adderss)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Adress		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Adress		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25 \quad [ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \quad [ns]$$

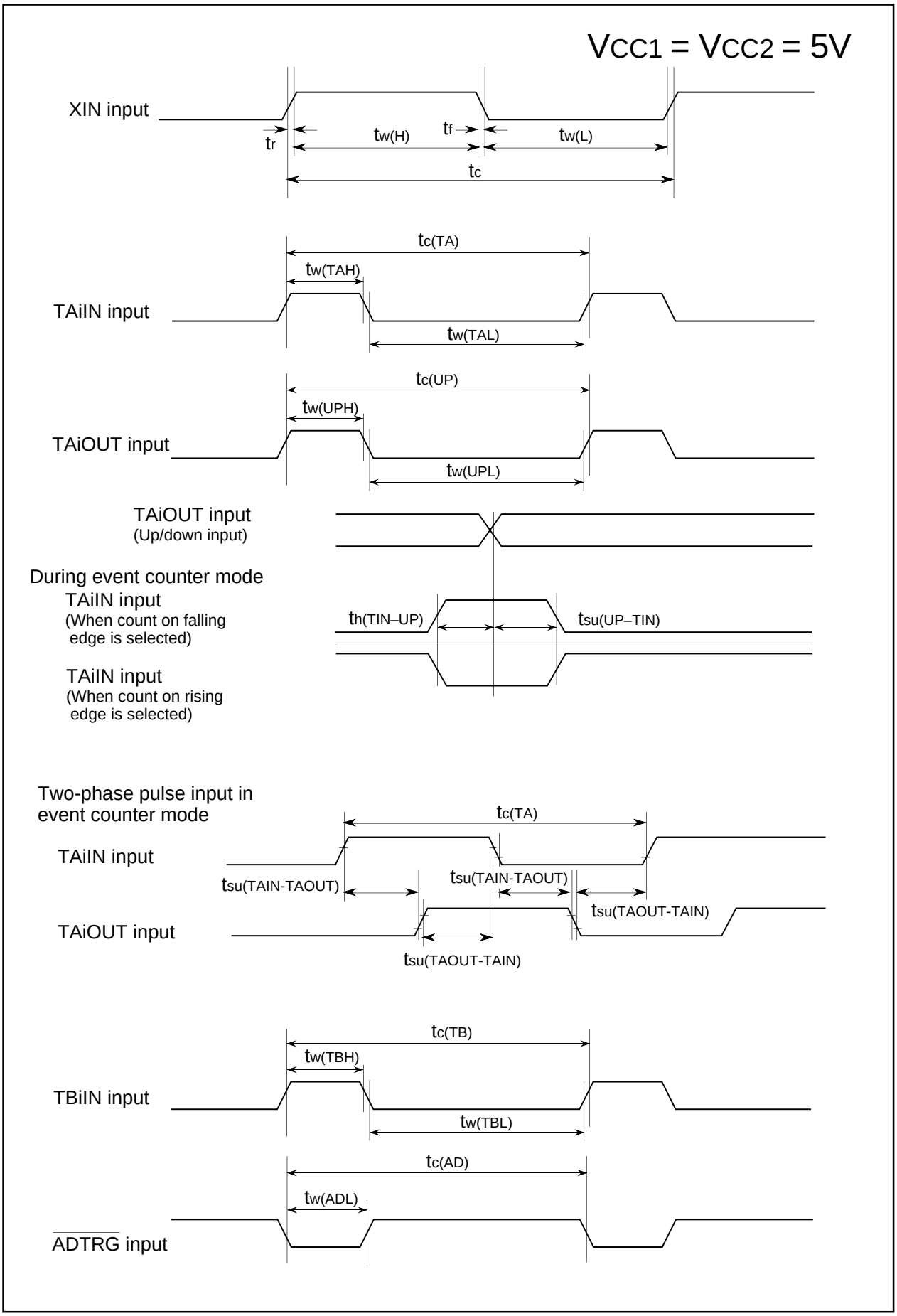


Figure 5.2 Timing Diagram (1)

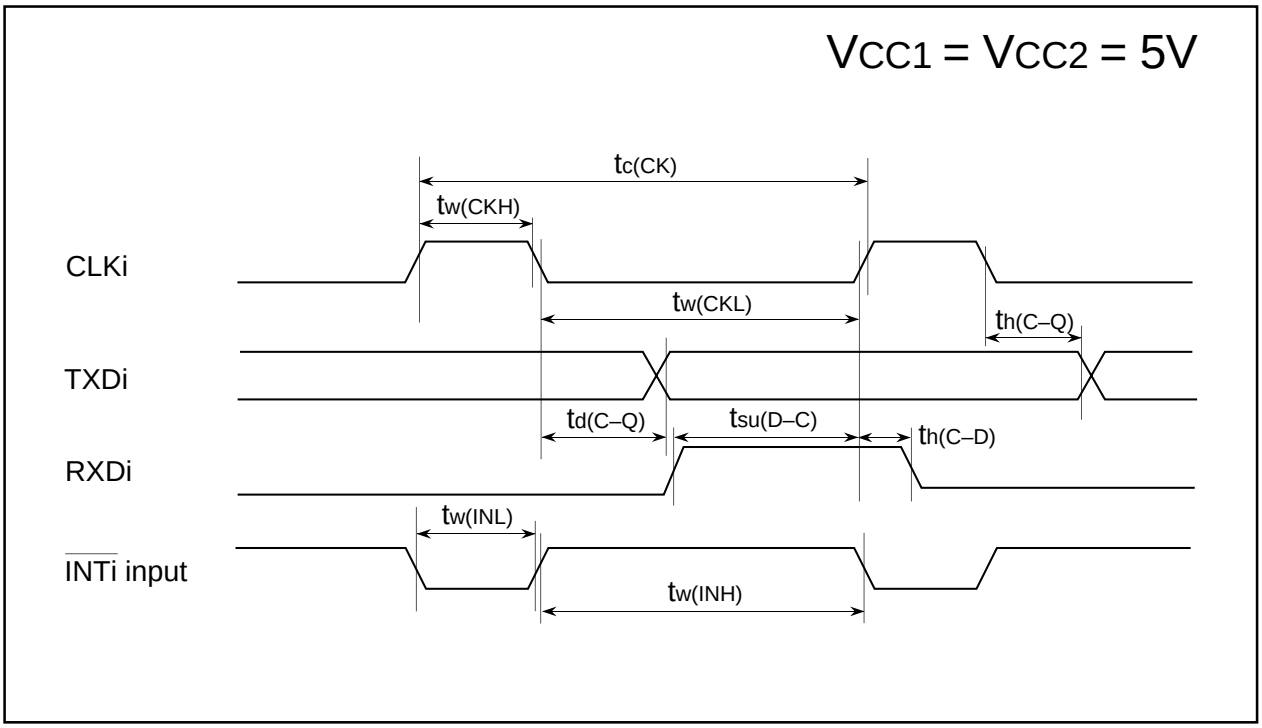
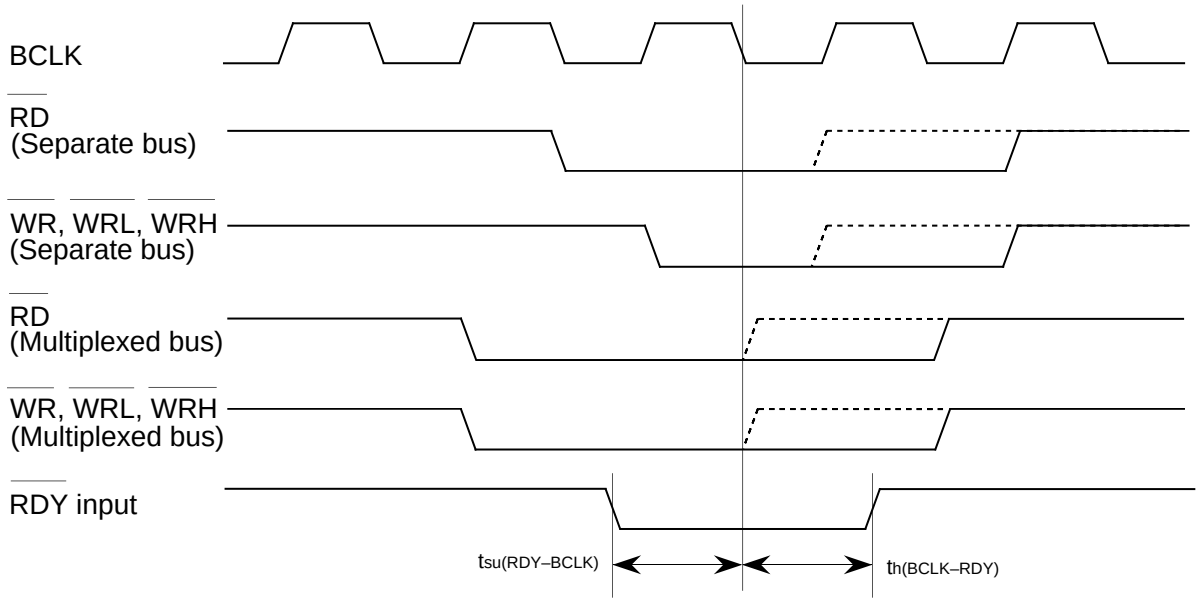


Figure 5.3 Timing Diagram (2)

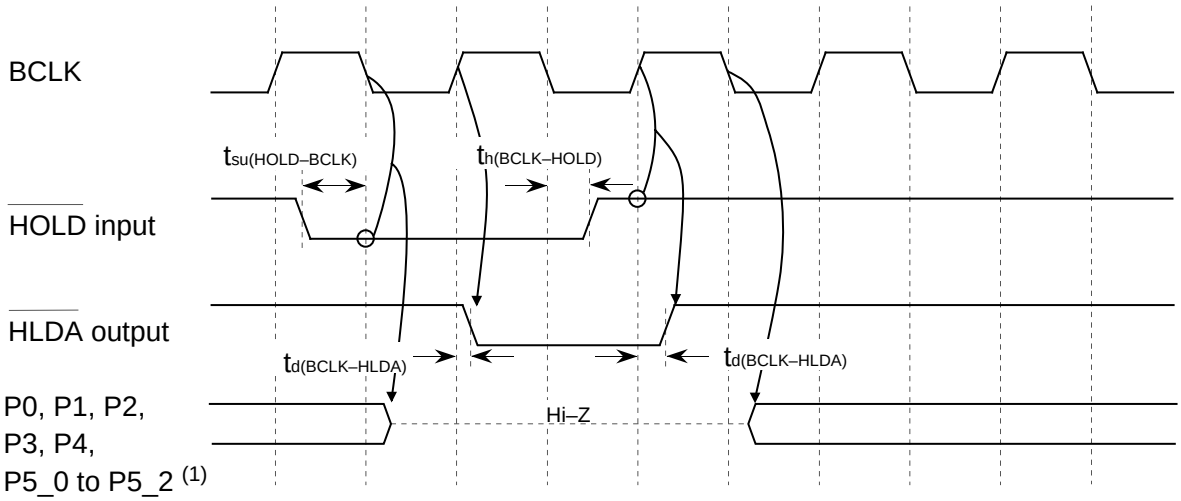
$V_{CC1} = V_{CC2} = 5V$

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait**)**



(Common to setting with wait and setting without wait**)**



NOTES:

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : Determined with V_{IL}=1.0V, V_{IH}=4.0V
- Output timing voltage : Determined with V_{OL}=2.5V, V_{OH}=2.5V

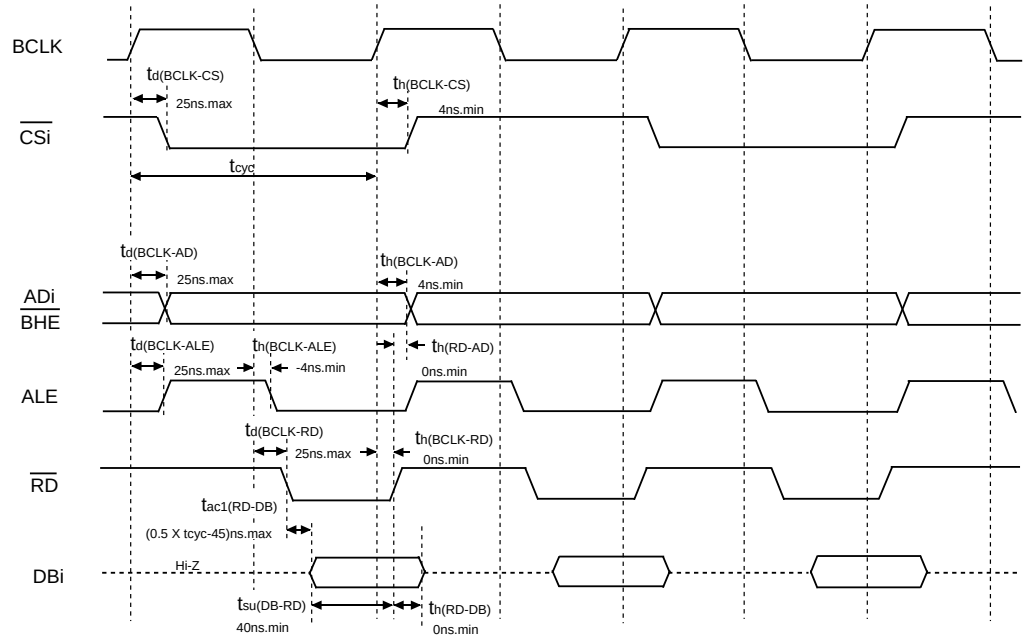
Figure 5.4 Timing Diagram (3)

$V_{CC1} = V_{CC2} = 5V$

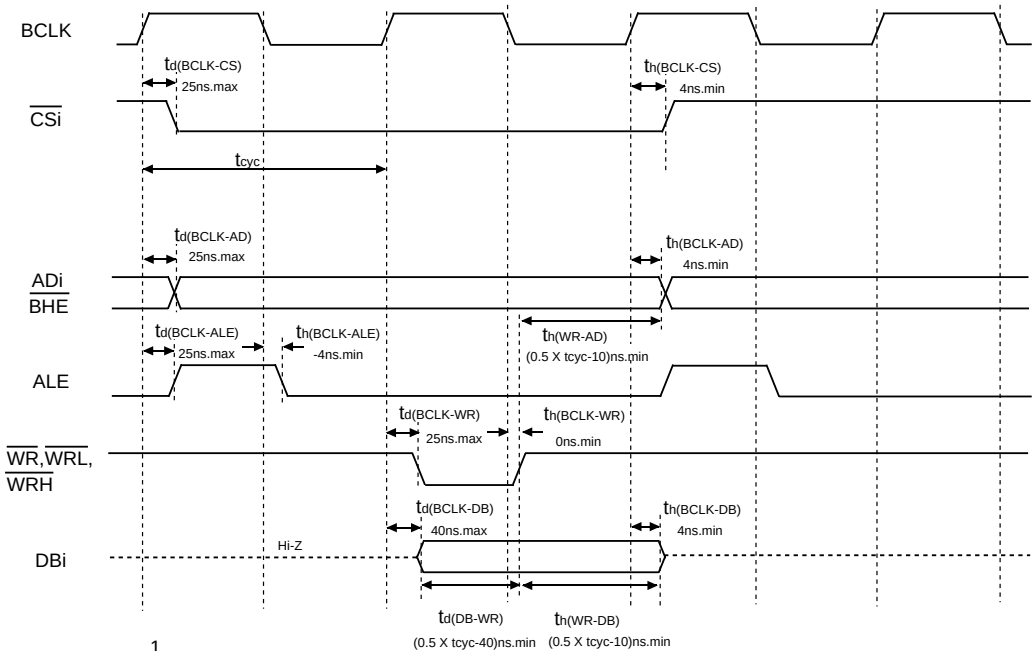
Memory Expansion Mode, Microprocessor Mode

(For setting with no wait**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

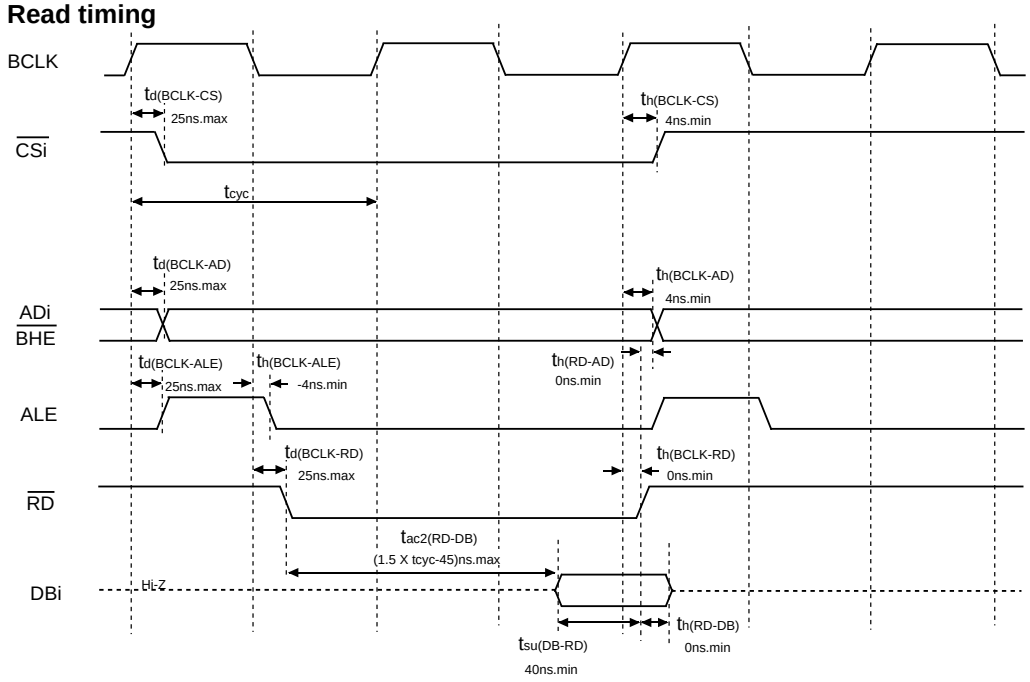
Figure 5.5 Timing Diagram (4)

$V_{CC1} = V_{CC2} = 5V$

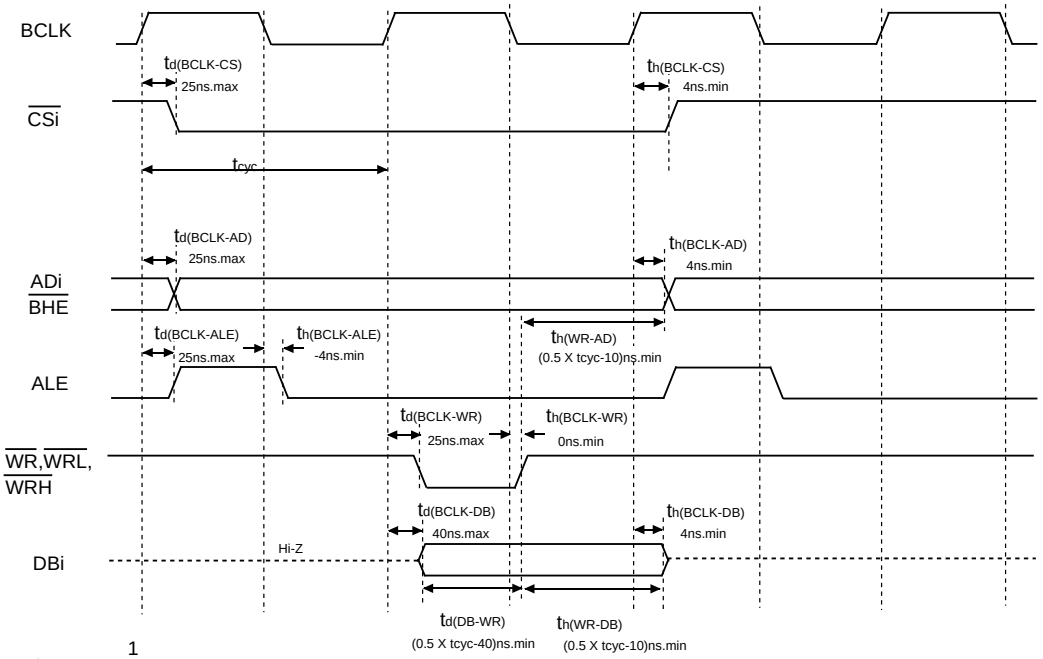
Memory Expansion Mode, Microprocessor Mode

(for 1-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
- Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

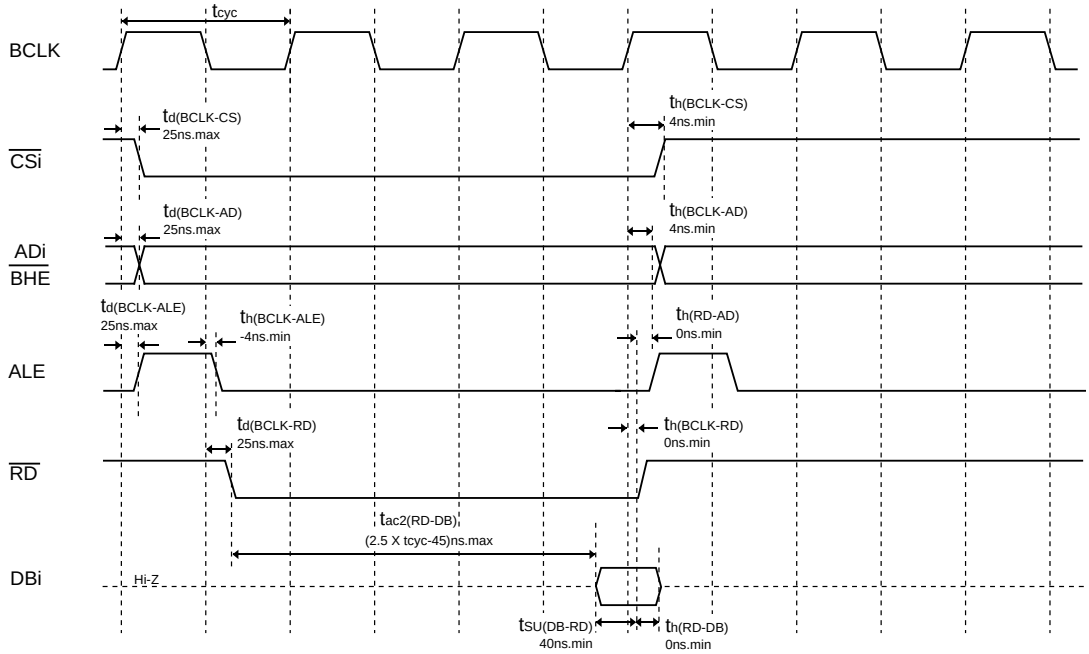
Figure 5.6 Timing Diagram (5)

$V_{CC1} = V_{CC2} = 5V$

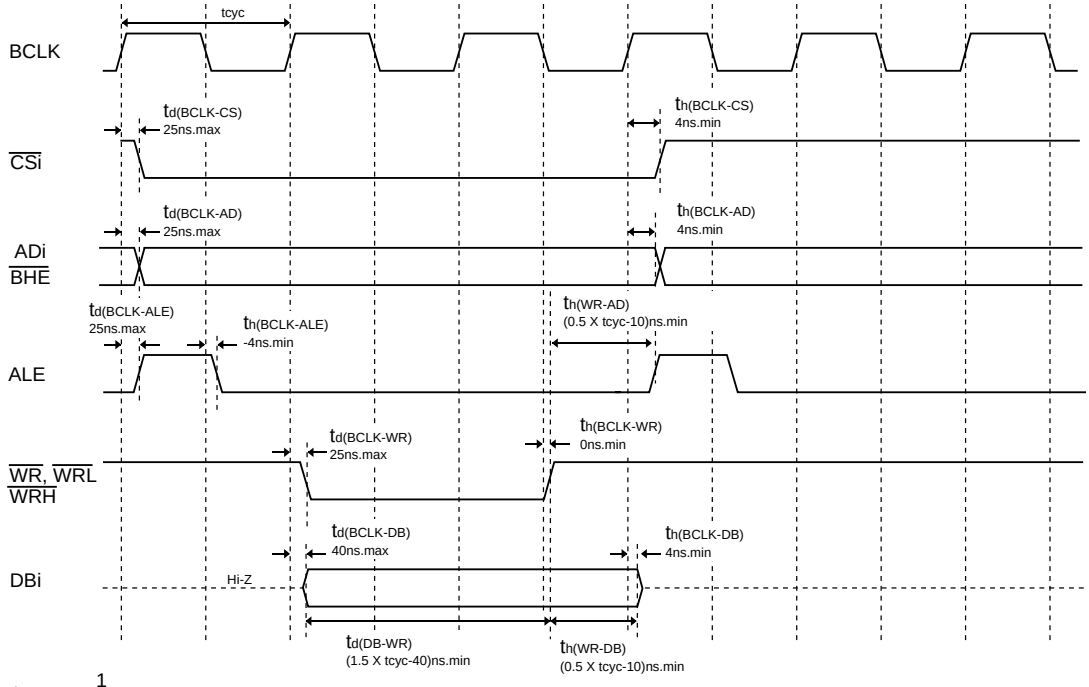
Memory Expansion Mode, Microprocessor Mode

(for 2-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

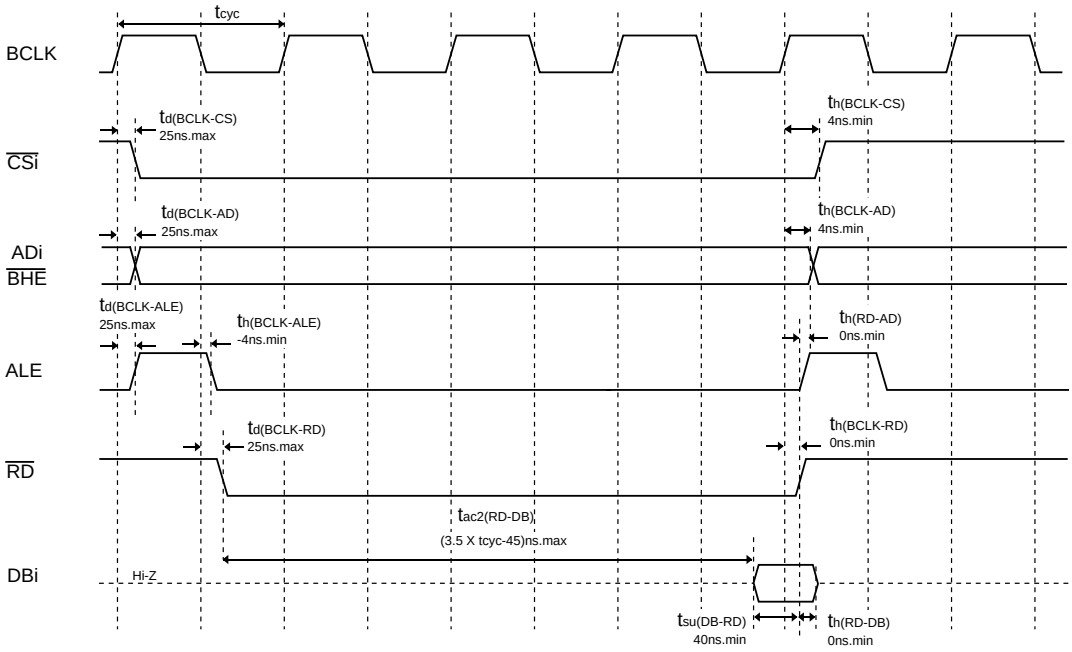
Figure 5.7 Timing Diagram (6)

$V_{CC1} = V_{CC2} = 5V$

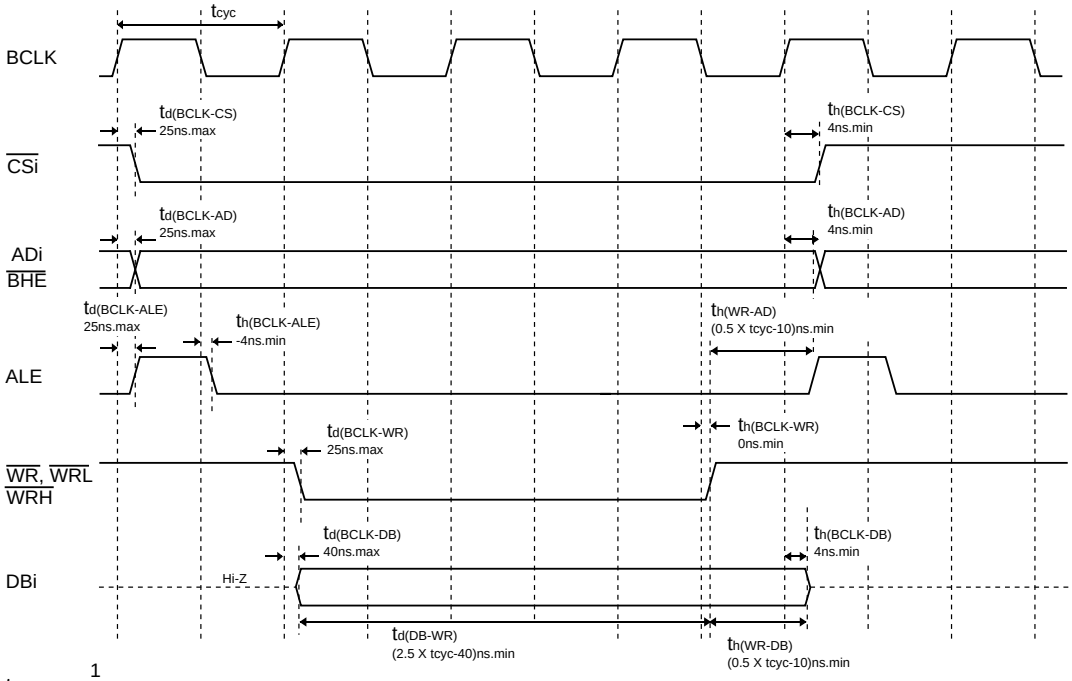
Memory Expansion Mode, Microprocessor Mode

(for 3-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

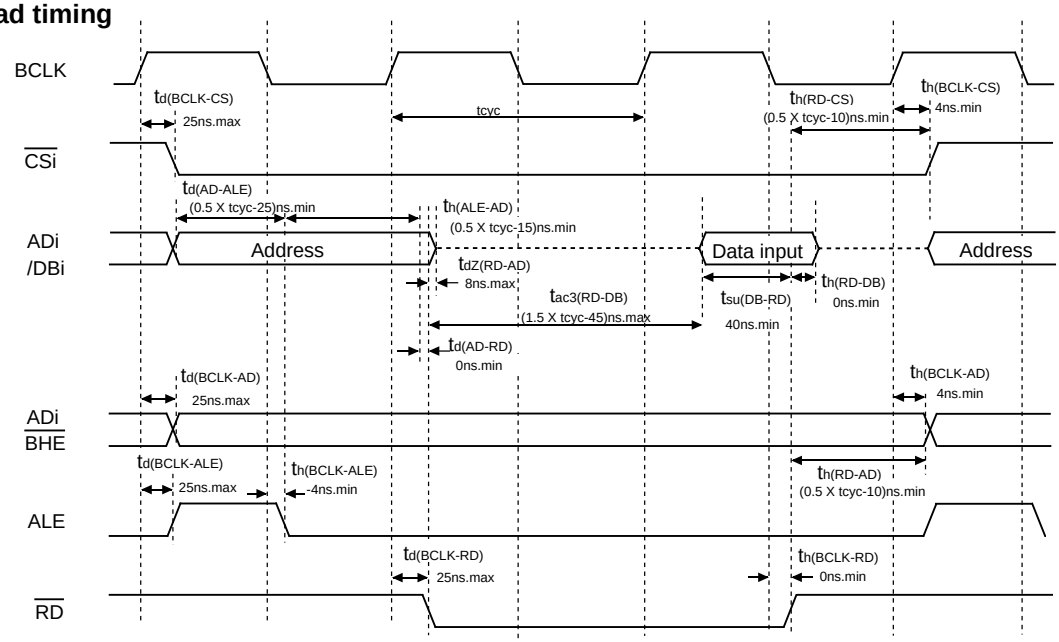
Figure 5.8 Timing Diagram (7)

$V_{CC1} = V_{CC2} = 5V$

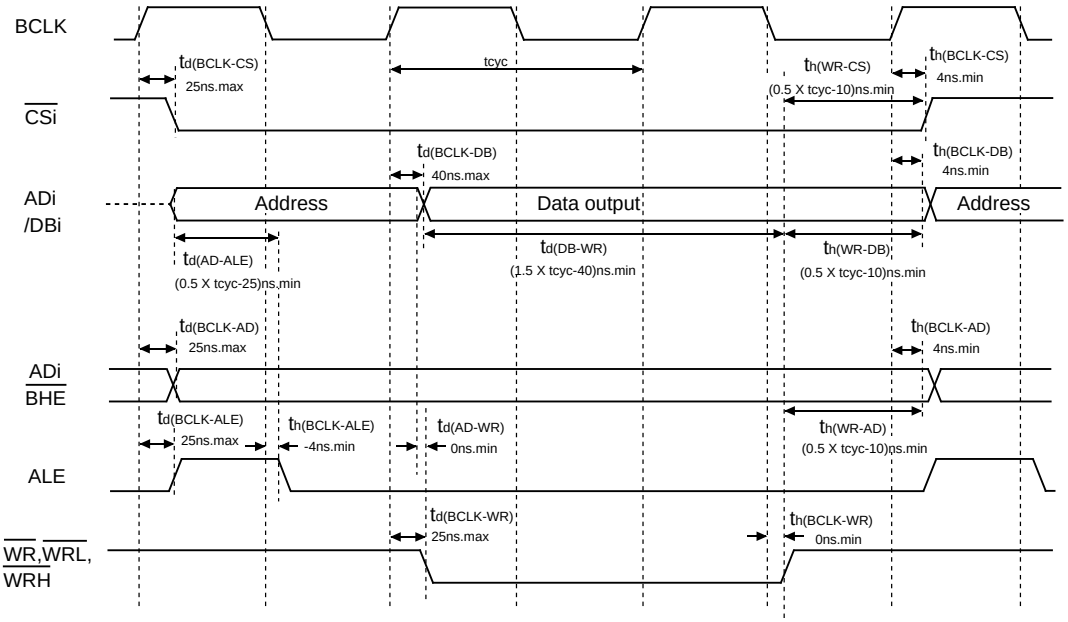
Memory Expansion Mode, Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

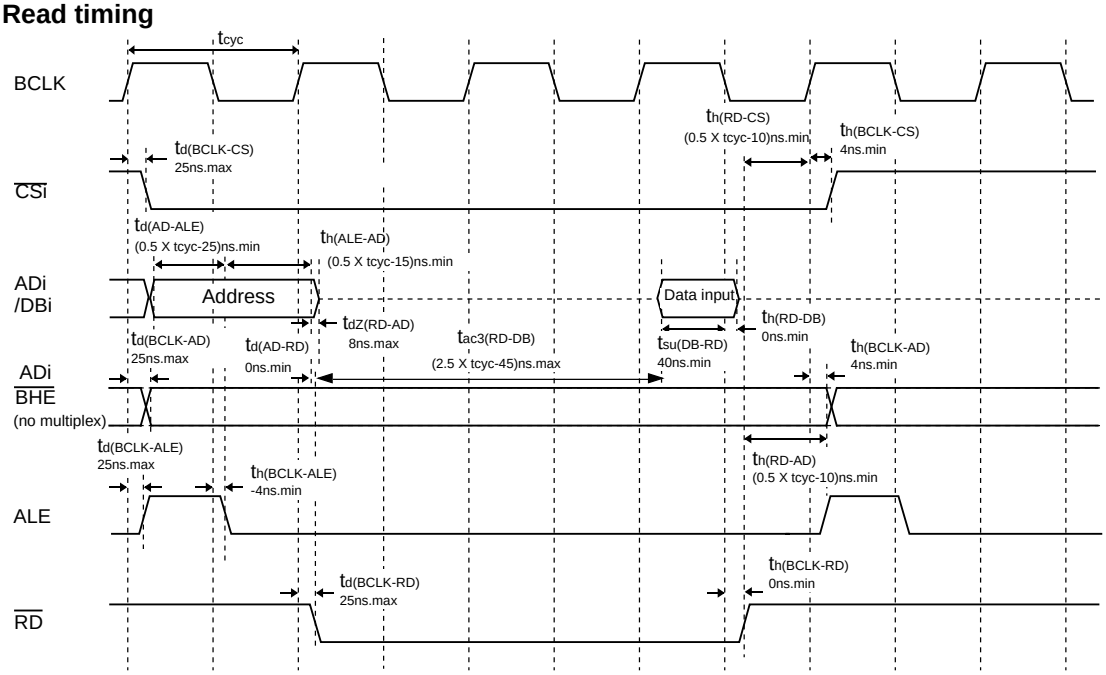
Figure 5.9 Timing Diagram (8)

$V_{CC1} = V_{CC2} = 5V$

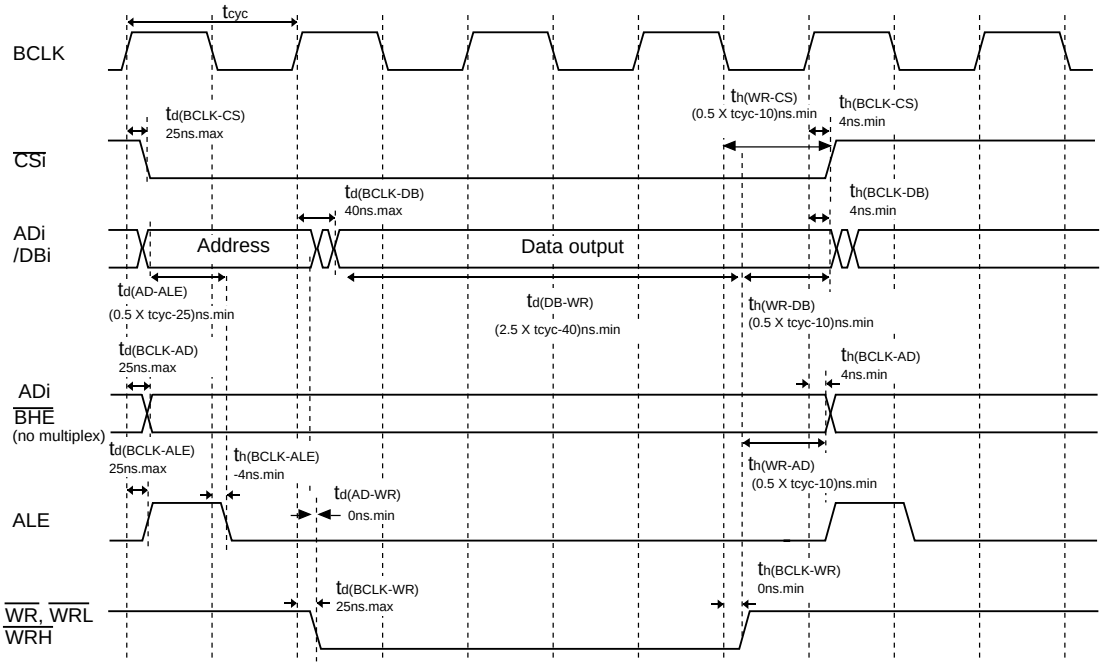
Memory Expansion Mode, Microprocessor Mode

(For 3-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

Figure 5.10 Timing Diagram (9)

$V_{CC1} = V_{CC2} = 3V$

Table 5.30 Electrical Characteristics (1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=-1mA	V_{CC1}-0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=-1mA (2)	V_{CC2}-0.5		V_{CC2}	
V_{OH}	HIGH output voltage XOUT	HIGHPOWER	I_{OH}=-0.1mA	V_{CC1}-0.5		V_{CC1}	V
		LOWPOWER	I_{OH}=-50µA	V_{CC1}-0.5		V_{CC1}	
	HIGH output voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=1mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=1mA (2)			0.5	
V_{OL}	LOW output voltage XOUT	HIGHPOWER	I_{OL}=0.1mA			0.5	V
		LOWPOWER	I_{OL}=50µA			0.5	
	LOW output voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SIN3, SIN4		0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2	(0.7)	1.8	V
V_{T+}-V_{T-}	Hysteresis	XIN		0.2		0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=3V			4.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=0V			-4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V_I=0V	50	100	500	kΩ
R_{fXIN}	Feedback resistance	XIN			3.0		MΩ
R_{fXCIN}	Feedback resistance	XCIN			25		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS}=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.
2. V_{CC1} for the port P6 to P11 and P14, and V_{CC2} for the port P0 to P5 and P12 to P13.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1} = V_{CC2} = 3V$

Table 5.31 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC1}=2.7 to 3.6V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=10MHz, No division		8	11	mA
				No division, Ring oscillation		1		mA
			Flash memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, Ring oscillation		1.8		mA
			Flash memory Program	f(BCLK)=10MHz, V_{CC1}=3.0V		12		mA
			Flash memory Erase	f(BCLK)=10MHz, V_{CC1}=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz, Low power dissipation mode, ROM (3)		25		µA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM (3)		25		µA
				f(BCLK)=32kHz, Low power dissipation mode, Flash memory (3)		420		µA
				Ring oscillation, Wait mode		45		µA
			Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (2), Oscillation capacity High		6.0		µA
				f(BCLK)=32kHz, Wait mode (2), Oscillation capacity Low		1.8		µA
				Stop mode, T_{opr}=25°C		0.7	3.0	µA
I_{det4}	Voltage down detection dissipation current (4)					0.6	4	µA
I_{det3}	Reset level detection dissipation current (4)					0.4	2	µA
I_{det2}	RAM retention limit detection dissipation current (4)					0.9	4	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
   I_{det4}: VC27 bit of VCR2 register
   I_{det3}: VC26 bit of VCR2 register
   I_{det2}: VC25 bit of VCR2 register

$V_{CC1} = V_{CC2} = 3V$

Timing Requirements

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.32 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

Table 5.33 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	50		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 60 \quad [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \quad [ns]$$

n is “2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

$V_{CC1} = V_{CC2} = 3V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.34 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	60		ns

Table 5.35 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	300		ns

Table 5.36 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 5.37 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 5.38 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	600		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	600		ns

Table 5.39 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

$V_{CC1} = V_{CC2} = 3V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.40 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	120		ns

Table 5.41 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 5.42 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 5.43 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

Table 5.44 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	50		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.45 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

$V_{CC1} = V_{CC2} = 3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.46 Memory Expansion, Microprocessor Modes (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See **Figure 5.11**		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(3)		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

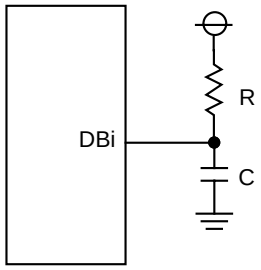
$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



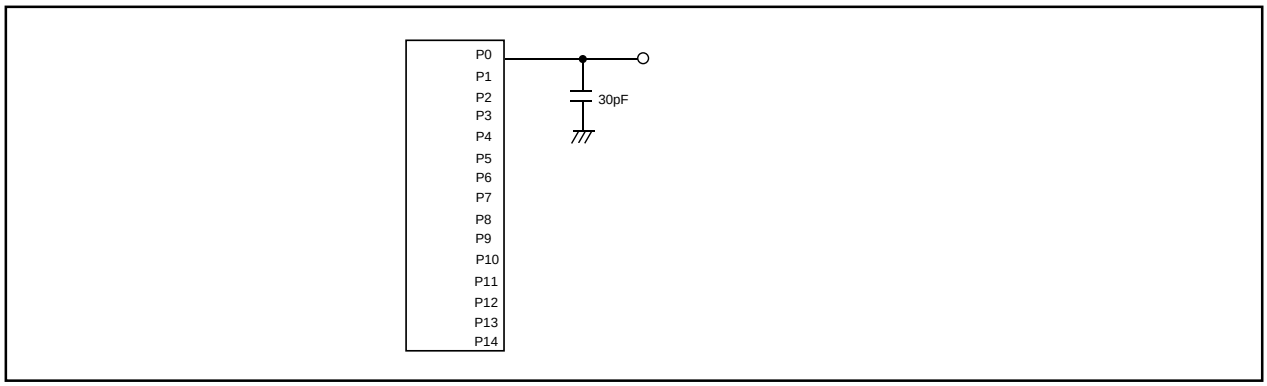


Figure 5.11 Ports P0 to P14 Measurement Circuit

$V_{CC1} = V_{CC2} = 3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 5.47 Memory expansion and Microprocessor Modes

(for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See **Figure 5.11**		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(3)		(Note 2)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n=1, f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

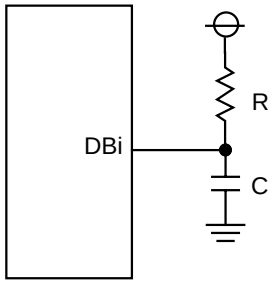
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$

by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output “L” level is

$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$

$= 6.7ns$.



$V_{CC1} = V_{CC2} = 3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C, unless otherwise specified)

Table 5.48 Memory expansion and Microprocessor Modes

(for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See **Figure 5.11**		50	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			50	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			40	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			40	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (refers to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (refers to BCLK)		– 4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (refers to Address)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (refers to Adderss)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Address		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 50 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \quad [ns]$$

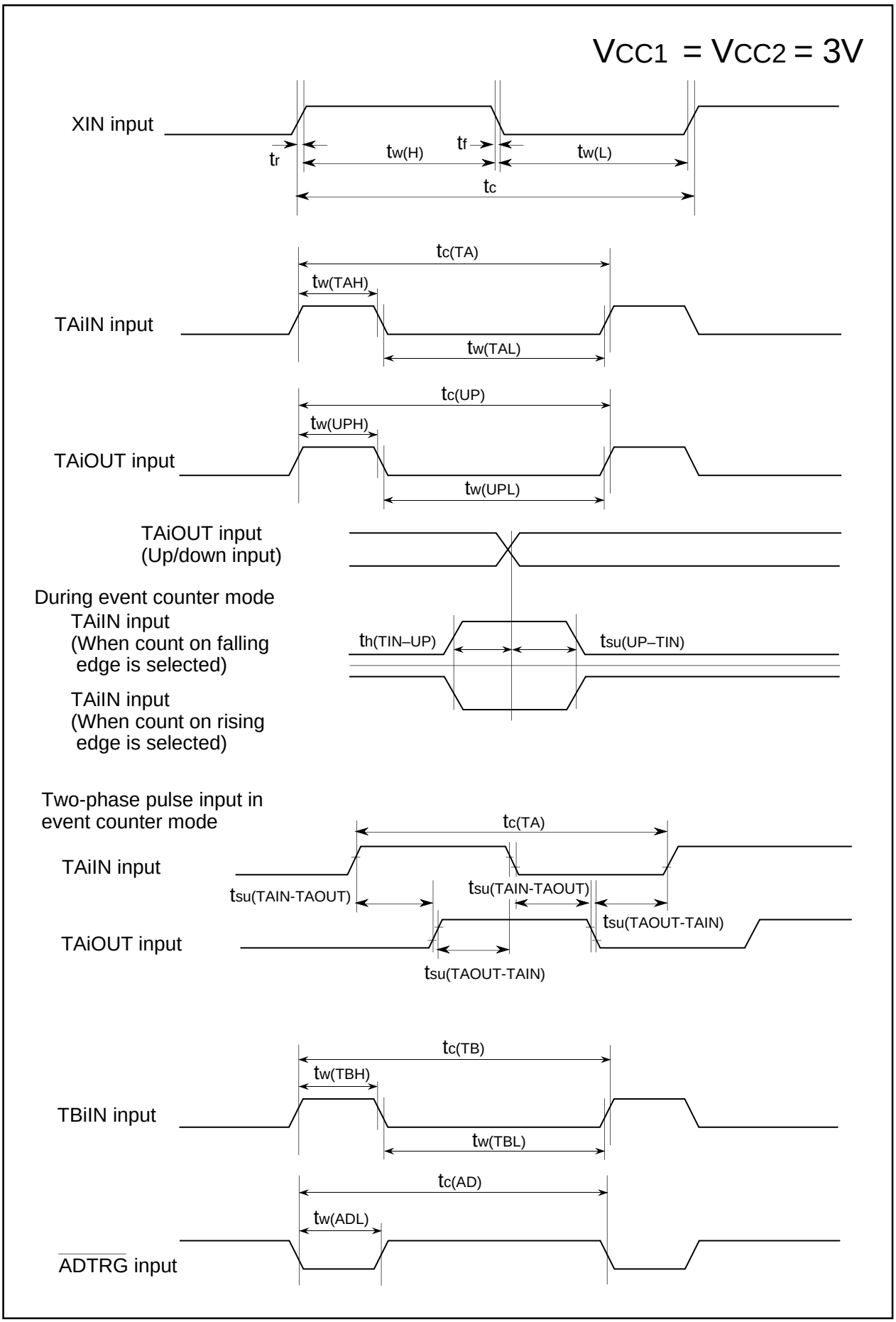


Figure 5.12 Timing Diagram (1)

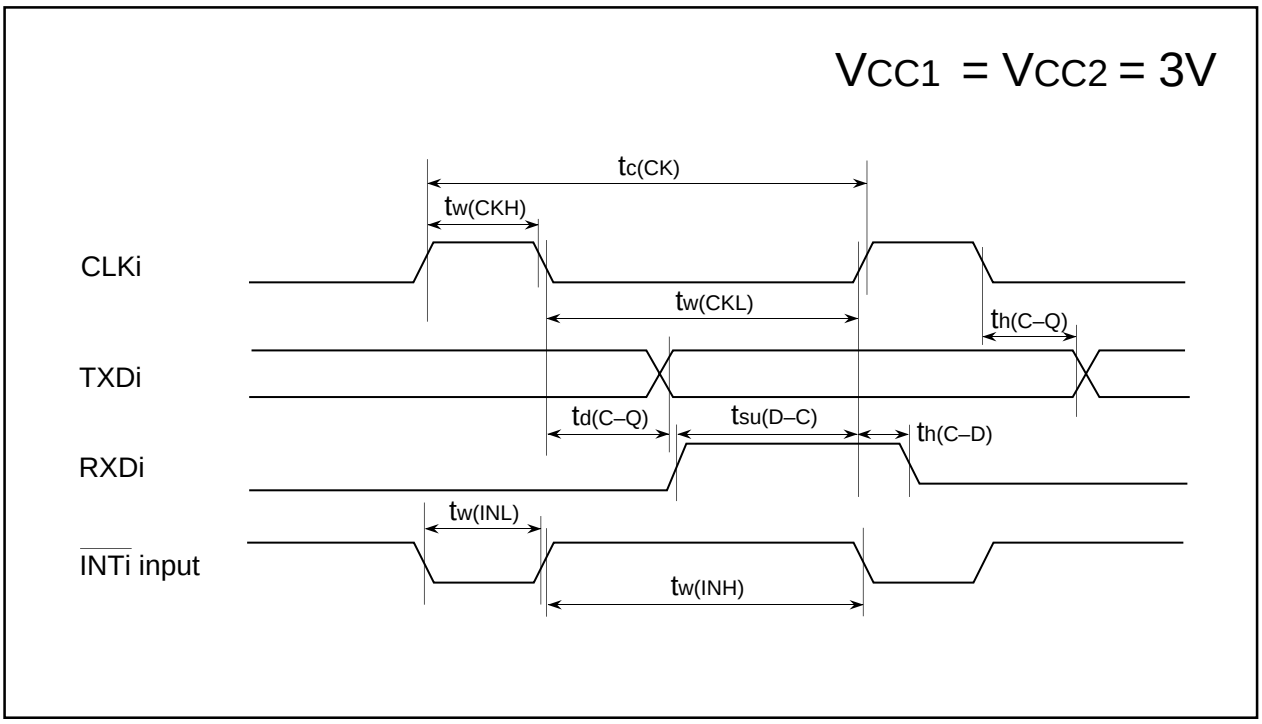
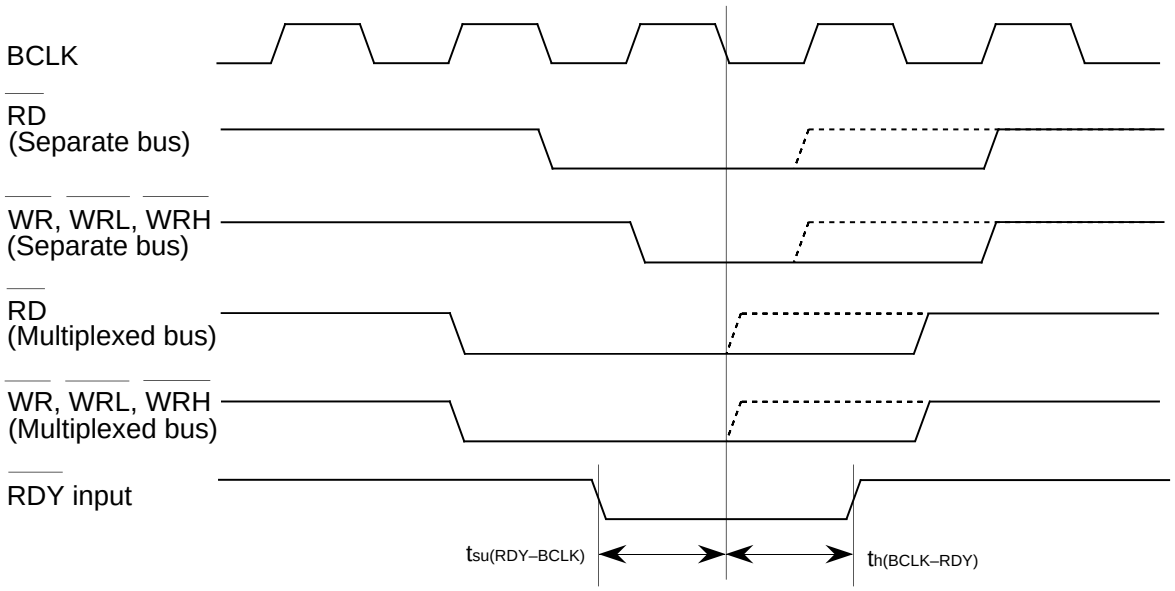


Figure 5.13 Timing Diagram (2)

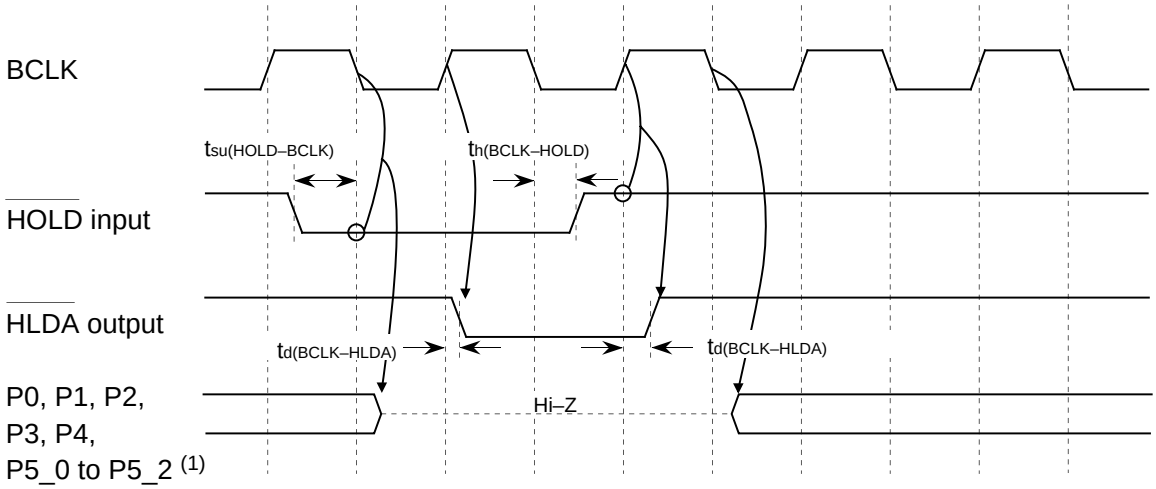
$V_{CC1} = V_{CC2} = 3V$

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



NOTES:

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

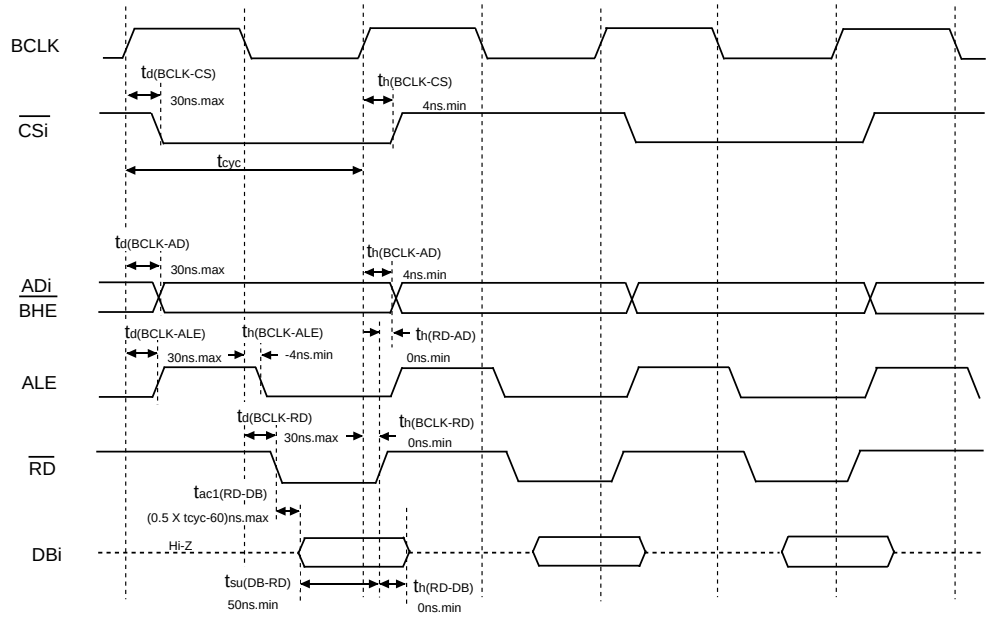
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : Determined with V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : Determined with V_{OL}=1.5V, V_{OH}=1.5V

Figure 5.14 Timing Diagram (3)

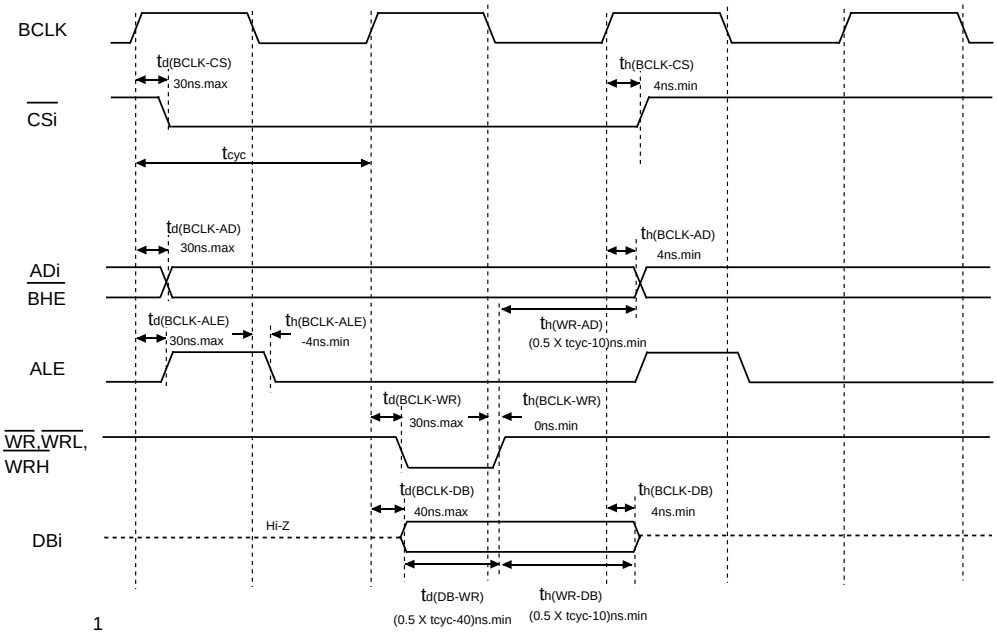
$V_{CC1} = V_{CC2} = 3V$

Memory Expansion Mode, Microprocessor Mode
(For setting with no wait**)**

Read timing



Write timing



$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

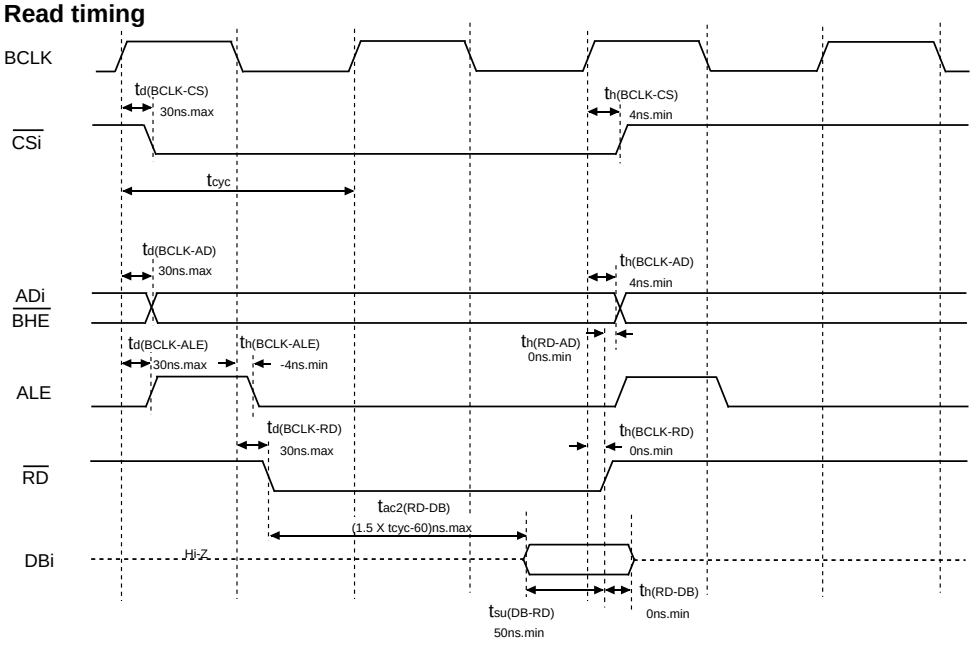
Figure 5.15 Timing Diagram (4)

$V_{CC1} = V_{CC2} = 3V$

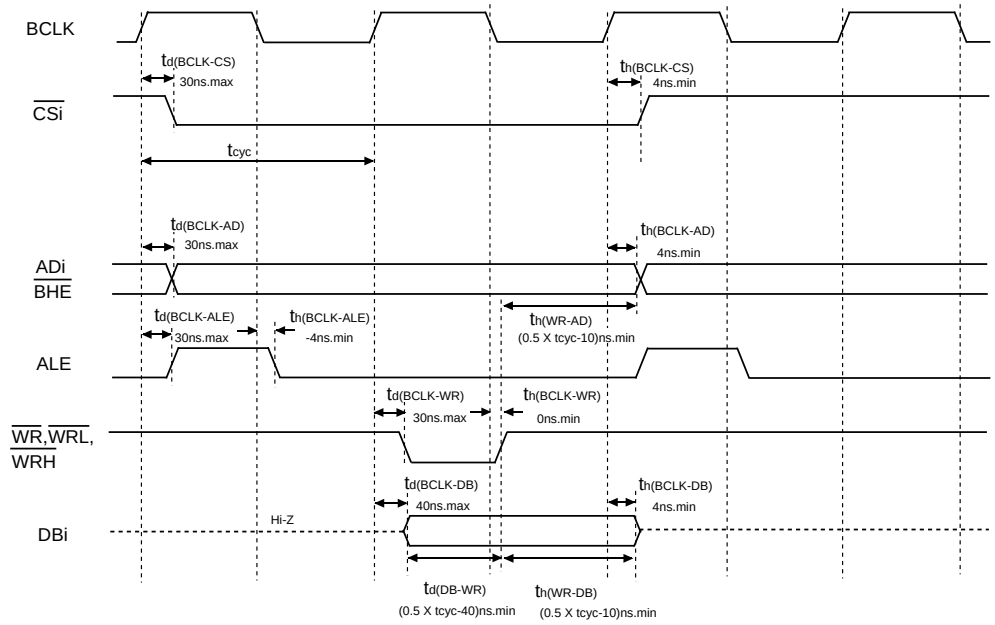
Memory Expansion Mode, Microprocessor Mode

(for 1-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

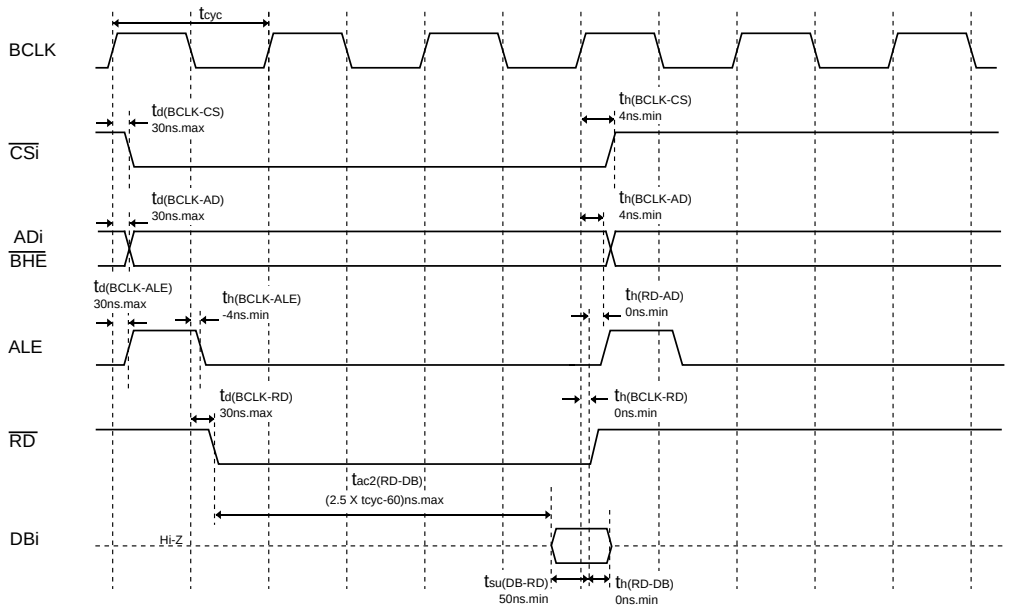
Figure 5.16 Timing Diagram (5)

$V_{CC1} = V_{CC2} = 3V$

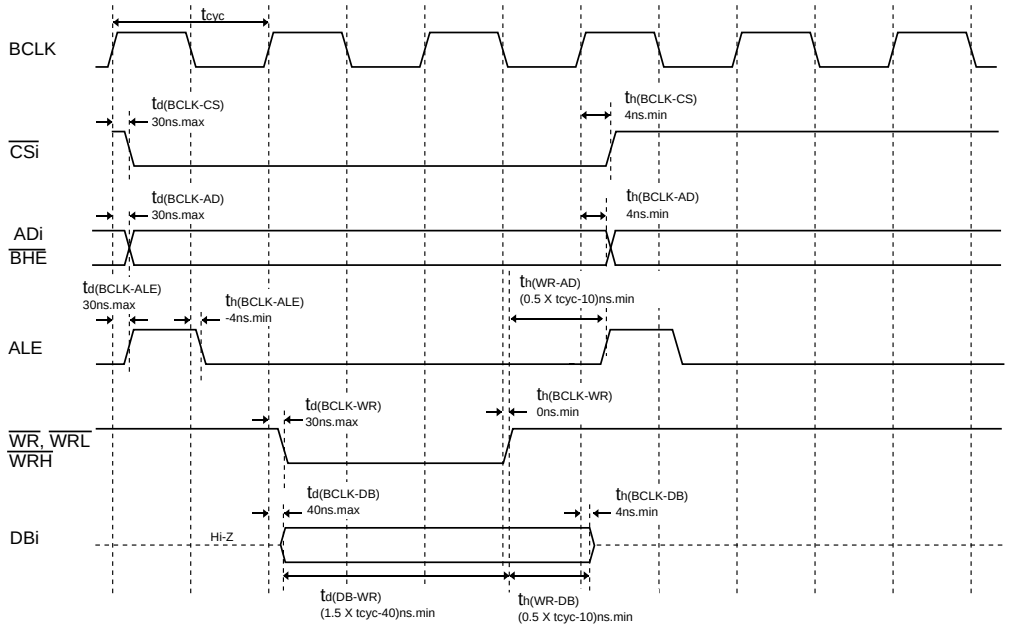
Memory Expansion Mode, Microprocessor Mode

(for 2-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

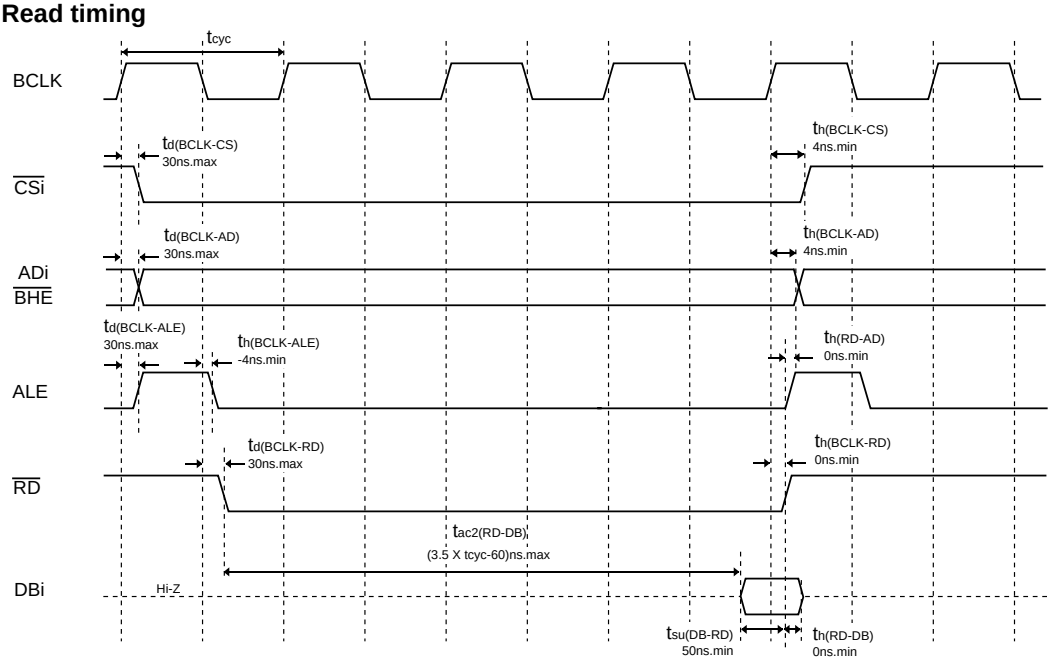
Figure 5.17 Timing Diagram (6)

$V_{CC1} = V_{CC2} = 3V$

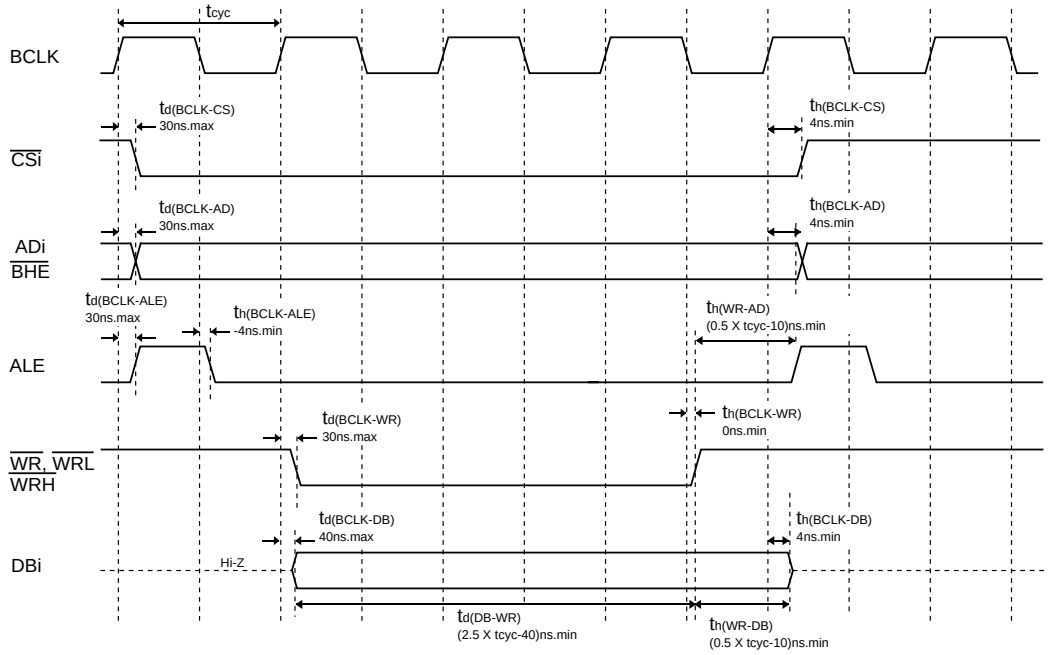
Memory Expansion Mode, Microprocessor Mode

(for 3-wait setting and external area access)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

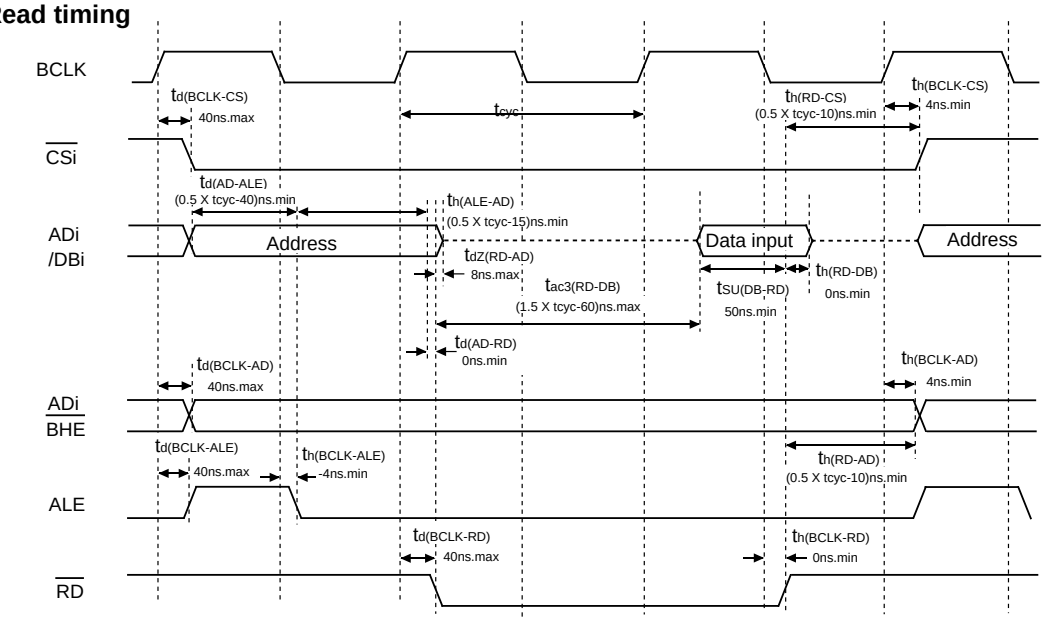
Figure 5.18 Timing Diagram (7)

$V_{CC1} = V_{CC2} = 3V$

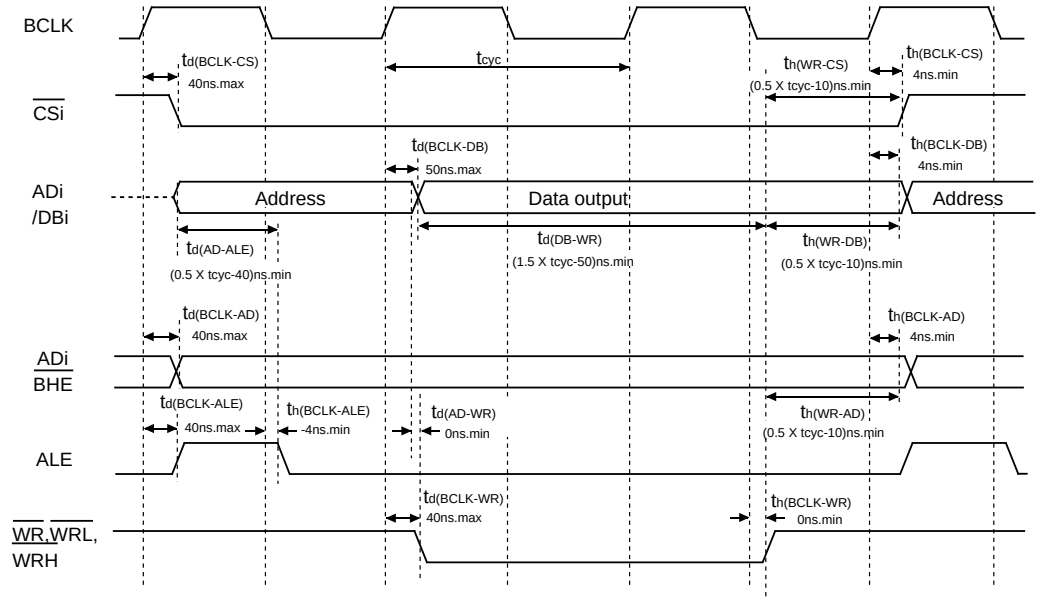
Memory Expansion Mode, Microprocessor Mode

(For 2-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

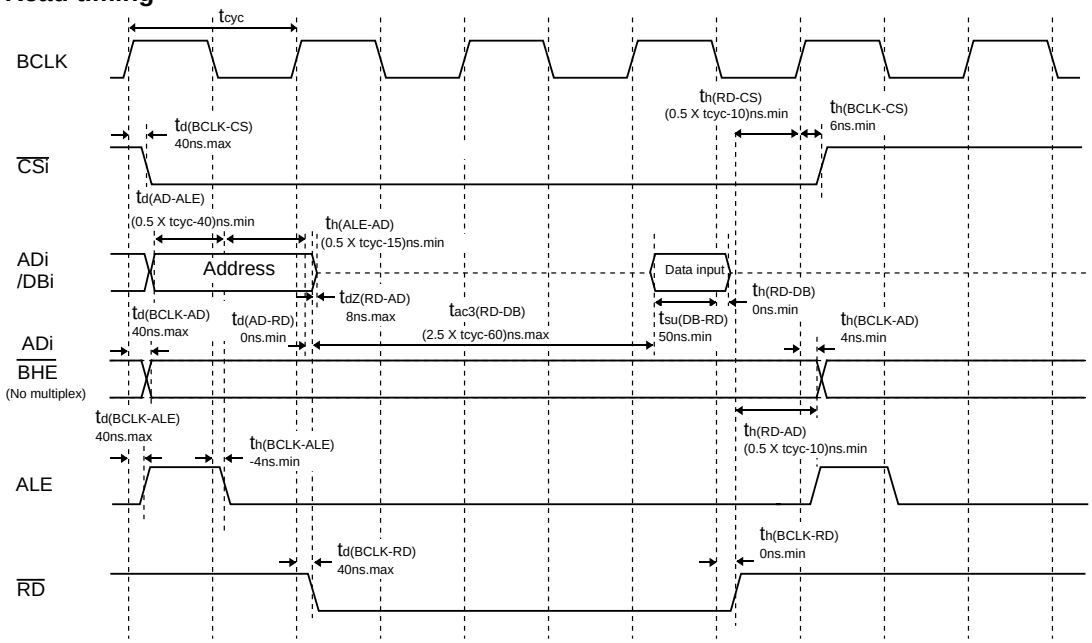
Figure 5.19 Timing Diagram (8)

$V_{CC1} = V_{CC2} = 3V$

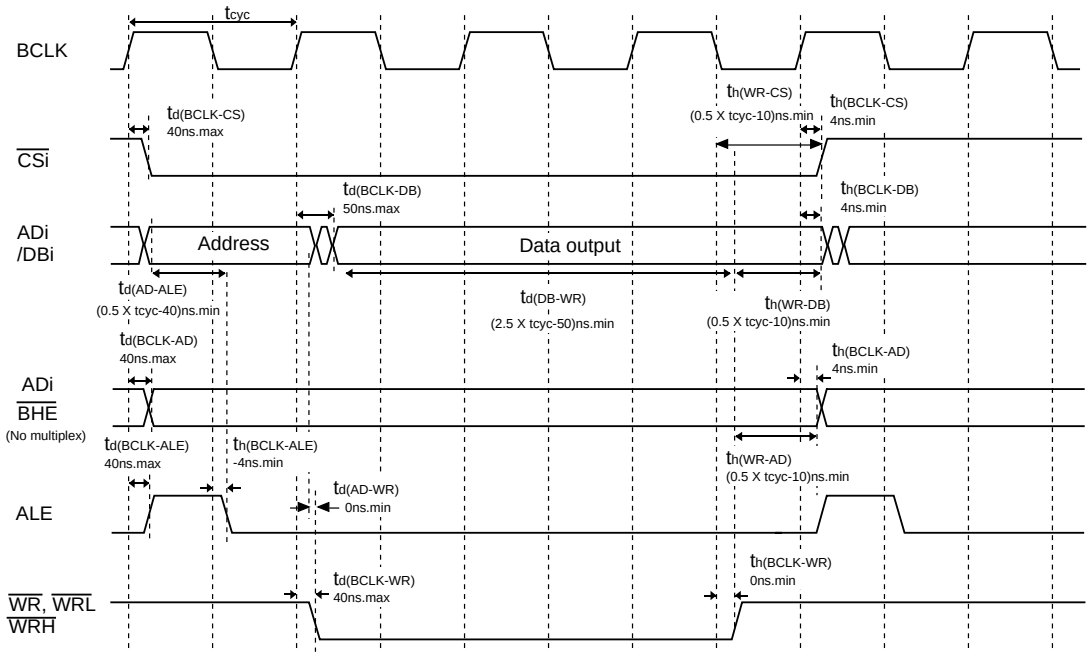
Memory Expansion Mode, Microprocessor Mode

(For 3-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

Figure 5.20 Timing Diagram (9)

5.2 Electrical Characteristics (M16C/62PT)

Table 5.49 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
V_{CC1}, V_{CC2}	Supply voltage		V_{CC1}=AVcc	-0.3 to 6.5	V
V_{CC2}	Supply voltage		V_{CC2}	-0.3 to V_{CC1}+0.1	V
AVcc	Analog supply voltage		V_{CC1}=AVcc	-0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		-0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		-0.3 to 6.5	V
V_O	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11 0 to P11_7, P14_0, P14_1, XOUT		-0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		-0.3 to 6.5	V
P_d	Power dissipation		-40 ° C < T_{opr} ≤ 85 ° C	300	mW
			-40 ° C < T_{opr} ≤ 125 ° C	200	
T_{opr}	Operating ambient temperature	When the microcomputer is operating		-40 to 85 / -40 to 125 (2)	° C
		Flash program erase		0 to 60	
T_{stg}	Storage temperature			-65 to 150	° C

NOTES :
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = -40 to 85 ° C, V version = -40 to 125 ° C.

Table 5.50 Recommended Operating Conditions (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage(V_{CC1}=V_{CC2})		4.0	5.0	5.5	V
AVcc	Analog supply voltage			V_{CC1}		V
Vss	Supply voltage			0		V
AVss	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	0.8V_{CC1}		V_{CC1}	V
		P7_0 , P7_1	0.8V_{CC1}		6.5	V
V_{IL}	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V_{CC2}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	0		0.2V_{CC1}	V
$I_{OH (peak)}$	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
$I_{OH (avg)}$	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-5.0	mA
$I_{OL (peak)}$	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL (avg)}$	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA
f (XIN)	Main clock input oscillation frequency	V_{CC1}=4.0 to 5.5V	0		16	MHz
f (XCIN)	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	Ring oscillation frequency		0.5	1	2	MHz
f (PLL)	PLL clock oscillation frequency (4)	V_{CC1}=4.0 to 5.5V	10		24	MHz
f (BCLK)	CPU operation clock		0		24	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	V_{CC1}=5.0V			20	ms

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 4.7 to 5.5V at Topr = -40 to 85 °C / -40 to 125 °C unless otherwise specified.
   T version = -40 to 85 °C, V version = -40 to 125 °C.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0 and P14_1 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be -40mA max. The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be -40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.
   As for 80-pin version, the total $I_{OL(peak)}$ for all ports and $I_{OH(peak)}$ must be 80mA. max. due to one V_{CC} and one V_{SS}.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.51 A-D Conversion Characteristics (1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{REF} =V_{CC1}				10	Bits
INL	Integral non-linearity error	10 bit	V_{REF}= V_{CC1}= 5V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bit	V_{REF} =V_{CC1}=3.3V				±2	LSB
–	Absolute accuracy	10 bit	V_{REF}= V_{CC1}= 5V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bit	V_{REF} =V_{CC1}=3.3V				±2	LSB
–	Tolerance level impedance					3		kΩ
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R_{LADDER}	Ladder resistance		V_{REF} =V_{CC1}		10		40	kΩ
t_{CONV}	Conversion time(10bit), Sample & hold function available		V_{REF} =V_{CC1}=5V, øAD=12MHz		2.75			µs
t_{CONV}	Conversion time(8bit), Sample & hold function available		V_{REF} =V_{CC1}=5V, øAD=12MHz		2.33			µs
t_{SAMP}	Sampling time				0.25			µs
V_{REF}	Reference voltage				2.0		V_{CC1}	V
V_{IA}	Analog input voltage				0		V_{REF}	V

NOTES:
1. Referenced to V_{CC1}=AV$_{CC}$=V_{REF}=4.0 to 5.5V, V_{SS}=AV$_{SS}$=0V at T_{opr} = -40 to 85 °C / -40 to 125 °C unless otherwise specified. T version = -40 to 85 °C, V version = -40 to 125 °C.
2. AD operation clock frequency (øAD frequency) must be 12 MHz or less.
3. A case without sample & hold function turn øAD frequency into 250 kHz or more in addition to a limit of Note 2.
   A case with sample & hold function turn øAD frequency into 1MHz or more in addition to a limit of Note 2.

Table 5.52 D-A Conversion Characteristics (1)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference power supply input current	(Note 2)			1.5	mA

NOTES :
1. Referenced to V_{CC1}=V_{REF}=4.0 to 5.5V, V_{SS}=AV$_{SS}$=0V at T_{opr} = -40 to 85 °C / -40 to 125 °C unless otherwise specified. T version=-40 to 85 °C, V version=-40 to 125 °C
2. This applies when using one D-A converter, with the D-A register for the unused D-A converter set to “00h”. The A-D converter’s ladder resistance is not included. Also, when D-A register contents are not “00h”, the current I_{VREF} always flows even though Vref may have been set to be unconnected by the A-D control register.

Table 5.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase endurance (3)		100			cycle
-	Word program time (V_{CC1}=5.0V, T_{opr}=25°C)			25	200	µs
-	Lock bit program time			25	200	µs
-	Block erase time (V_{CC1}=5.0V, T_{opr}=25 °C)	4K bytes block		0.3	4	s
		8K bytes block		0.3	4	s
		32K bytes block		0.5	4	s
		64K bytes block		0.8	4	s
-	Erase all unlocked blocks time (2)				4 X n	s
t_{PS}	Flash memory circuit stabilization wait time				15	µs
-	Data hold time (5)		10			year

Table 5.54 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (Block A and Block 1 (7))

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase endurance (3, 8, 9)		10,000 (4)			cycle
-	Word program time (V_{CC1}=5.0V, T_{opr}=25°C)			25		µs
-	Lock bit program time			25		µs
-	Block erase time (V_{CC1}=5.0V, T_{opr}=25 °C)	4K bytes block		0.3		s
t_{PS}	Flash memory circuit stabilization wait time				15	µs
-	Data hold time (5)		10			year

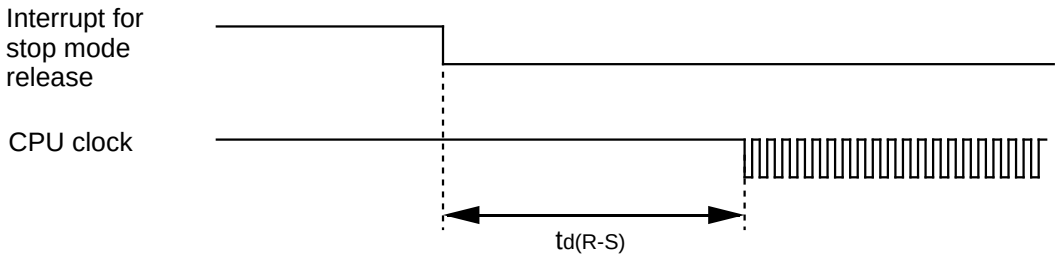
NOTES :
1. Referenced to V_{CC1}=4.5 to 5.5V at T_{opr} = 0 to 60 °C unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4K bytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. T_{opr} = -40 to 85 °C (T version) / -40 to 125 °C (V version).
6. Referenced to V_{CC1} = 4.0 to 5.5V at T_{opr} = -40 to 85 °C (T version) / -40 to 125 °C (V version) unless otherwise specified.
7. Table 5.55 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.54.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary. Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60°C)

Flash program, erase voltage	Flash read operation voltage
V_{CC1}=5.0 ± 0.5 V	V_{CC1}=4.0 to 5.5 V

Table 5.56 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	V_{CC1}=4.0 to 5.5V			2	ms
$t_{d(R-S)}$	STOP release time				150	µs
$t_{d(W-S)}$	Low power dissipation mode wait mode release time				150	µs
$t_{d(M-L)}$	Time for internal power supply stabilization when main clock oscillation starts				50	µs



$V_{CC1} = V_{CC2} = 5V$

Table 5.57 Electrical Characteristics (1)

Symbol	Parameter		Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	HIGH output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=-5mA	V_{CC1}-2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=-5mA (2)	V_{CC2}-2.0		V_{CC2}	
V_{OH}	HIGH output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=-200µA	V_{CC1}-0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=-200µA (2)	V_{CC2}-0.3		V_{CC2}	
V_{OH}	HIGH output voltage XOUT	HIGHPOWER	I_{OH}=-1mA	V_{CC1}-2.0		V_{CC1}	V
		LOWPOWER	I_{OH}=-0.5mA	V_{CC1}-2.0		V_{CC1}	
	HIGH output voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=5mA (2)			2.0	
V_{OL}	LOW output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=200µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=200µA (2)			0.45	
V_{OL}	LOW output voltage XOUT	HIGHPOWER	I_{OL}=1mA			2.0	V
		LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW output voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL0 to SCL2, SDA0 TO SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SIN3, SIN4		0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	XIN		0.2		0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=5V			5.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback resistance	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistance	XCIN			15		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.0 to 5.5V, V_{SS}=0V at T_{opr} = -40 to 85 °C / -40 to 125 °C, f(BCLK)=24MHz unless otherwise specified.
   T version is -40 = 85 °C, V version = -40 to 125 °C.
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1} = V_{CC2} = 5V$

Table 5.58 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC1}=4.0 to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=24MHz, No division, PLL operation		14	20	mA
				No division, Ring oscillation		1		mA
			Flash memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, Ring oscillation		1.8		mA
			Flash memory Program	f(BCLK)=10MHz, V_{CC1}=5.0V		15		mA
			Flash memory Erase	f(BCLK)=10MHz, V_{CC1}=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz, Low power dissipation mode, ROM (3)		25		µA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM (3)		25		µA
				f(BCLK)=32kHz Low power dissipation mode, Flash memory (3)		420		µA
				Ring oscillation, Wait mode		50		µA
			Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (2), Oscillation capacity High		7.5		µA
				f(BCLK)=32kHz, Wait mode (2), Oscillation capacity Low		2.0		µA
				Stop mode, T_{opr}=25°C		0.8	3.0	µA
I_{det4}	Voltage down detection dissipation current (4)					0.7	4	µA
I_{det3}	Reset area detection dissipation current (4)					1.2	8	µA
I_{det2}	RAM retention limit detection dissipation current (4)					1.1	6	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}= 4.0 to 5.5V, V_{SS}=0V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.
   T version = -40 to 85 °C, V version = -40 to 125 °C
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
   I_{det4}: VC27 bit of VCR2 register
   I_{det3}: VC26 bit of VCR2 register
   I_{det2}: VC25 bit of VCR2 register

$V_{CC1} = V_{CC2} = 5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 40 to 85°C (T version) / – 40 to 125°C (V version) unless otherwise specified)

Table 5.59 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	62.5		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

$V_{CC1} = V_{CC2} = 5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 40 to 85°C (T version) / – 40 to 125°C (V version) unless otherwise specified)

Table 5.60 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	40		ns

Table 5.61 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	200		ns

Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 5.64 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

$V_{CC1} = V_{CC2} = 5V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -40$ to $85^{o}C$ (T version) / -40 to $125^{o}C$ (V version) unless otherwise specified)

Table 5.66 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 5.67 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.68 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.69 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW pulse width	125		ns

Table 5.70 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	30		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.71 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input LOW pulse width	250		ns

$V_{CC1} = V_{CC2} = 5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = – 40 to 85°C (T version) / – 40 to 125°C (V version) unless otherwise specified)

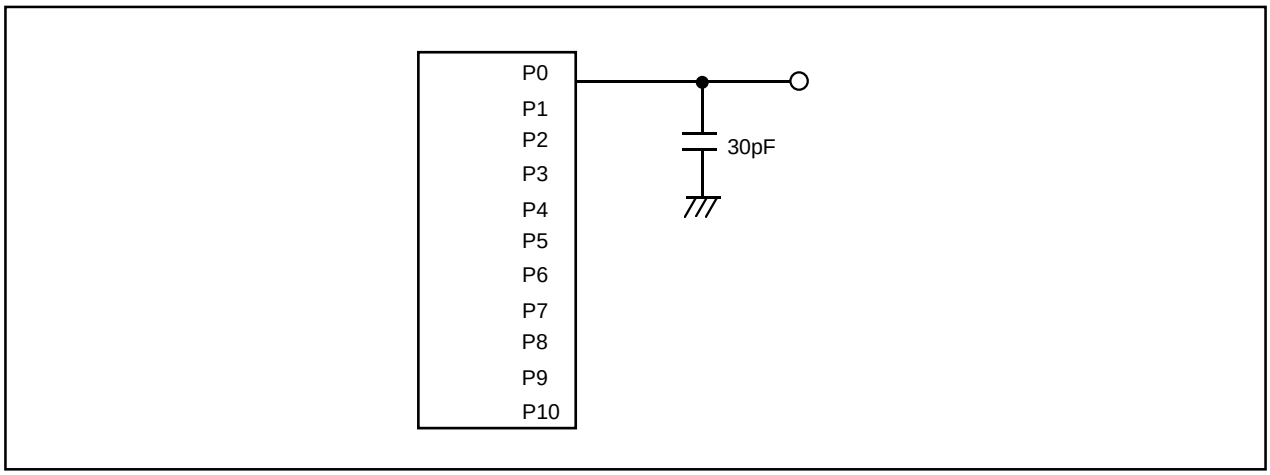


Figure 5.21 Ports P0 to P10 Measurement Circuit

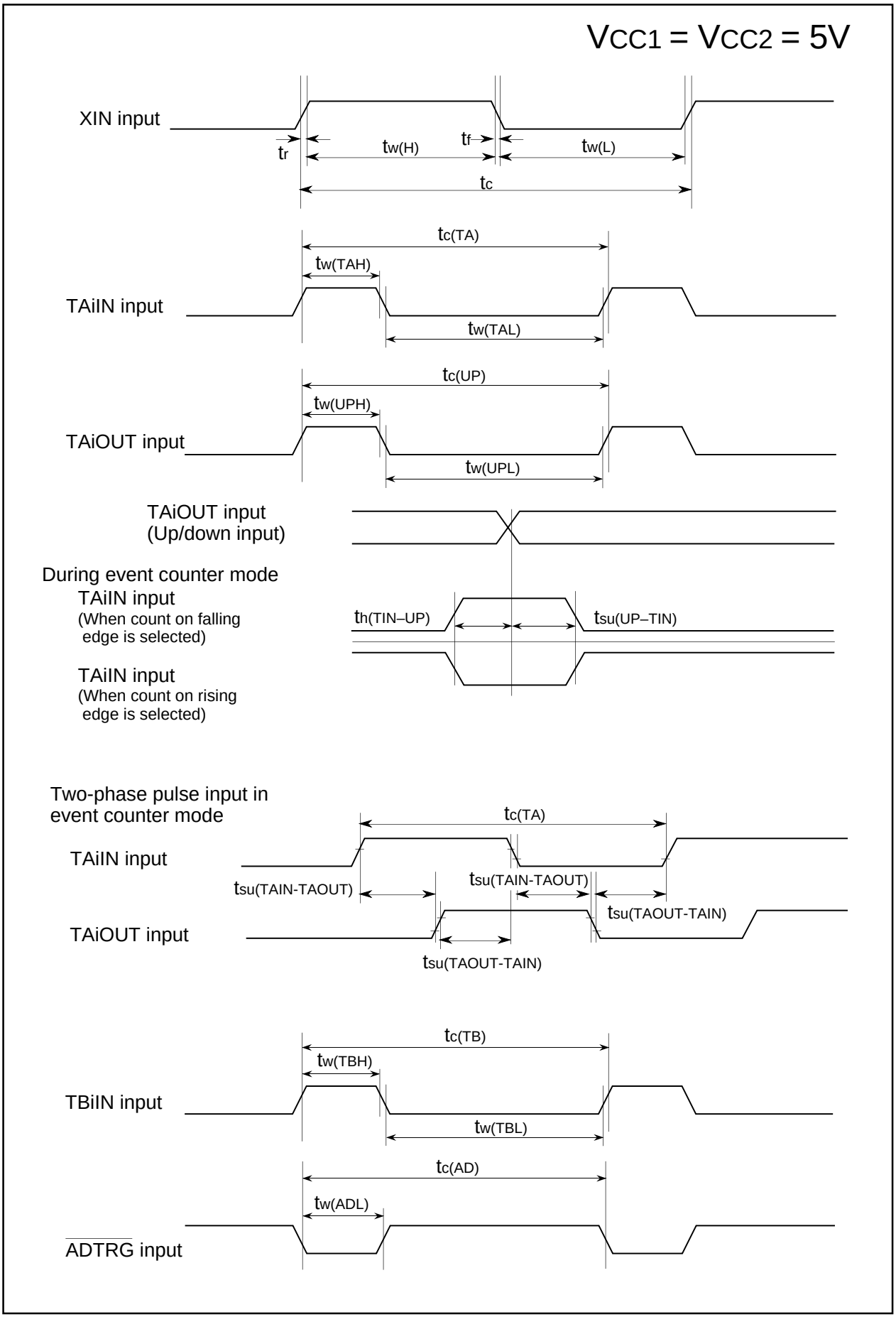


Figure 5.22 Timing Diagram (1)

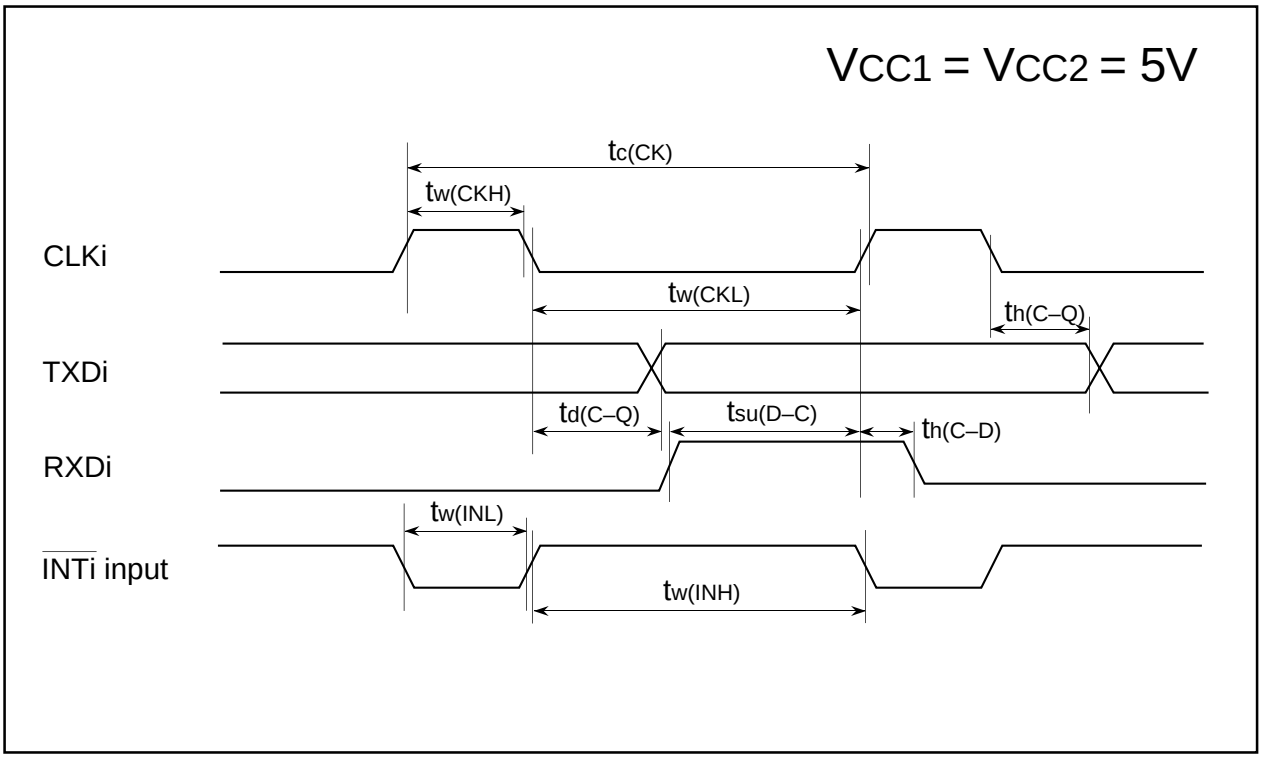


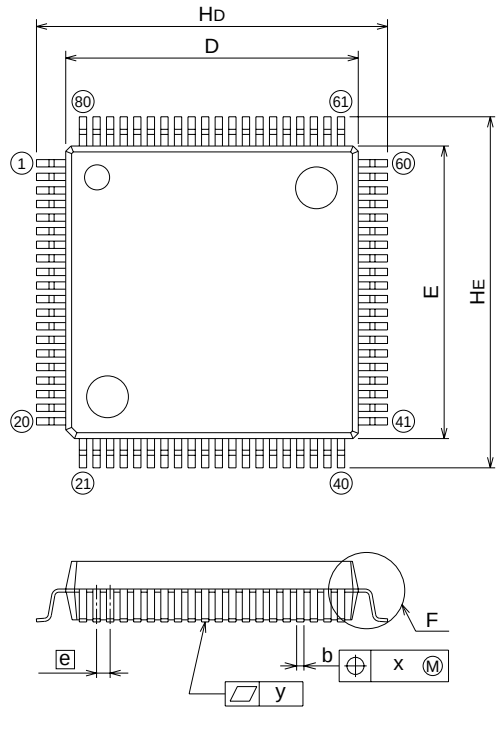
Figure 5.23 Timing Diagram (2)

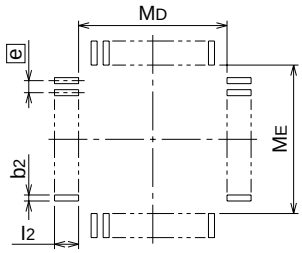
Package Dimensions

80P6S-A (MMP)

Plastic 80pin 14×14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1414-0.65		1.11	Alloy 42





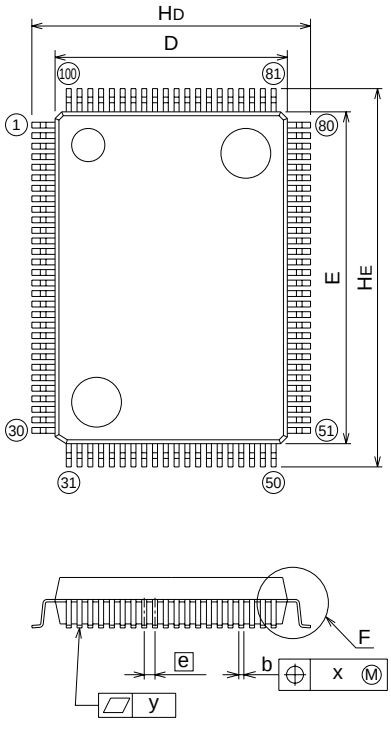
Recommended Mount Pad

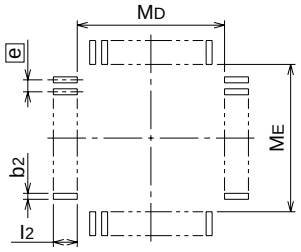
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	14.6	–

100P6S-A (MMP)

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42





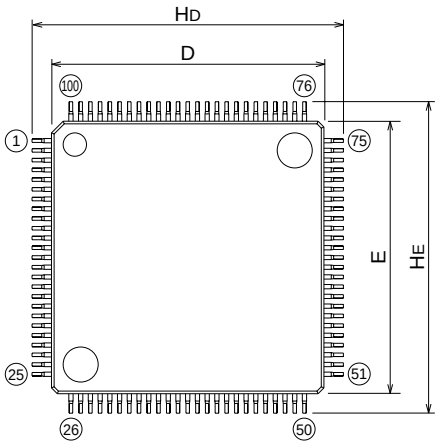
Recommended Mount Pad

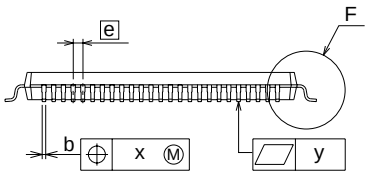
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

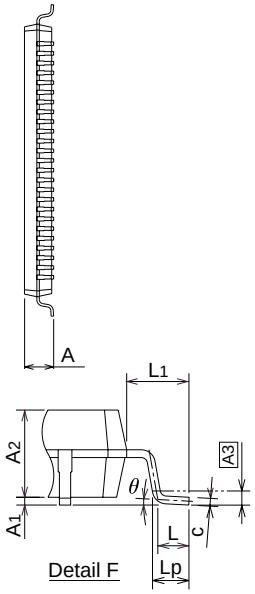
100P6Q-A (MMP)

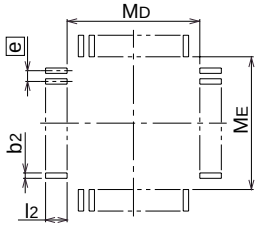
Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy









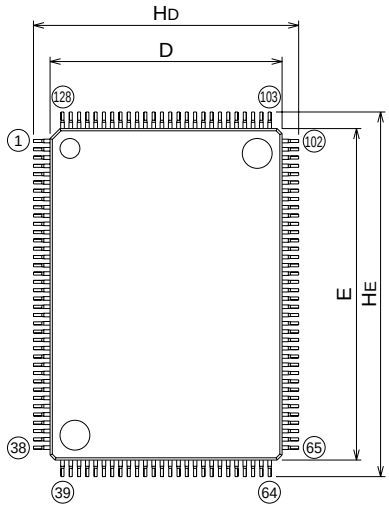
Recommended Mount Pad

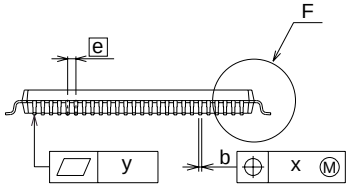
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–

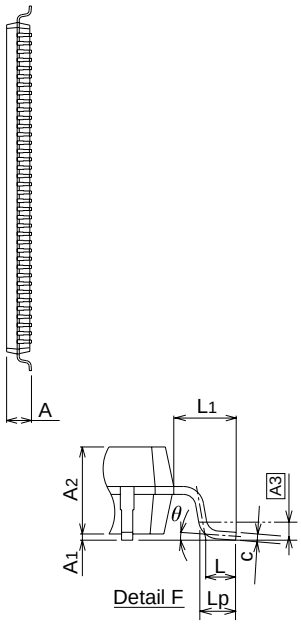
128P6Q-A (MMP)

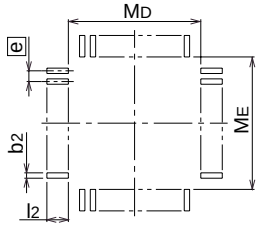
Plastic 128pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	–	–	Cu Alloy









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.4	1.5	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	–	1.0	–
MD	–	14.4	–
ME	–	20.4	–

REVISION HISTORY	M16C/62 Group (M16C/62P, M16C/62PT) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.10	May/28/Y03 (Continued)	2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised.
		14-19	SFR is partly revised.
			“Note 1” is partly revised.
		22	Table 1.5.3 is partly revised.
		23	Table 1.5.5 is partly revised.
			Table 1.5.6 is added.
		24	Table 1.5.9 is partly revised.
		30	Notes 1 and 2 in Table 1.5.26 is partly revised.
		31	Notes 1 in Table 1.5.27 is partly revised.
		30-31	Note 3 is added to “Data output hold time (refers to BCLK)” in Table 1.5.26 and 1.5.27.
		32	Note 4 is added to “th(ALE-AD)” in Table 1.5.28.
		30-32	Switching Characteristics is partly revised.
		36-39	th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised.
		40-41	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to 1.5.10 is partly revised.
		42	Note 2 is added to Table 1.5.29.
		47	Notes 1 and 2 in Table 1.5.45 is partly revised.
		48	Notes 1 in Table 1.5.46 is partly revised.
		47-48	Note 3 is added to “Data output hold time (refers to BCLK)” in Table 1.5.45 and 1.5.46.
		49	Note 4 is added to “th(ALE-AD)” in Table 1.5.47.
		47-49	Switching Characteristics is partly revised.
		53-56	th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised.
		57-58	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to 1.5.20 is partly revised.
2.00	Oct./29/Y03	-	Since high reliability version is added, a group name is revised. M16C/62 Group (M16C/62P) Æ M16C/62 Group (M16C/62P, M16C/62PT)
		2-4	Table 1.1 to 1.3 are revised. Note 3 is partly revised.
		6	Figure 1.2 Note5 is deleted.
		7-9	Table 1.4 to 1.7 Product List is partly revised.
		11	Table 1.8 and Figure 1.4 are added.
		12-15	Figure 1.5 to 1.9 ZP is added.
		17,19	Table 1.10 and 1.12 ZP is added to timer A.
		18,20	Table 1.11 and 1.13 VCC1 is added to VREF.
		30	Table 5.1 is revised.
		31-32	Table 5.2 and 5.3 are revised.
		33	Table 5.4 A-D Conversion Characteristics is revised. Table 5.5 D-A Conversion Characteristics revised.
		34,74	Table 5.6 to 5.7 and table 5.54 to 5.55 are revised.
		36	Table 5.11 is revised.
		38,55	Table 5.14 and 5.33 HLDA output deley time is deleted.
		41	Figure 5.1 is partly revised.
		41-43, 58-60	Table 5.27 to 5.29 and table 5.46 to 48 HLDA output deley time is added.
		44	Figure 5.2 Timing Diagram (1) X_{IN} input is added.

Rev.	Date	Description	
		Page	Summary
		47-48	Figure 5.5 to 5.6 Read timing DB --> DBi
		49-50	Figure 5.7 to 5.8 Write timing DB --> DBi
		52	Figure 5.10 DB --> DBi
		53	Table 5.30 is revised.
		58	Figure 5.11 is partly revised.
		61	Figure 5.12 Timing Diagram (1) X_{IN} input is added.
		64-65	Figure 5.15 to 5.16 Read timing DB --> DBi
		66-67	Figure 5.17 to 5.18 Write timing DB --> DBi
		69	Figure 5.20 DB --> DBi
		70-85	Electrical Characteristics (M16C/62PT) is added.
2.10	Nov./07/Y03	8-9	Table 1.5 to 1.7 Product List is partly revised. Note 1 is deleted.
		23	Table 3.1 is revised.
		71	Table 5.50 is revised.
		72	Table 5.51 is deleted.

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