

UTC UC3842B / 3843B LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

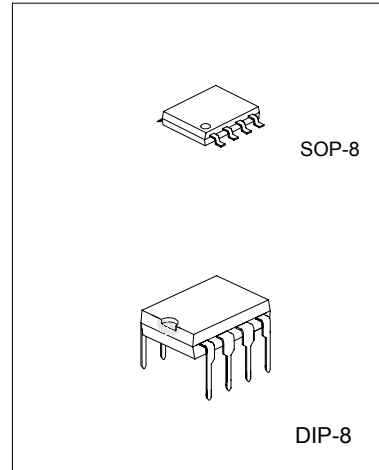
DESCRIPTION

The UTC UC3842B/3843B are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components.

The UC3842B has UVLO thresholds 16V (on) and 10V (off), ideally suited for off-line converters. The UC3843B is tailored for lower voltage applications having UVLO thresholds of 8.5V (on) and 7.6V (off).

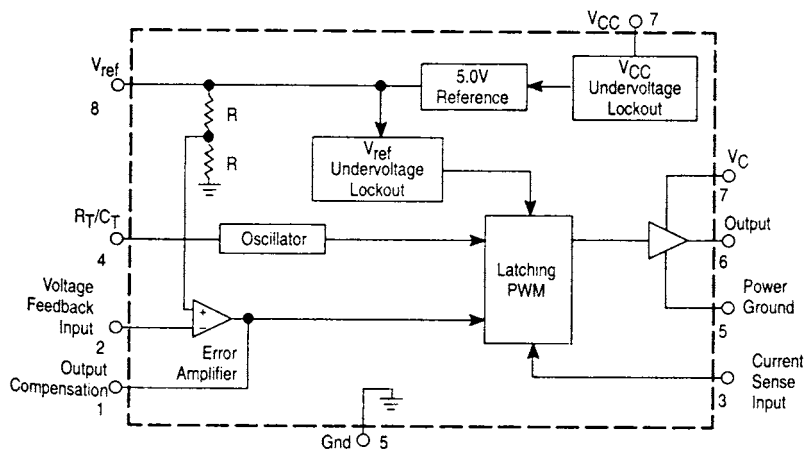
FEATURES

- *Trimmed Oscillator for Precise Frequency Control
- *Oscillator Frequency Guaranteed at 250kHz
- *Current Mode Operation to 500kHz
- *Automatic Feed Forward Compensation
- *Latching PWM for Cycle-By-Cycle Current Limiting
- *Internally Trimmed Reference with Undervoltage Lockout
- *High Current Totem Pole Output
- *Undervoltage Lockout with Hysteresis
- *Low Startup and Operating Current



BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

PARAMETER	SYMBOL	VALUE	UNIT	
Total power supply and Zener current	(ICC + I _Z)	30	mA	
Output current, source or sink (note1)	I _O	1.0	A	
Output energy (capacitive load per cycle)	W	5.0	μJ	
Current sense and voltage feedback inputs	V _{in}	-0.3 ~ +5.5	V	
Error Amp. Output sink current	I _O	10	mA	
Power dissipation and thermal characteristics	PD PθJA	DIP:1250 DIP: 100	SOP: 702 SOP: 178	mW °C/W
Operating junction temperature	T _J	+150	°C	
Operating ambient temperature	T _A	0 ~ +70	°C	
Storage temperature range	T _{stg}	-65 ~ +150	°C	

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC}=15V [note 2], R_T=10k, C_T=3.3nF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Output Voltage	V _{REF}	I _O =1.0mA, T _J =25°C	4.9	5.0	5.1	V
Line Regulation	Reg _{line}	V _{CC} =12V to 25V		2.0	20	mV
Load Regulation	Reg _{load}	I _O =1.0mA to 20mA		3.0	25	mV
Temperature Stability	T _s			0.2		mV/°C
Total Output Variation	V _{ref}	Line, Load, Temperature	4.82		5.18	V
Output Noise Voltage	V _n	F=10kHz to 10Hz, T _J =25°C		50		μV
Long Term Stability	S	T _A =125°C, 1000Hrs		5		mV
Output Short Circuit Current	I _{sc}		-30	-85	-180	mA
Oscillator Section						
Frequency		T _J =25°C T _A =0°C to 70°C T _J =25°C (R _T =6.2k, C _T =1.0nF)	49 48 225	52 250	55 56 275	kHz
Frequency Change with Voltage	Δf _{osc} /ΔV	12 ≤ V _{CC} ≤ 25V		0.2	1.0	%
Frequency Change with Temperature	Δf _{osc} /ΔT	0°C ≤ T _A ≤ 70°C		0.5		%
Oscillator Voltage Swing (Peak to Peak)	V _{OSC}			1.6		V
Discharge Current	I _{dischg}	T _J =25°C 0°C ≤ T _A ≤ 70°C	7.8 7.6	8.3	8.8 8.8	mA
Error Amplifier Section						
Voltage Feedback Input	V _{FB}	V _O =2.5V	2.42	2.50	2.58	V
Input Bias Current	I _{IB}	V _{FB} =5.0V		-0.1	-2.0	μA
Open Loop Voltage Gain	AVOL	2 ≤ V _O ≤ 4V	65	90		dB
Unity Gain Bandwidth	BW	T _J =25°C	0.7	1.0		MHz
Power Supply Rejection Ratio	PSRR	12V ≤ V _{CC} ≤ 25V	60	70		dB
Output Sink Current	I _{sink}	V _O =1.1V, V _{FB} =2.7V	2.0	12		mA
Output Source Current	I _{source}	V _O =5.0V, V _{FB} =2.3V	-0.5	-1.0		mA
Output Voltage Swing High State	V _{OH}	V _{FB} =2.3V, R _L =15k to GND	5.0	6.2		V
Output Voltage Swing Low State	V _{OL}	V _{FB} =2.7V, R _L =15k to V _{ref}		0.8	1.1	V
Current Sense section						
Current Sense Input Voltage Gain	A _v	(note 3,4)	2.85	3.0	3.15	V/V

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Current Sense Input Threshold	V _{th}	(note 3)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	12<=V _{cc} <=25V (note 3)		70		dB
Input Bias Current	I _{IB}			-2	-10	μA
Propagation Delay	t _{PLH(In/Out)}	Current Sense Input to Output		150	300	ns
Output Section						
Output Low Voltage	V _{OL}	I _{sink} =20mA		0.1	0.4	V
		I _{sink} =200mA		1.6	2.2	V
Output High Level	V _{OH}	I _{source} =20mA	13	13.5		V
		I _{source} =200mA	12	13.4		V
Output Voltage with UVLO Activated	V _{OL (UVLO)}	V _{cc} =6.0V, I _{sink} =1.0mA		0.1	1.1	V
Output Voltage Rise Time	t _r	T _j =25°C, C _L =1nF		50	150	ns
Output Voltage Fall Time	t _f	T _j =25°C, C _L =1nF		50	150	ns
Under-Voltage Lockout Section						
Startup Threshold	V _{th}	UTC UC3842B	14.5	16	17.5	V
		UTC UC3843B	7.8	8.4	9	V
Min. Operating Voltage After Turn-on(V _{cc})	V _{CC(min)}	UTC3842B	8.5	10	11.5	V
		UTC3843B	7.0	7.6	8.2	V
PWM Section						
Maximum Duty Cycle	DC(MAX)		94	96		%
Minimum Duty Cycle	DC(MIN)				0	%
Total Device						
Power Startup Supply Current	I _{cc+Ic}	V _{cc} =6.5V for UC3843B V _{cc} =14V for UC3842B		0.3	0.5	mA
Power Operating Supply Current	I _{cc+Ic}	Note2		12	17	mA
Power Supply Zener Voltage	V _z	I _{cc} =25mA	30	36		V

Note 1: Maximum Package power dissipation limits must be observed.

Note 2: Adjust V_{cc} above the Startup threshold before setting to 15V.

Note 3: This parameter is measured at the latch trip point with V_{FB}=0V.

Note 4: Comparator gain is defined as :

$$AV = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$$

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TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1. Timing Resistor versus Oscillator Frequency

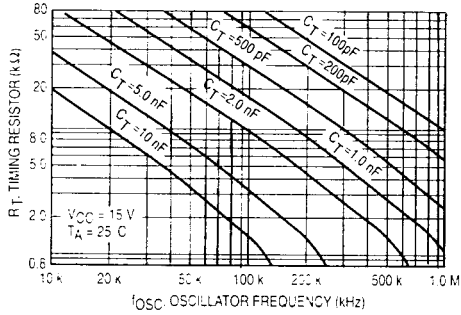


Figure 2. Output Deadtime versus Oscillator Frequency

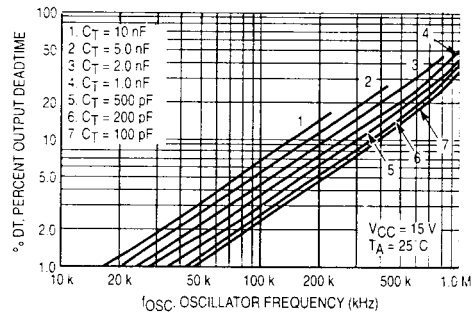


Figure 3. Oscillator Discharge Current versus Temperature

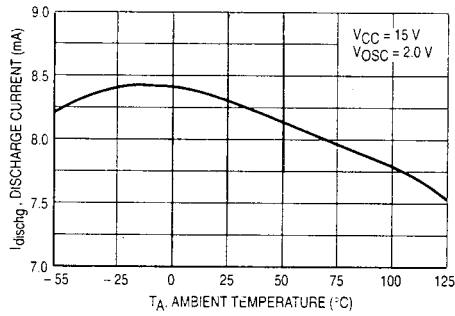
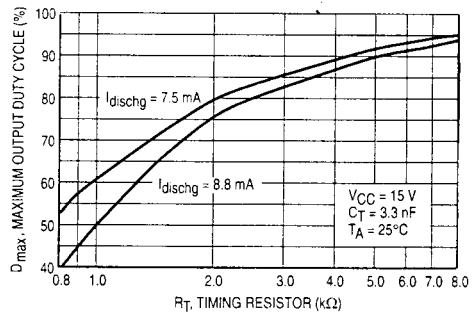


Figure 4. Maximum Output Duty Cycle versus Timing Resistor



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Figure 5. Error Amp Small Signal Transient Response

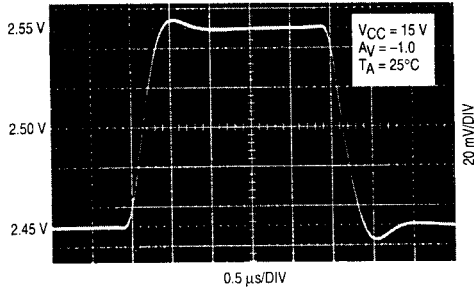


Figure 6. Error Amp Large Signal Transient Response

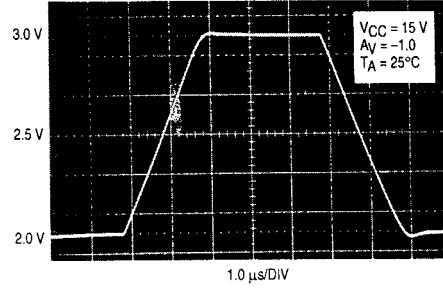


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

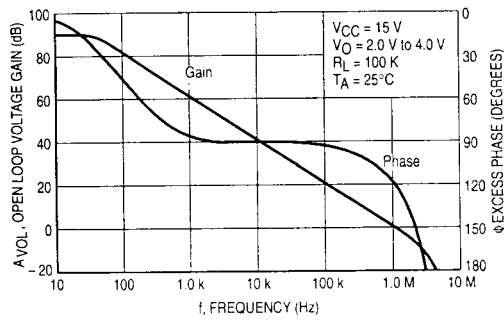


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

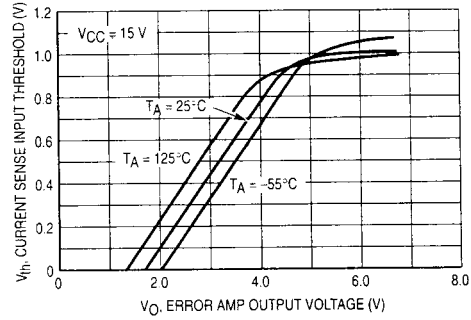


Figure 9. Reference Voltage Change versus Source Current

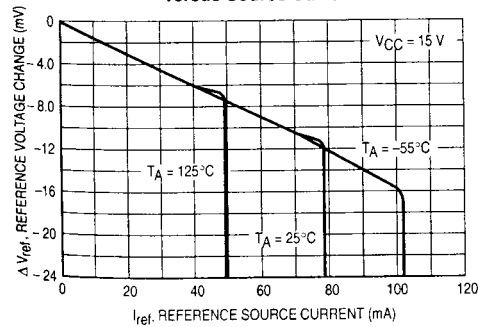
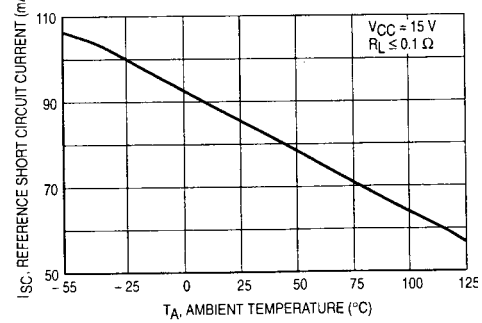


Figure 10. Reference Short Circuit Current versus Temperature



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Figure 11. Reference Load Regulation

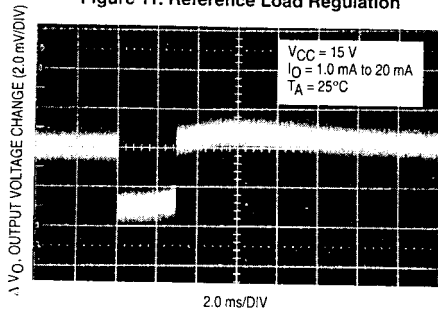


Figure 12. Reference Line Regulation

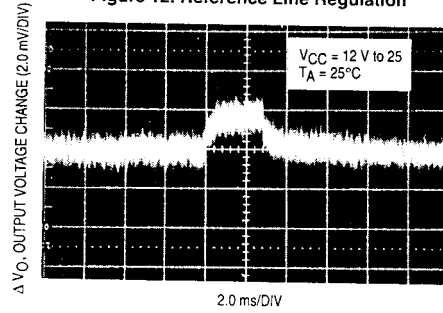


Figure 13. Output Saturation Voltage versus Load Current

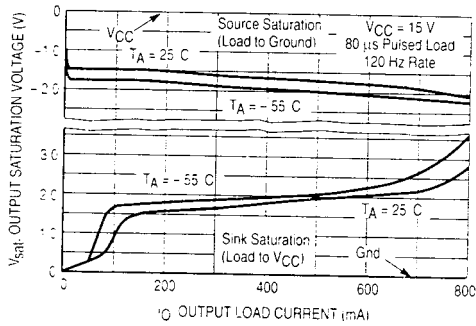


Figure 14. Output Waveform

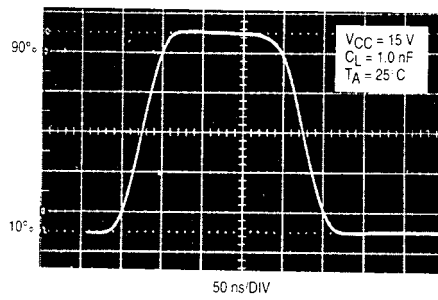


Figure 15. Output Cross Conduction

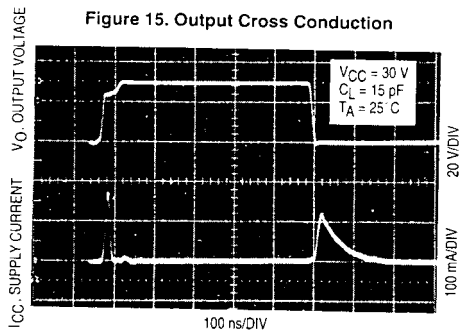
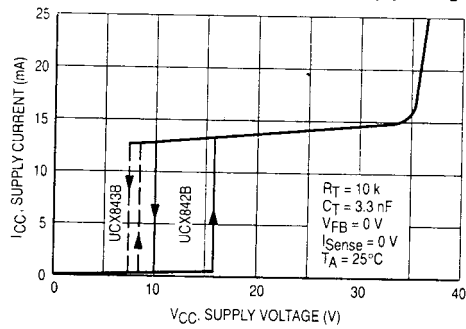


Figure 16. Supply Current versus Supply Voltage



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