



# LCD Module Technical Specification

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Final Revision  
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T-51378L025J-FW-P-AB

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## Revision History

Rev.	Date	Page	Comment

## 1. Application

This technical specification applies to 2.5" color TFT-LCD panel. The 2.5" color TFT LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays.

## 2. Features

- . Compatible with NTSC or PAL system
- . High Resolution : 112,320 Dots
- . Optimum Viewing Direction : 6 o'clock
- . Up/Down and Left/Right Image Reversion

## 3. Mechanical Specifications

<b>Parameter</b>	<b>Specifications</b>	<b>Unit</b>
Screen Size	2.5 (diagonal)	inch
Surface Treatment	Anti-Glare	
Display Format	480×234	dot
Active Area	50.21×37.67	mm
Dot Pitch	0.105(W)×0.161(H)	mm
Pixel Configuration	Delta	
Outline Dimension	61.6 (W)×49.3 (H)×5.9 (D)	mm
Weight	TBD±3	g



## 5. Input / Output Terminals

Pin No	Symbol	I/O	Description	Remark
1	STH1	I/O	Start pulse for source driver	Note 5-1
2	AV <sub>SS</sub>	I	Analog GND for source driver	
3	AV <sub>DD</sub>	I	Analog power input for source driver	Note 5-2
4	V <sub>B</sub>	I	Video Input B	Note 5-4
5	V <sub>G</sub>	I	Video Input G	
6	V <sub>R</sub>	I	Video Input R	
7	V <sub>SS</sub>	I	Digital GND	
8	V <sub>DD</sub>	I	Digital power input	Note 5-3
9	CPH1	I	Sampling and shift clock for source driver	
10	CPH2	I	Sampling and shift clock for source driver	
11	CPH3	I	Sampling and shift clock for source driver	
12	STH2	I/O	Start pulse for source driver	Note 5-1
13	Q2H	I	Video input rotation control	
14	INH	I	Output enable for source driver	
15	R/L	I	Left/Right Control for source driver	Note 5-1
16	V <sub>COM</sub>	I	Common electrode voltage	Note 5-4
17	V <sub>COM</sub>	I	Common electrode voltage	
18	XOE	I	Output enable for gate driver	
19	CPV	I	Clock input for gate driver	
20	U/D	I	Up/Down Control for gate driver	
21	DIO2	I/O	Vertical start pulse	Note 5-5
22	DIO1	I/O	Vertical start pulse	
23	V <sub>GL</sub>	I	Gate off voltage(alternative every 1-H)	Note 5-4
24	V <sub>EE</sub>	I	Gate driver negative voltage	Note 5-6
25	V <sub>SS</sub>	I	GND	
26	V <sub>CC</sub>	I	Logic power for gate driver	Note 5-3
27	V <sub>GH</sub>	I	Gate on voltage	Note 5-7
28	NC	-	No connection	-

Note 5-1 : STH1, STH2 and R/L mode

R/L	STH1	STH2	Remark
High(VDD)	Input	Output	Left to Right
Low(0 Volt.)	Output	Input	Right to Left

Note 5-2 : AV<sub>DD</sub> = +5V (Typ.)

Note 5-3 : V<sub>DD</sub>, V<sub>CC</sub> = +5V or +3.3V (Typ.)

Note 5-4 : V<sub>COM</sub> = 6V<sub>PP</sub>.

Phase of the video signal input and  $V_{COM}$

The relation between these values could refer to 8-1 Operating condition.

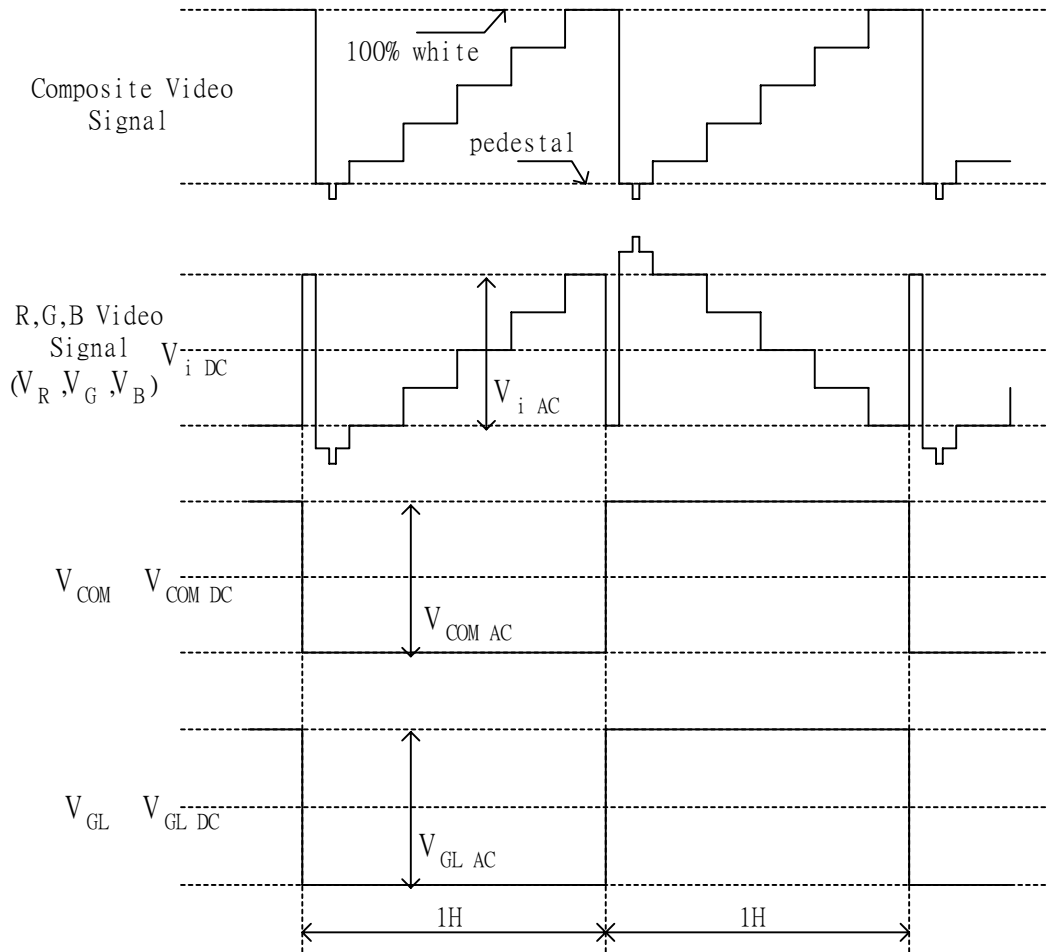


Fig.1

Liquid crystal transmission of the video signal input,  $V_{COM}$  and timing

	$V_{COM}$	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

White : maximum transmission / Black : minimum transmission

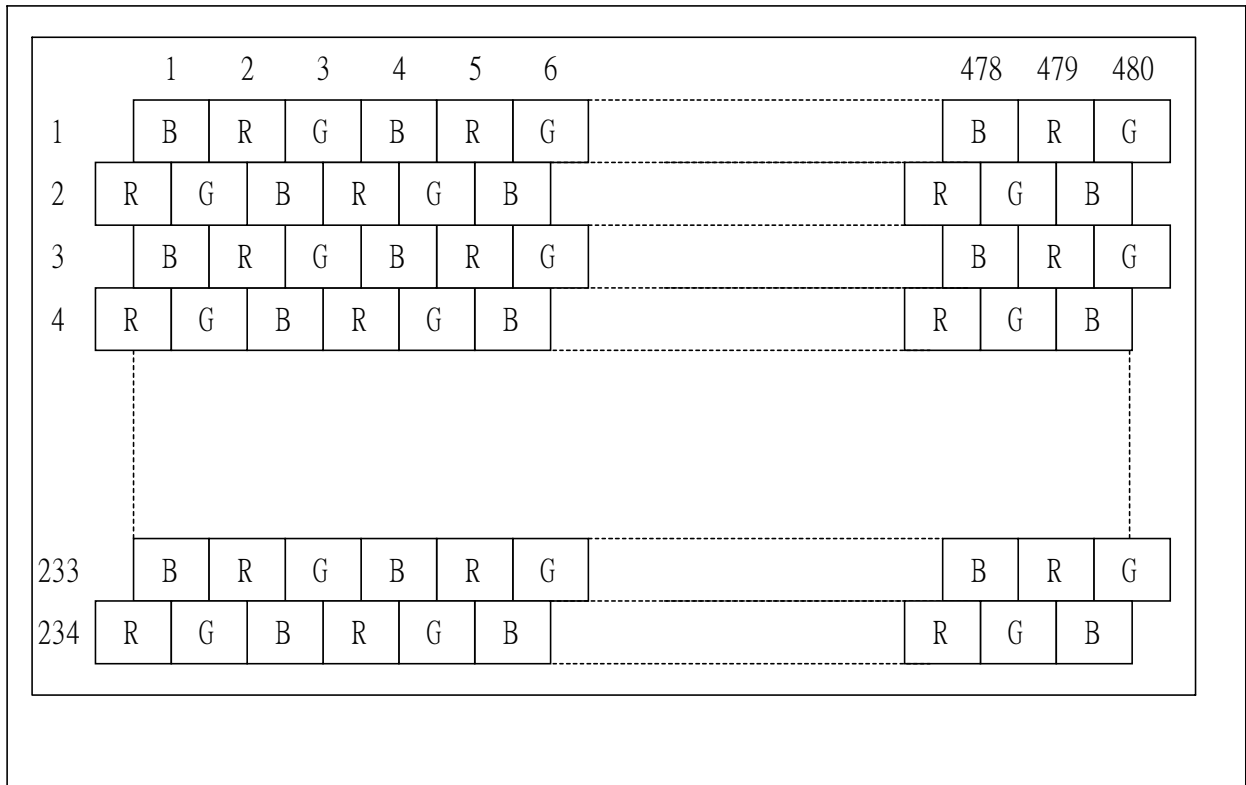
Note 5-5 : DIO1, DIO2 and U/D mode

U/D	DIO1	DIO2	Remark
High (VDD)	Input	Output	Down to Up
Low (0 Volt.)	Output	Input	Up to Down

Note 5-6 :  $V_{EE} = -15V$  (Typ.).

Note 5-7 :  $V_{GH} = +15V$  (Typ.).

## 6. Pixel Arrangement and input connector pin NO.



1 28

## 7. Absolute Maximum Ratings:

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V · Ta = 25

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver	Analog	AV <sub>DD</sub>	-0.3	+7	V	
	Digital	V <sub>DD</sub>	-0.3	+7		
Supply Voltage for Gate Driver	Positive	V <sub>GH</sub>	-0.3	+45	V	
	Negative	V <sub>GL</sub>	-23	+0.3	V	
		V <sub>GH</sub> V <sub>GL</sub>	+15	+40	V	
Analog input voltage	V <sub>Video</sub>		-0.3	+7.3	V	Notes:7-1
Storage Temperature			-20	+70	°C	
Operation Temperature			0	+60	°C	Notes:7-2

Notes 7-1 : Analog Input Voltage means V<sub>R</sub>,V<sub>G</sub>,V<sub>B</sub>.

Notes 7-2 : Operating Temperature define that contrast, response time, other display optical character are Ta=+25.

## 8. Electrical Characteristics

### 8-1) Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Remark	
Power Supply	$V_{CC}$	+3.0	+3.3	+3.6	V	3.3V Operating	
	$V_{DD}$	+4.5	+5.0	+5.5	V	5.0V Operating	
	$AV_{DD}$	+4.5	+5.0	+5.5	V		
	$V_{GH}$	+14.5	+15.0	+15.5	V		
	$V_{EE}$	-14.5	-15.0	-15.5	V		
	$V_{GL AC}$	-	+6.0	-	$V_{P-P}$	AC Component of $V_{GL}$	
	$V_{GL DC}$	-11.5	-12.0	-12.5	V	DC Component of $V_{GL}$	
Video Signal ( $V_R, V_G, V_B$ )	$V_{i AC}$	-	+4.0	+4.6	$V_{P-P}$	AC Component	
	$V_{i DC}$	-	+2.5	-	V	DC Component	
$V_{COM}$	$V_{COM AC}$	-	+6.0	-	$V_{P-P}$	AC Component of $V_{COM}$	
	$V_{COM DC}$	+0.9	+1.0	+1.1	V	DC Component of $V_{COM}$	
	H Level	$V_{IH}$	+0.7 $V_{DD}$	-	-	V	Note 8-1
	L Level	$V_{IL}$	-	-	+0.3 $V_{DD}$	V	

Note 8-1 : STH1,STH2,CPH1,CPH2,CPH3,Q2H,INH,CPV,XOE,DIO1,DIO2

### 8-2) Current Consumption (GND= $AV_{SS}$ =0V)

$T_a = 25$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Driver	$I_{GH}$	$V_{GH}=+15V$	TBD	TBD	TBD	mA	
	$I_{GL}$	$V_{GL}=-12V$	TBD	TBD	TBD	mA	$V_{GL}$ center voltage
	$I_{CC}, I_{DD}$	$V_{CC}, V_{DD}=+5V$	TBD	TBD	TBD	mA	
	$I_{ADD}$	$AV_{DD}=+5V$	TBD	TBD	TBD	mA	

### 8-3) Backlight driving & Power Consumption

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
3	VL2	Input terminal (Low voltage side)	Note 8-2

Note 8-2 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

### Power Consumption

$T_a = 25^\circ C$

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
LCD Panel Power Consumption			TBD		W	Note 8-4

#### 8-4) Input / Output Connector

A) LCD Module Connector  
 FFC Down Connector,  
 28 Pins  
 Pitch : 0.5 mm

#### 8-5) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
1Field Scanning Period	t1V	-	262.5	-	H	
1Line Scanning Period	t1H	-	63.5	-	μs	
Source Driver Operating Frequency	fhc	1.0	3.14	5.0	MHz	
Signal Sampling Pulse Width	tchw	200	317.7	1000	ns	
Signal Sampling Pulse Delay	tchd	95.3	105.9	116.5	ns	tchd 12,23
Signal Sampling Pulse Width(H)	tchwh	142.9	158.8	174.7	ns	
Signal Sampling Pulse Delay(L)	tchwl	142.9	158.8	174.7	ns	
Source Start Signal Pulse Width	tshw	90	317.7	630*	ns	*tshset=tshhld
Source Start Signal Setup Time	tshset	20	158.8	-	ns	
Source Start Signal Hold Time	tshhld	20	158.8	-	ns	
Source Output Enable Pulse Width	tohw	1.0	2.0	-	μs	
Source Start Signal Rising Time	tss	-	9.8	-	μs	
Video Input Signal Start Point	tvS	-	10.0	-	μs	
Phase Difference Between OEH&CPV	toc	1.5	2.3	-	μs	
Gate Clock Period	tcvw	10	63.5	-	μs	
Gate Clock Pulse Width(H)	tcvwh	10	31.7	48	μs	
Gate Clock Pulse Width(L)	tcvwl	10	31.7	48	μs	
Gate Start Signal Pulse Width	tsvw	5	63.5	126**	μs	**tsvset=tsvhld
Gate Start Signal Setup Time	tsvset	5	53.2	-	μs	
Gate Start Signal Hold Time	tsvhld	5	10.3	-	μs	
Phase Difference Between OEH&STH	tosp	-	4	-	μs	
Phase Difference Between	tohs	-	1.4	-	μs	
Gate Output Enable Pulse Width	toev	-	2.5	-	μs	
V <sub>COM</sub> Delay Time	t <sub>DCOM</sub>	-	-	3	μs	
RGB Delay Time	t <sub>DRGB</sub>	-	-	2	μs	
Vertical Display Start	tSV	-	3	-	tH	



8-6) Signal Timing Waveforms

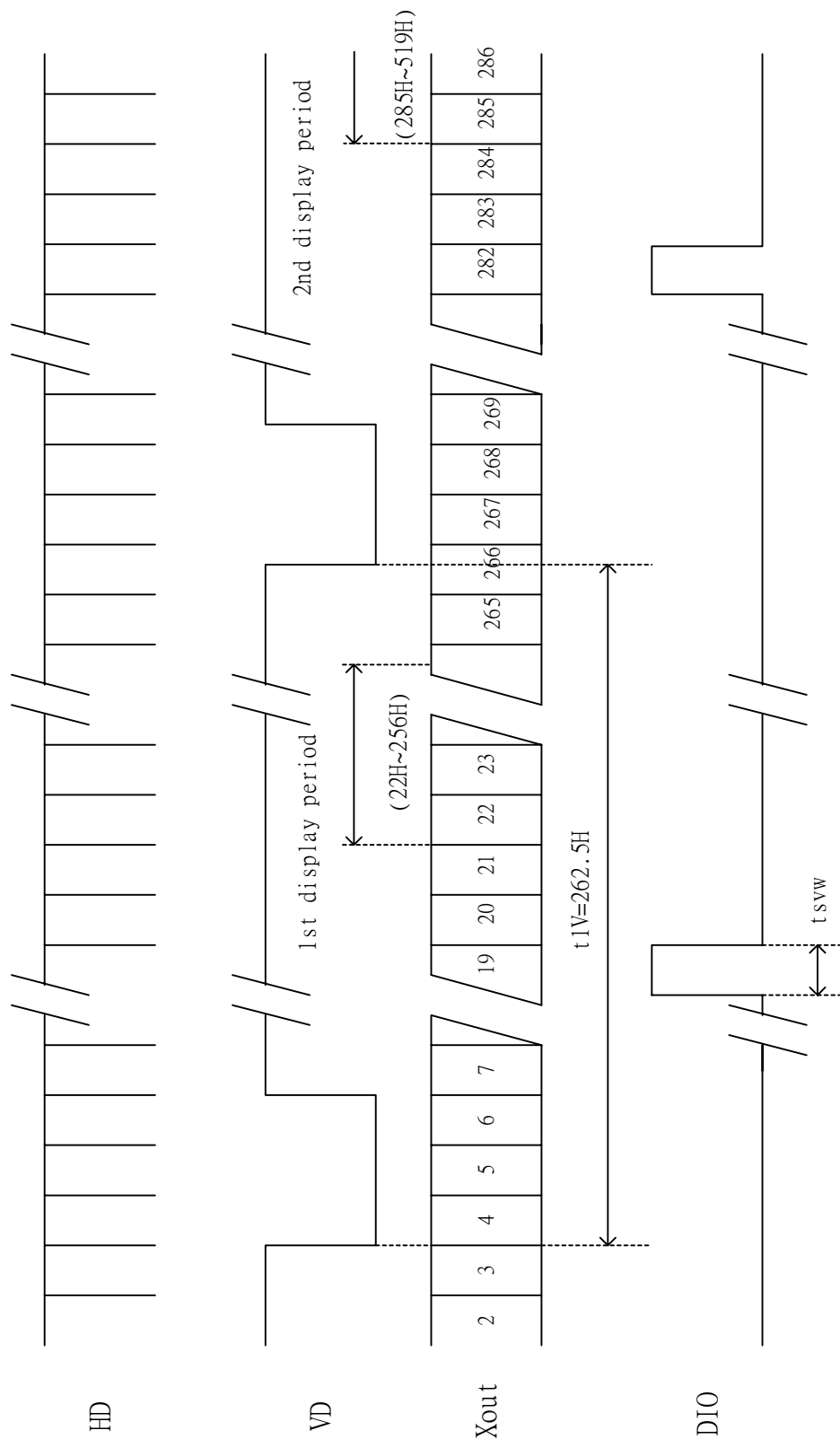
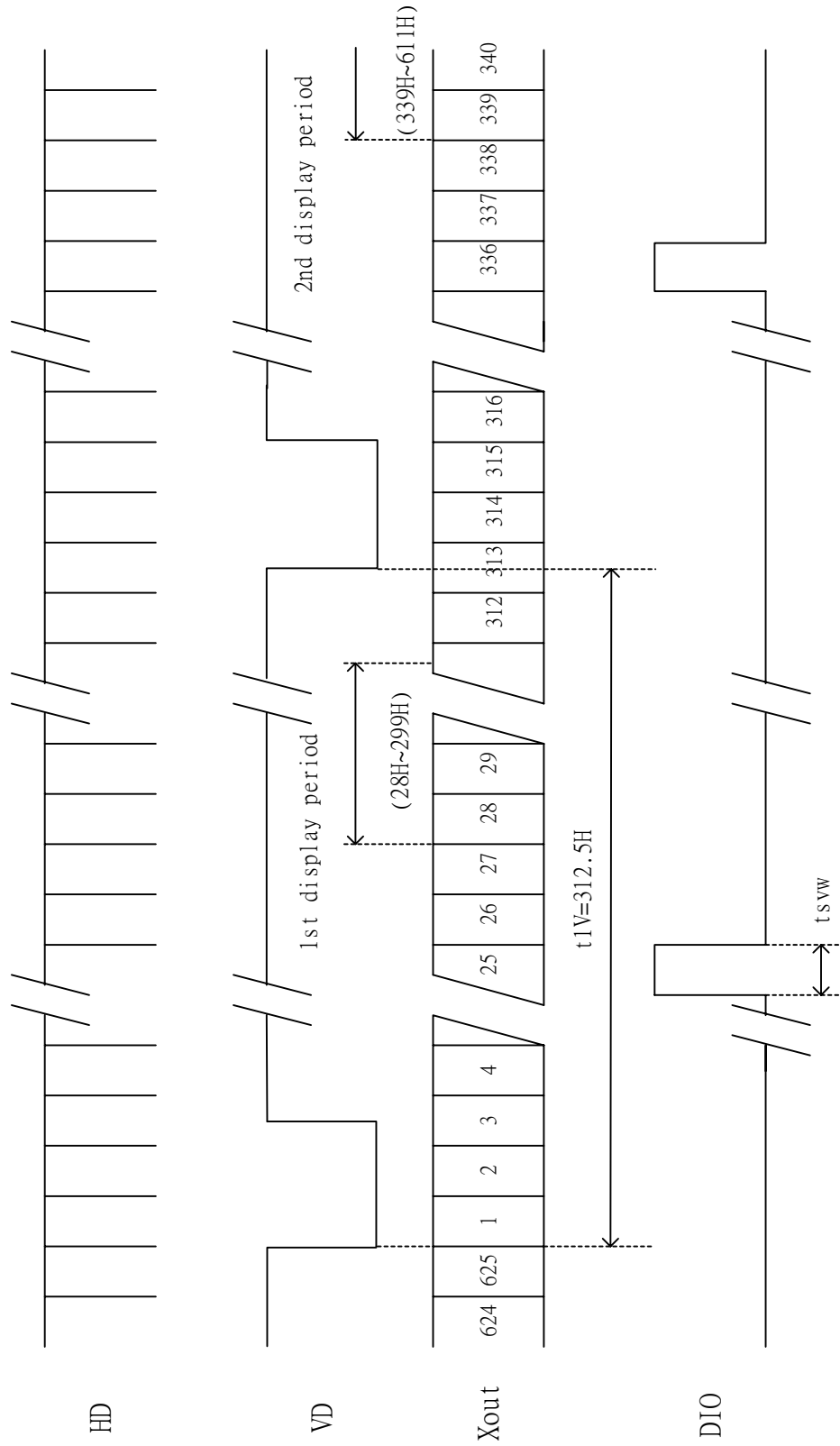


Fig. 8-1 Vertical Start Line for NTSC



\*\* odd field : Scan lines  $14n+6$   $14n+12$  ( $n = 2, 3, 4..$ ) are not displayed.  
 even field : Scan lines  $14n+12$   $14n+20$  ( $n = 2, 3, 4..$ ) are not displayed.

Fig. 8-1 Vertical Start Line for PAL

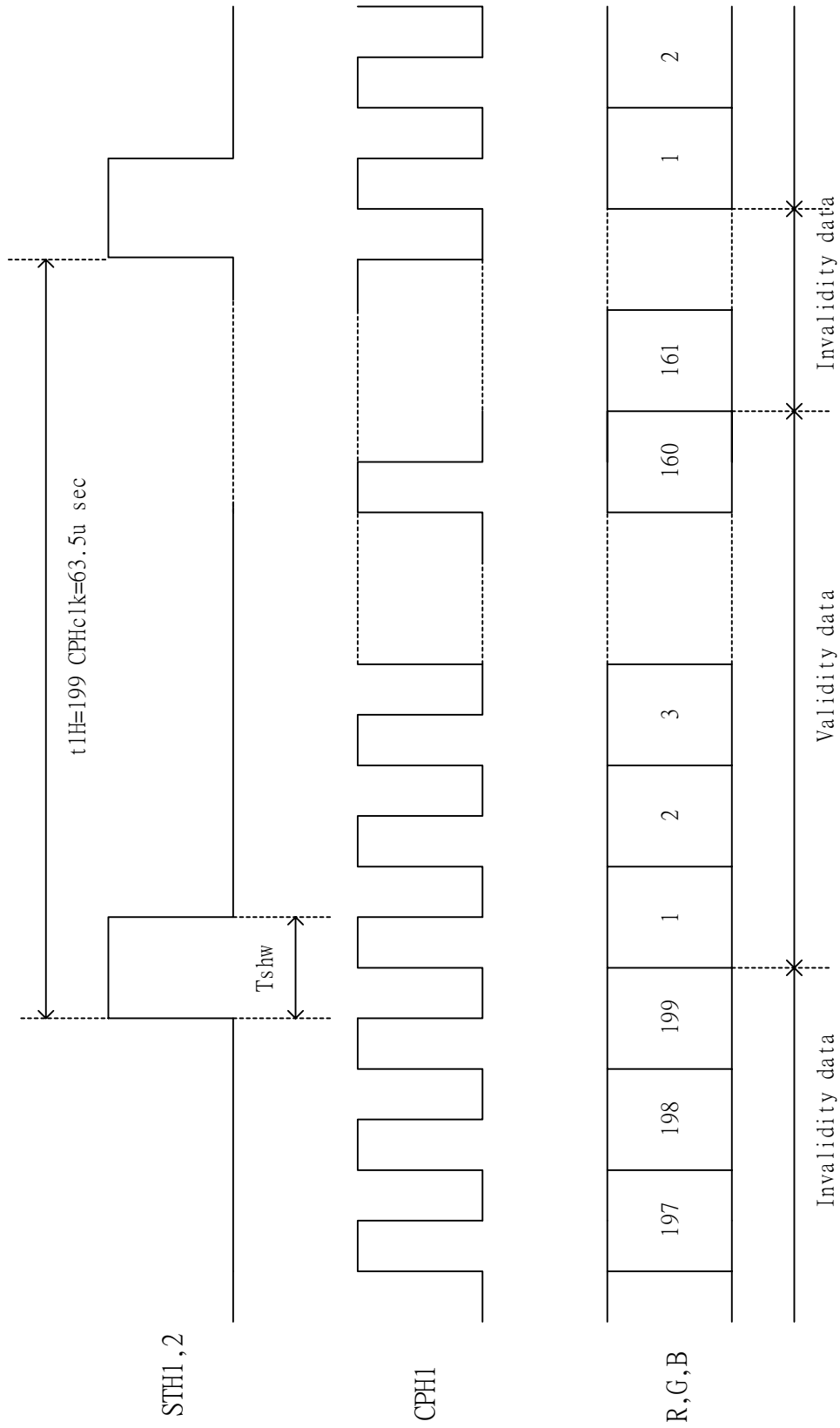


Fig. 8-2 Horizontal Start Pixel

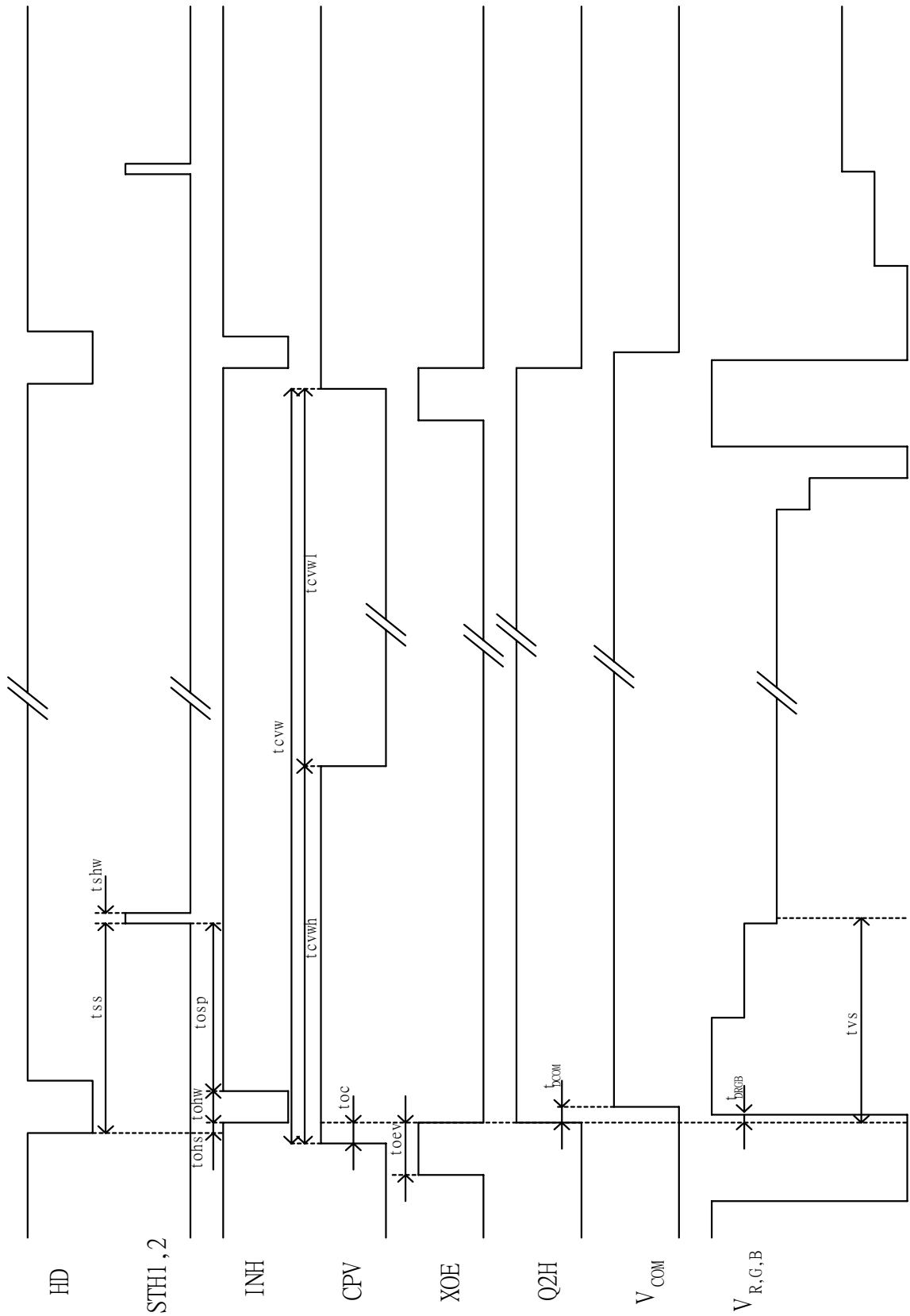


Fig. 8-3 Detail Horizontal Timing

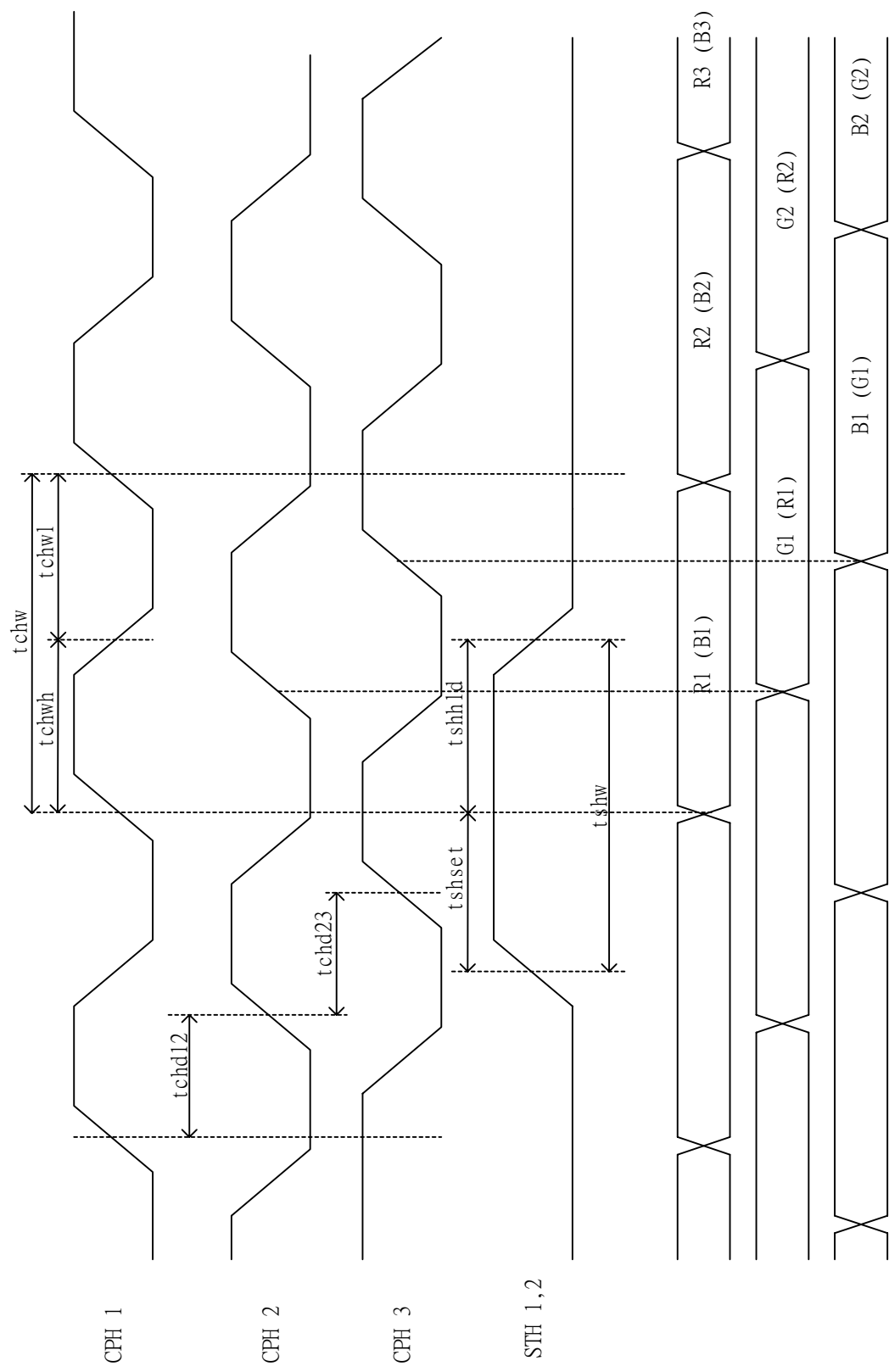


Fig. 8-4 Sampling Clock Timing

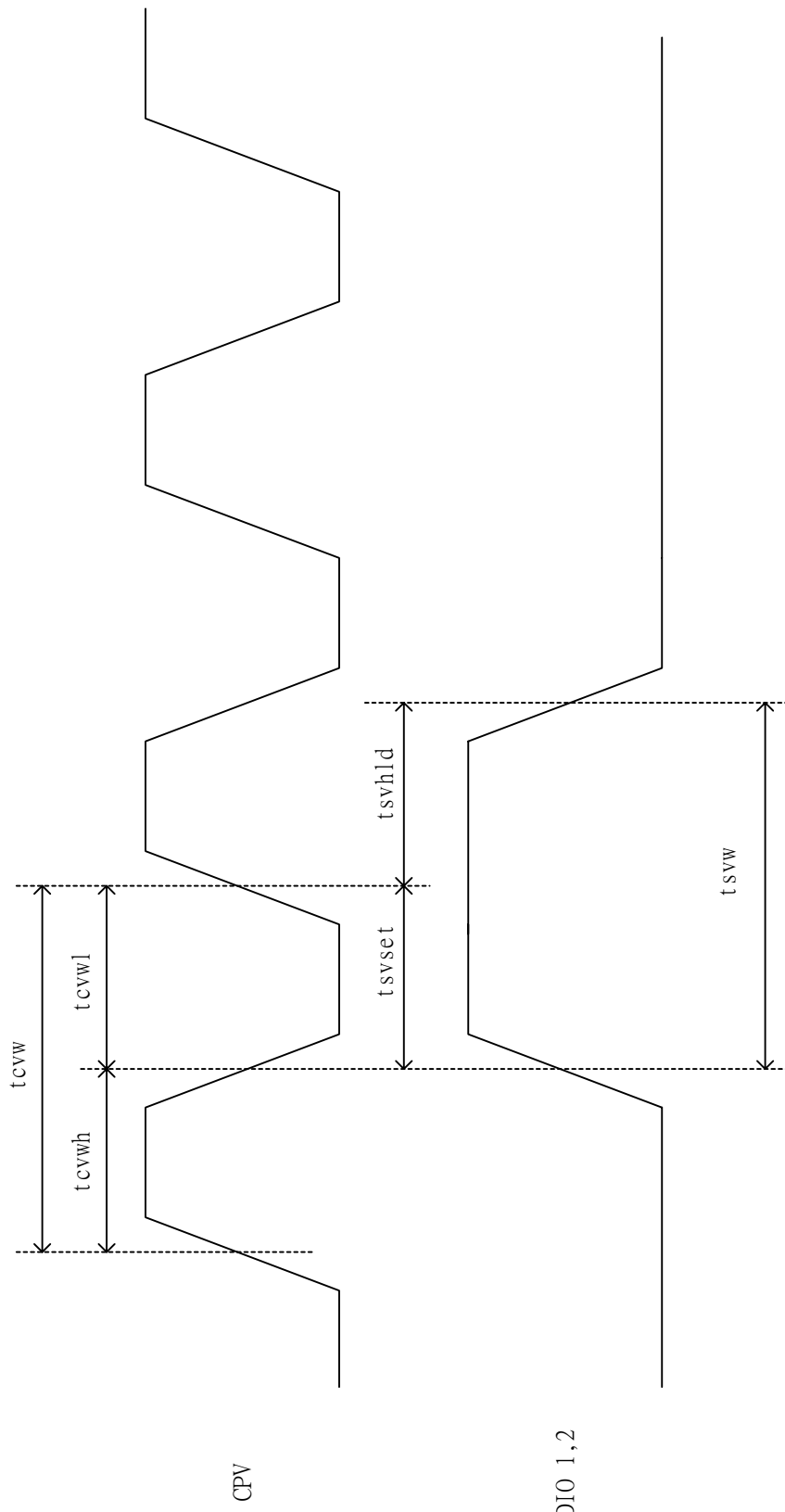


Fig. 8-5 Vertical Shift Clock Timing

Vertical timing (From up to down)

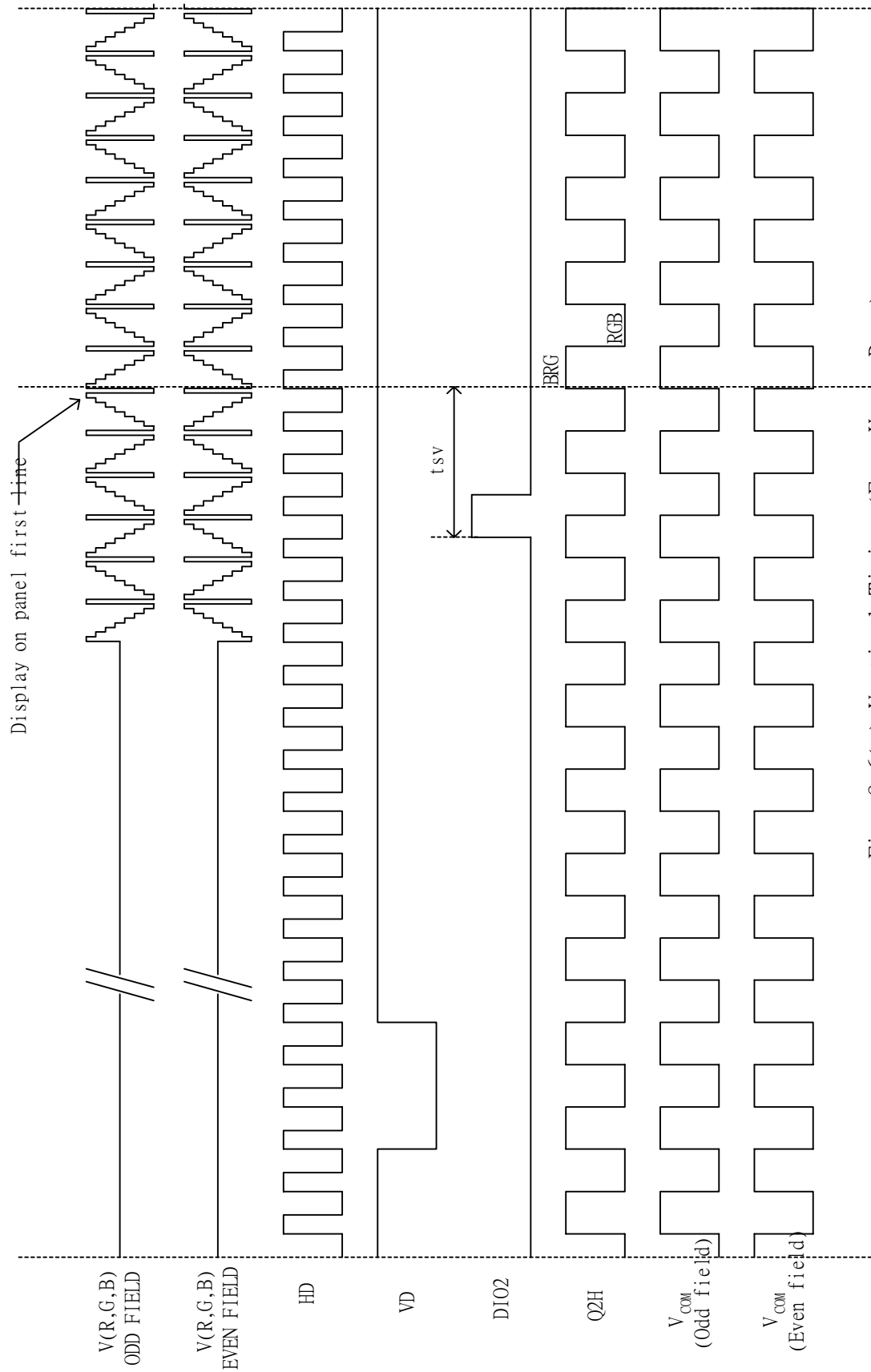


Fig. 8-6(a) Vertical Timing (From Up to Down)

Vertical timing (From down to up)

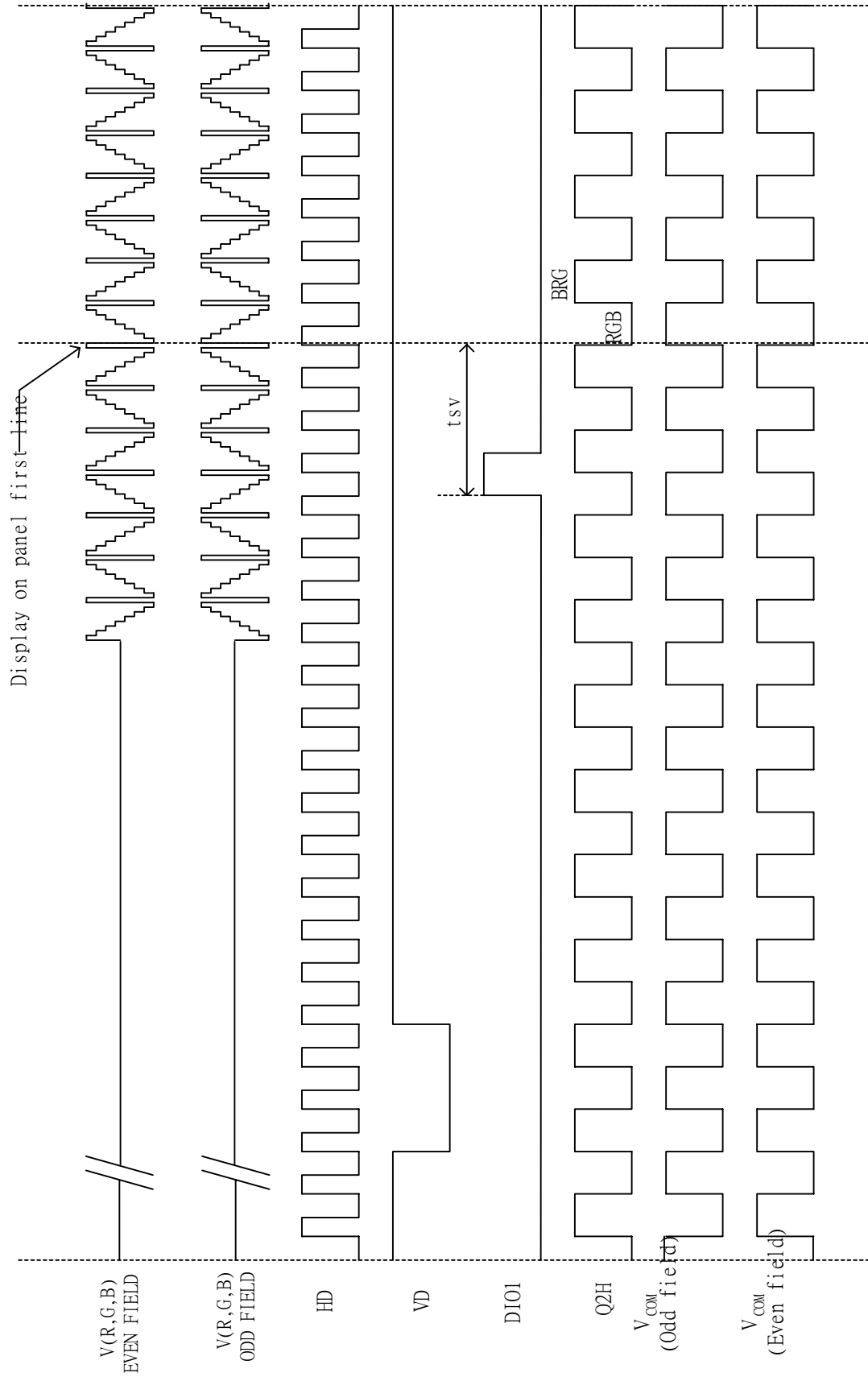
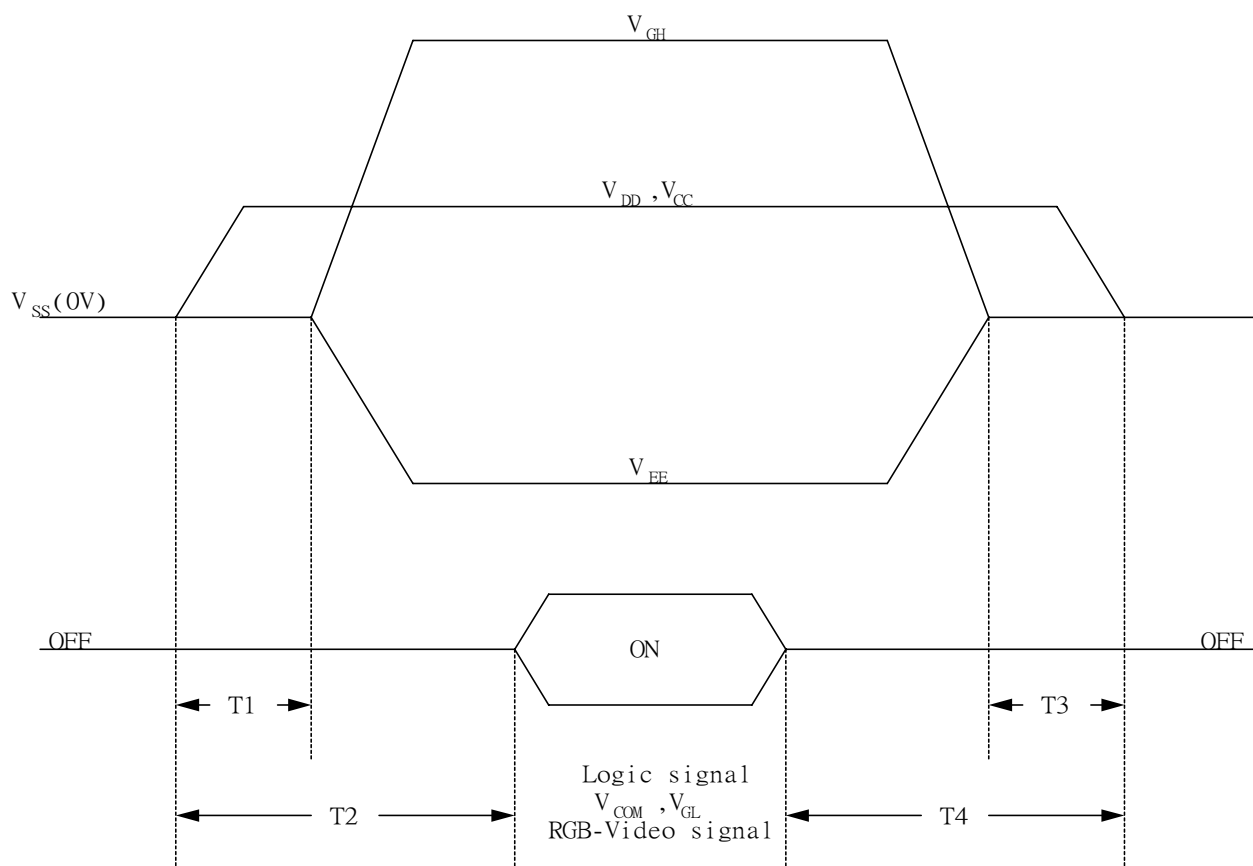


Fig. 8-6(b) Vertical Timing (From Down to Up)



### 9. Power on Sequence(Voltage source)

The Power on Sequence only effect by  $V_{CC}$ ,  $V_{SS}$ ,  $V_{DD}$ ,  $V_{EE}$  and  $V_{GH}$ , the others do not care.



- 1)  $10\text{ms} \leq T1 < T2$
- 2)  $0\text{ms} < T3 \leq T4 \leq 10\text{ms}$

### 10. Optical Characteristics

#### 10-1) Specification

$T_a = 25$

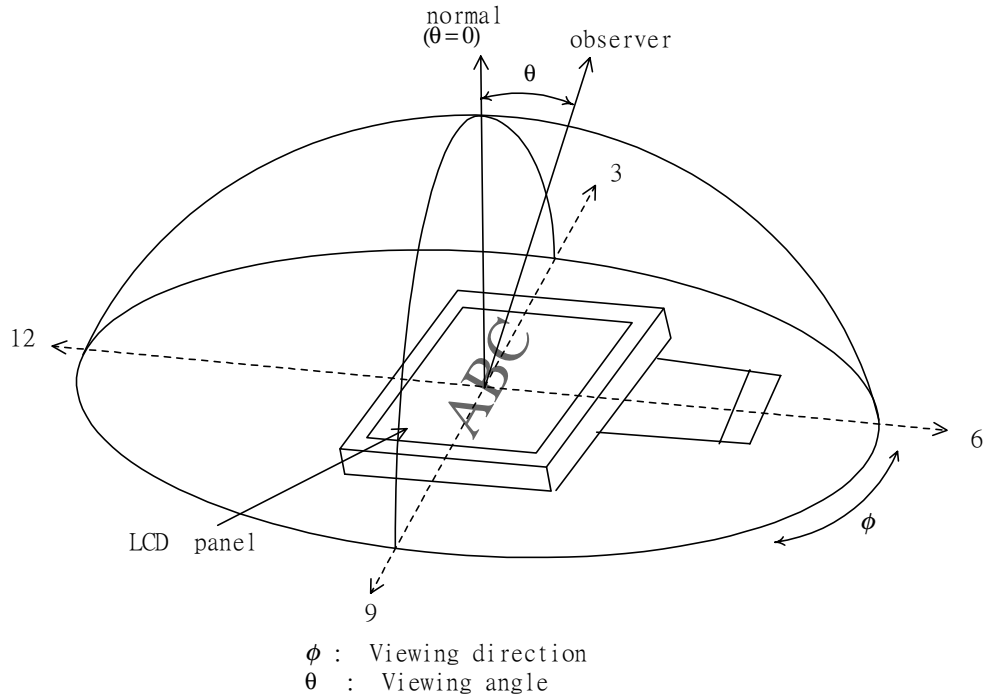
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
Viewing Angle	Horizontal	$CR \geq 10$	$\pm 45$	$\pm 50$		deg	Note 10-3	
	Vertical		(to 12 o'clock)	10	15			deg
			(to 6 o'clock)	30	35			deg
Contrast Ratio	CR		110	150			Note 10-1	
Response time	Rise	$\theta = 0^\circ$			30	ms	Note 10-4	
	Fall	$\phi = 0^\circ$			50	ms		
Reflectance Ratio	R			TBD		%		
Brightness			170	220		cd/m <sup>2</sup>	Note 10-2	
White Chromaticity	X	$\theta = 0^\circ$	0.250	0.300	0.350		Note 10-2	
	y		0.260	0.310	0.360			
Lamp Life Time	+25		10,000			hr		

Note 10-1 :  $CR = \frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

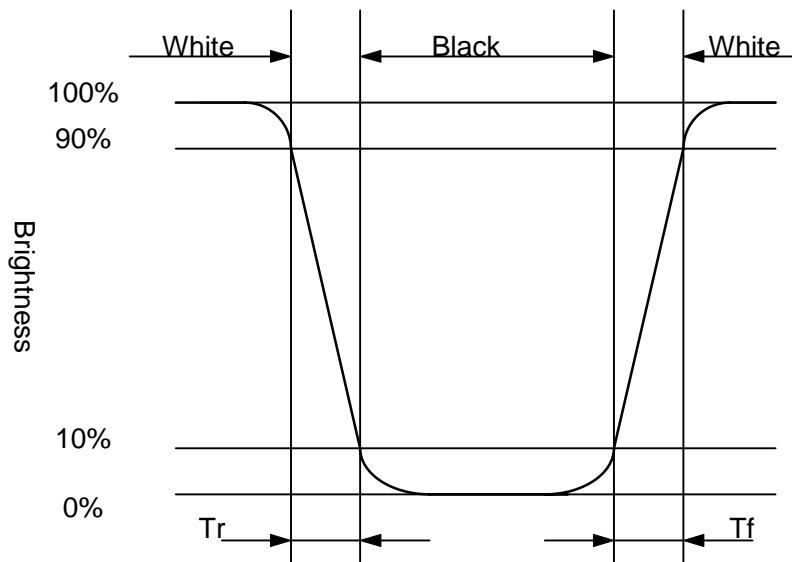
Contrast Ratio is measured in optimum common electrode voltage.  
The test configurations of contrast ratio see section 10-2.

- Note 10-2 : 1.Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).  
 2.Lamp current : 3 mA  
 3.Inverter model : TDK-347.

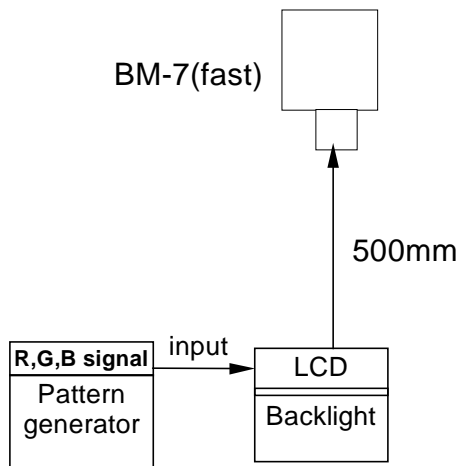
Note 10-3 : The definition of viewing angle diagrams :



Note 10-4 : The definitions of response time:

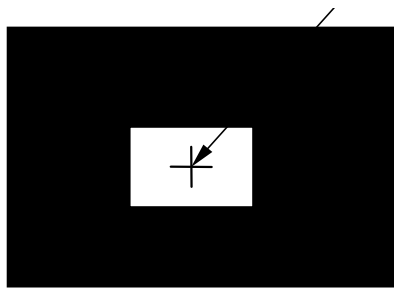


10-2) Test Configuration

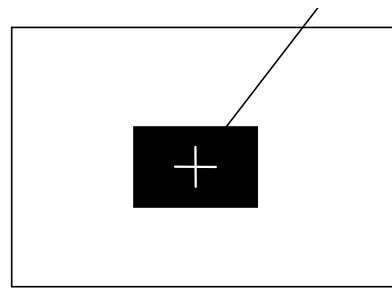


Caution: 1. Environmental illumination  $\leq 1$  lux  
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display Testing Point

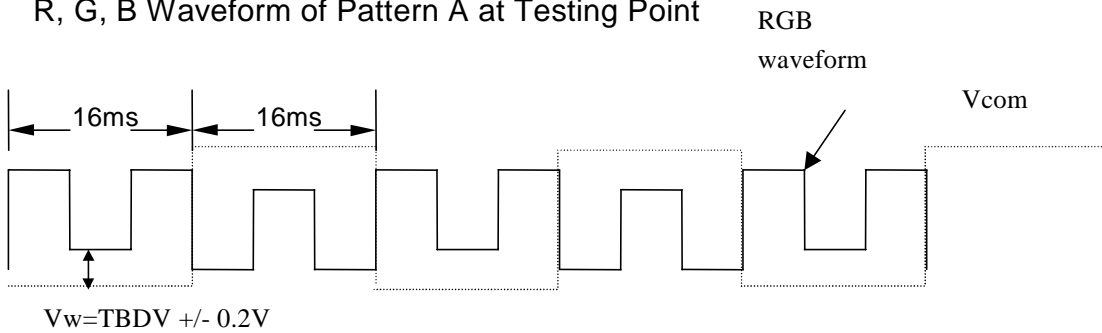


Pattern A

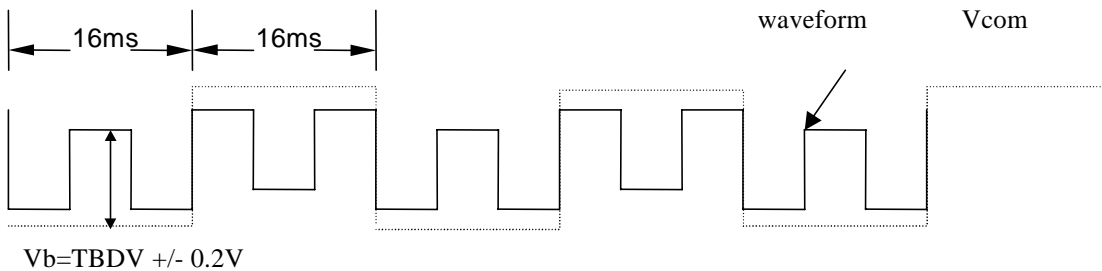


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



## 11. Handling Cautions

### 11-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
  - 1. The noise from the backlight unit will increase.
  - 2. The output from inverter circuit will be unstable.
  - 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

### 11-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

### 11-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

### 11-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many Hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

## 12. Reliability

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70 , 240 hrs
2	Low Temperature Storage Test	Ta = -20 , 240 hrs
3	Low Temperature Operation Test	Ta = 0 , 240 hrs
4	High Temperature & High Humidity Operation Test	Ta = +60 , 95%RH, 240 hrs
5	Thermal Cycling Test (non-operating)	-25 → +25 → +70 , 200 Cycles 30 min 5min 30 min
6	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.0 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
7	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
8	Electrostatic Discharge Test (non-operating)	150pF, 330Ω Air: ±15KV; Contact: ±8KV 10 times/point, 4 points/panel face

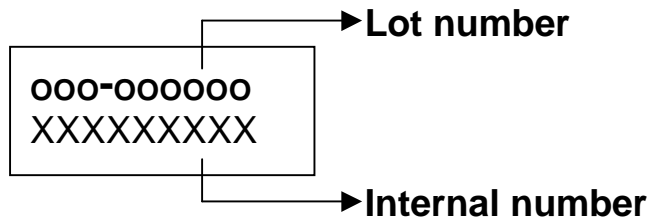
Ta: ambient temperature

### [Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

## 13. Indication of Lot Number Label

a) Indicated contents of the label



Contents of lot number : SB9—STC OEM product

5th—Production year : 1999⇒9, 2000⇒A, 2001⇒1.....

6th—Production month : 1, 2, 3,...9, A, B, C

7th~10th—Serial numbers : 0001~9999

## 14. Block Diagram

