MINDSPEED
BUILD IT FIRST

MC2045-3

Postamplifier for Applications to 200Mbps

FEATURES

- Low-cost IC, fabricated in advanced sub-micron BiCMOS process
- 1.5mV input sensitivity
- Wide range programmable input-signal level detect
- Fully differential design
- Supports 3.3V and 5V supplies
- Available in TSSOP20, SOIC16 and QSOP16 package as well as die form
- Complimentary PECL data & signal detect logic outputs

DESCRIPTION

The **MC2045-3** is an integrated, high gain limiting amplifier intended for fibre optic communication to 200Mbps. Normally placed following the photodetector & transimpedance amplifier, the post-amplifier provides the necessary gain to give PECL compatible logic outputs.

The **MC2045-3** also includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. The signal detect function has typically 2.25dB (optical) of hysteresis which prevents chatter at low input levels.

A squelch function, which turns off the output when no signal is present, is provided by externally connecting the $\overline{ST}$ output to the JAM input.

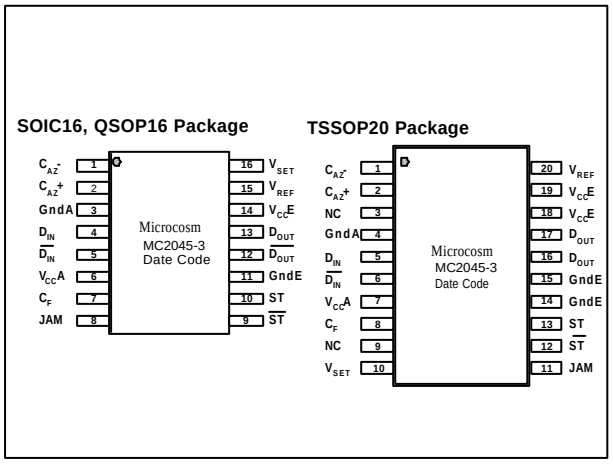
APPLICATIONS

- SDH/SONET/ATM
- Fast Ethernet
- FDDI
- ESCON

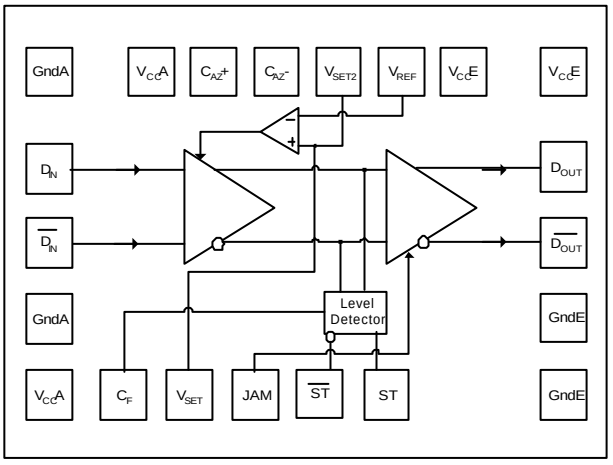
ORDERING INFORMATION

Part	Pin-Package
MC2045-3DIEWP	Waffle pack
MC2045-3WAFER	Expanded Whole 8"on a 10" Grip Ring
MC2045-3S16	SOIC16
MC2045-3Q16	QSOP16
MC2045-3T20	TSSOP20

CONNECTIONS



TOP LEVEL DIAGRAM



PIN DESCRIPTION

Pin Name	16 SOIC Pin No.	20 TSSOP Pin No.	Function
C_{AZ}-	1	1	Auto-zero capacitor pin.
C_{AZ}+	2	2	Auto-zero capacitor pin.
GNDA	3	4	Analogue section ground pin. Connect to most negative supply. Must be at same potential as GNDE Pin.
D_{IN}	4	5	Differential data input.
$\overline{D_{IN}}$	5	6	Inverse differential data input.
V_{CC}A	6	7	Analogue section power pin. Connect to most positive supply. Must be at the same potential as V_{CC}E pin.
C_F	7	8	Level-detect filter capacitor pin. Connect the capacitor between this pin and V_{CCA}.
JAM	8	11	PECL compatible input controlling output buffers (D_{OUT} and $\overline{D_{OUT}}$ pins). On chip pull-down defaults to low. Can be driven from CMOS.
$\overline{ST}$	9	12	Logical inverse of ST Pin. May be connected to JAM Pin to enable automatic squelch function to operate. PECL output.
ST	10	13	Input signal-level status. This PECL output is LOW when the input signal is below the threshold set by the uses.
GNDE	11	14, 15	Digital section ground pin. Connect to the most negative supply. Must be at the same potential as GNDA Pin.
$\overline{D_{OUT}}$	12	16	Logical inverse of D_{OUT} Pin. JAM high forces $\overline{D_{OUT}}$ high. In phase with $\overline{D_{IN}}$.
D_{OUT}	13	17	PECL compatible diffential Data Output. JAM high forces D_{OUT} low. In phase with D_{IN}.
V_{CC}E	14	18,19	Digital output section power pin. Connect to the most positive supply must be at same potential as V_{CC}A pin.
V_{REF}	15	20	Connect to positive supply via resistor. Sets value of internal reference current.
V_{SET}	16	10	Input threshold-level setting circuit. Connect to V_{CC} via a resistor.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-Gnd)	6	V
T_A	Operating ambient	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IN}	Input signal voltage Single-ended: Differential:	0.5 1	-	400 800	mVpp
V_{OS}	Effective input offset voltage	-	-	50	µV
V_N	Input RMS noise in 100MHz	-	-	85	µV
V_{TH}	Input level detect programmability	2	-	100	mVpp
V_{HYS}	Level detect hysteresis (optical)	1.85	2.25	3.00	dB
I_{INJ}	JAM input current HIGH	-10	-	10	µA
I_{CC}	Supply current (no ECL loads)	-	-	35	mA
V_{OH}	PECL(1) output HIGH	(2) -1.025 (3) -1.075	- -	-0.88 -0.88	V
V_{OL}	PECL(1) output LOW	(2) -1.81 (3) -1.86	- -	-1.62 -1.62	V

(1) 50Ω to V_{CC} -2V

(2) 0 to +80°C

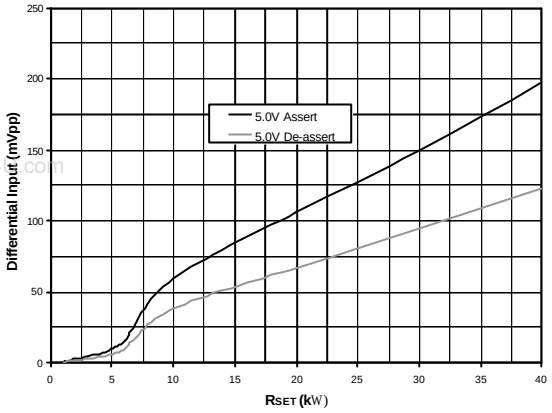
(3) -40°C

AC CHARACTERISTICS

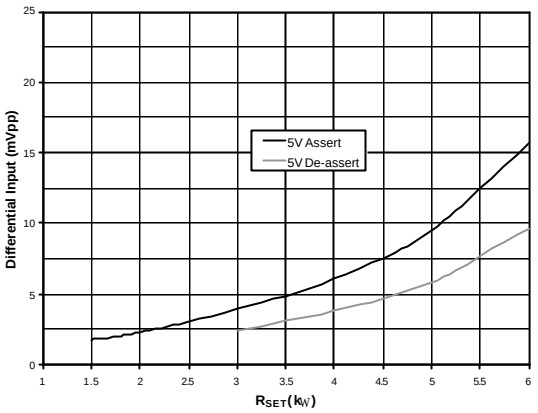
Symbol	Parameter	Min.	Typ.	Max.	Units
BW	Bandwidth: Gain >60dB	100	-	-	MHz
R_{IN}	Input resistance	-	10	-	kΩ
C_{IN}	Input capacitance	-	-	2	pF
t_{PWD}	Pulse width distortion	-	-	0.4	ns
t_R, t_F	ECL out rise / falltimes (20-80% points)	-	1.0	2.0	ns

TYPICAL PERFORMANCE CURVES

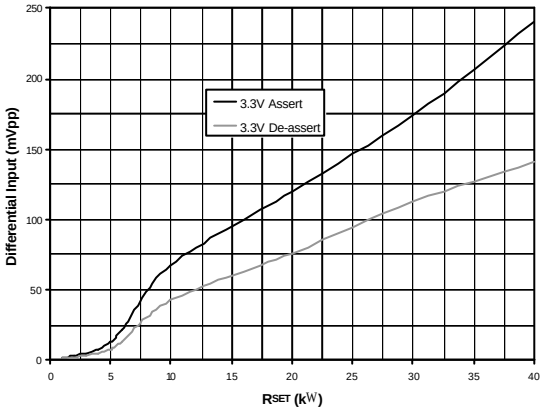
Typical Signal Detect (5V)



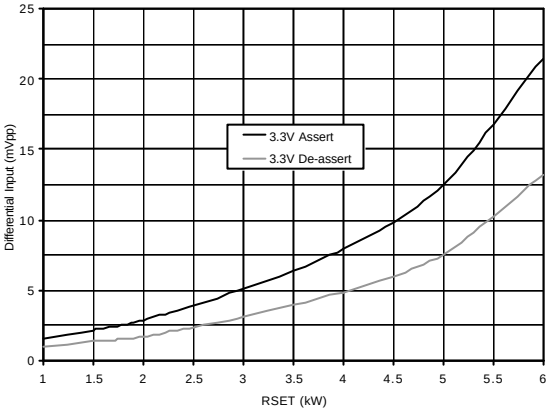
Signal Detect Detail (5V)



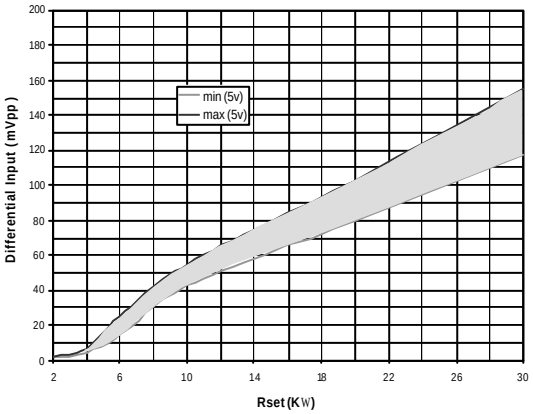
Typical Signal Detect (3.3V)



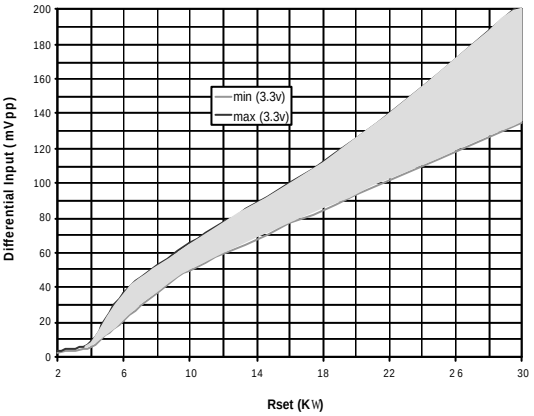
Signal Detect Detail (3.3V)



Signal Detect Assert Range (5V)
(over process and temperature)

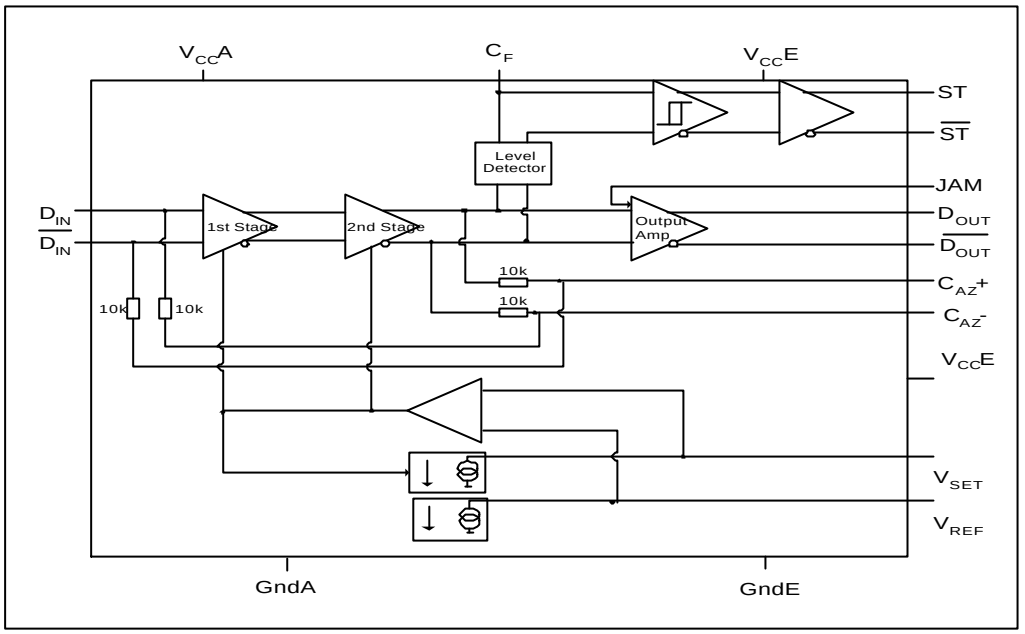


Signal Detect Assert Range (3.3V)
(over process and temperature)



Note: For all of these graphs R_{REF} = 2kΩ

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input

The Data Input pins are internally DC biased at approximately V_{CC}-1V. The MC2045-3 signals are AC coupled, using capacitors. These capacitors must be large enough to pass the lowest frequencies of interest (consecutive '1's or '0's) considering the input resistance.

For example, at 155Mbps SONET, there is a maximum of 72 consecutive '1' s, which is is 465ns. To acheive the maximum allowed data dependant jitter, the low frequency cut-off needs to be lower by a factor of 10. However, it is better to set it at least one decade lower, due to the interaction of the time constants for the input stage and the DC restore circuitry, giving an input capacitor value of 2.2nF.

DC Offset Compensation

An autozero circuit is included to remove the effects of DC offset. An external capacitor smoothes the feed back, acting with the internal 10kΩ circuit resistance to pass the lowest frequencies of interest. At data rates between 125Mbps and 155 Mbps, this is normally set to 180pF.

Level detector

The input data is first amplified, with the level of amplification set by the ratio of R_{SET}/R_{REF}. This amplification level sets the level of input at which the status thresholds operate. The data is then rectified and low-pass filtered before being compared with a reference voltage. The low-pass filter is controlled by C_F, and 10nF will provide a nominal 2µS time constant, thus avoiding false triggering due to variation in edge density of data.

The comparator has the equivalent of 2.25dB (typ.) of optical hysteresis.

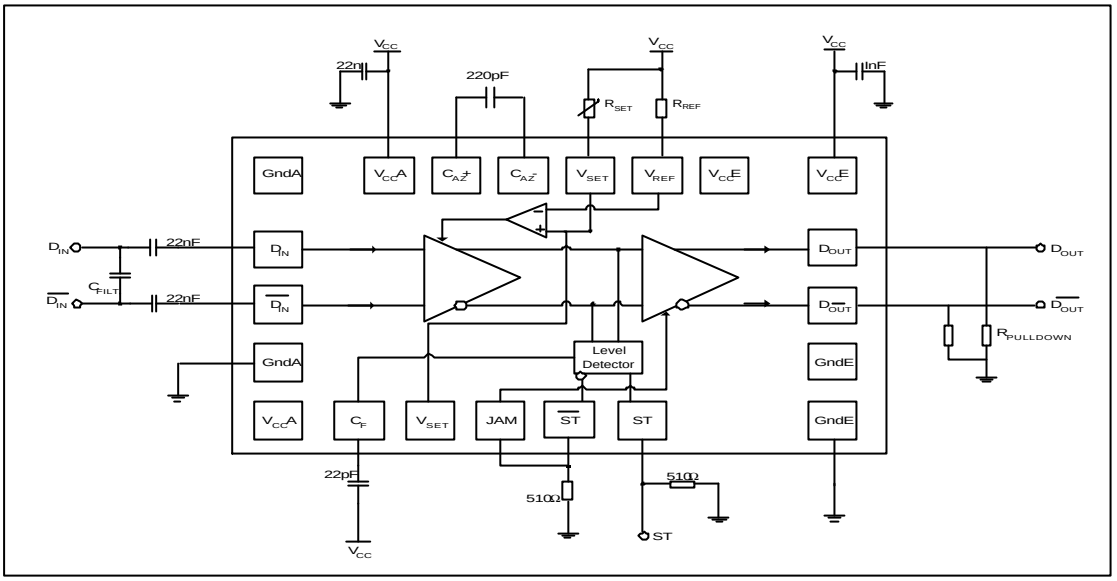
Squelch Function

The MC2045-3 provides for programmable input-signal level detection, and this may be used to automatically force the data outputs to a known state if the input signal falls below threshold using the JAM input. This is normally used to allow data to propagate only when the signal is above the users' Bit-Error-Rate (BER) requirement. It therefore stops the data outputs toggling due to noise when no signal is present.

In order to implement this function, ST should be connected to the JAM, thus forcing the data outputs to logical zero when the signal falls below threshold.

Note that R_{SET} and R_{REF} must be connected, even if the Level-Detect function is not required.

TYPICAL APPLICATIONS CIRCUIT



APPLICATIONS INFORMATION

Setting Signal Detect

The MC2045-3 uses two external resistors to set the signal detect level Rref is set to 2kΩ for all applications. Rset is chosen using the graphs on page -4-. The value is dependant on supply voltage and should be chosen for 3.3V or 5V operation. If 3.3V and 5V operation are to be supported inter-changeably set R_{SET} based on the 3.3V graphs.
The graphs also show the variation over process and temperature of the signal detect assert level. This, along with the minimum and maximum hysteresis are used to predict the usable sensitivity of the system.

PECL Termination

The outputs of the MC2045-3 are ECL100K and 300K compatible and any of the standard termination techniques can be used. The postamplifier PECL outputs often have to drive a transmission line. The most common method is to use pull-down resistors to V_{EE} on the ECL outputs. This provides a DC current path for the ECL outputs in order to maintain the emitter follower outputs in the transistor's active region. A shunt resistor equal to twice the characteristic impedance across the differential outputs is used to terminate the transmission lines at the other end.

Another termination technique is to terminate with a resistor equal to the characteristic impedance of the transmission line to a DC voltage of V_{CC} – 2V. This has the advantage that the resistance value is the same for 3.3V and 5V operation and it also has performance advantages at high data rates. The DC voltage must be within 5% of nominal and must be adequately de-coupled. This can be implemented using a parallel (Thevenin) resistance combination.

The value of the pull-down and termination resistors can be selected from the tables below:

5V Supply

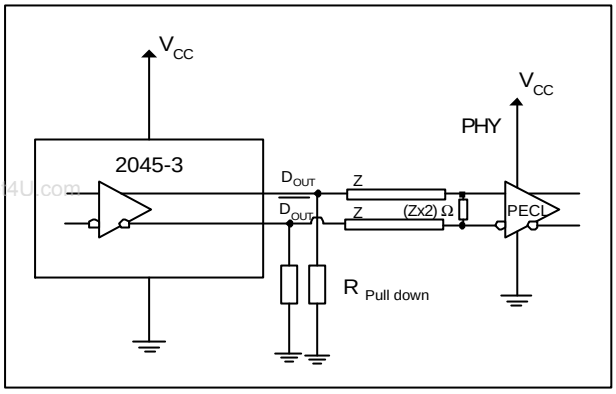
Impedance	Pull-down	Termination	Thevenin (R_{TOP})	Thevenin (R_{BOTTOM})
50Ω	270Ω	100Ω	82Ω	130Ω
75Ω	390Ω	150Ω	120Ω	180Ω

3.3V Supply

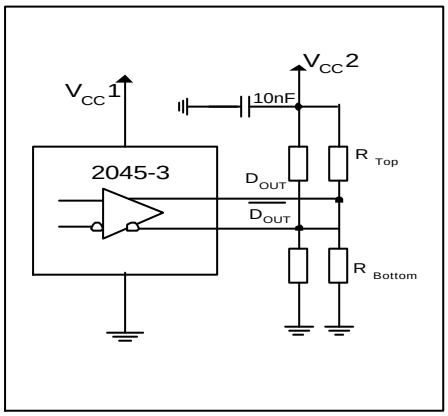
Impedance	Pull-down	Termination	Thevenin (Top)	Thevenin (Bottom)
50Ω	150Ω	100Ω	130Ω	82Ω
75Ω	220Ω	150Ω	180Ω	120Ω

APPLICATIONS INFORMATION

DC Coupled PECL Termination



Thevenin PECL Termination



Power supply decoupling & optimising sensitivity

The MC2045-3 is not expected to require ferrite beads in order to give adequate performance. However, if optimum MC2045-3 sensitivity is required, the V_{CC}A and GndA pins of the MC2045-3 should each be connected to their respective power rails via a ferrite suppressor, such as Murata BLM31A601SPT.

Capacitors should be chosen with low effective series resistance, low dissipation factor and high Q. NPO or COG temperature characteristics are preferred because they provide more reliable performance over a wide range of environmental conditions.

Small surface mount packages are recommended since they exhibit less parasitic inductance which can lower the overall effectiveness of the bypass capacitor at high frequencies. Filter capacitors should be placed close to the transceiver power and ground pins to minimise noise coupling which can occur between the filter and the transceiver.

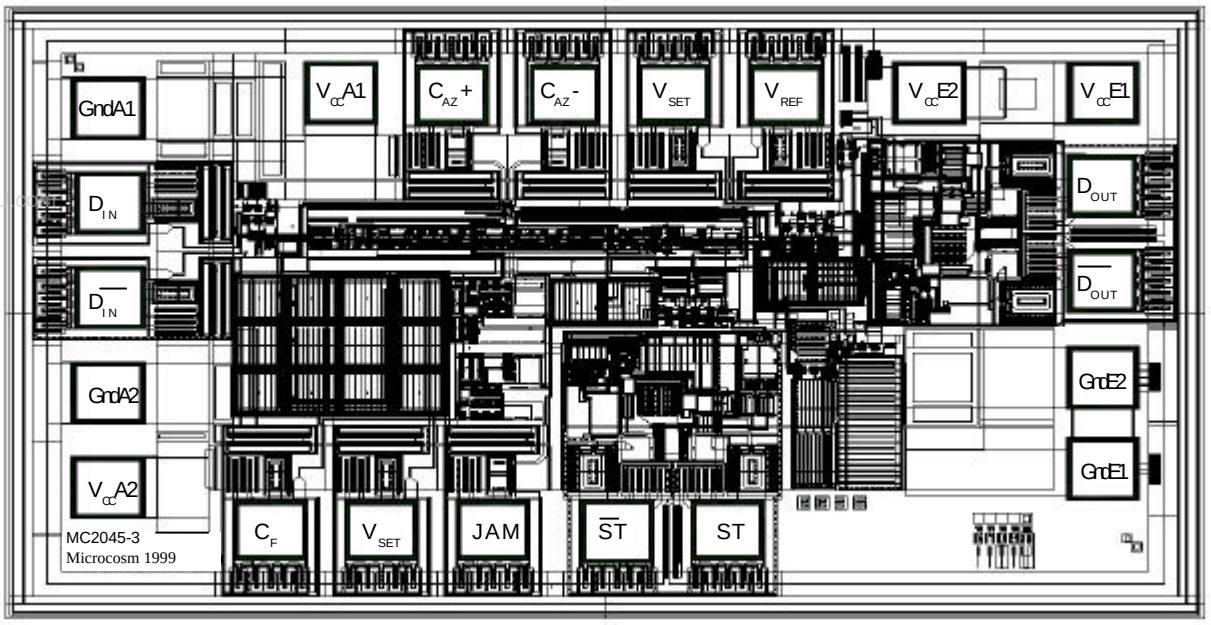
Differences between die and packaged parts:

V_{SET} and V_{SET2} are alternative inputs to the same 'Vset' function. Connect one or other, not both.

There are 2 sets of V_{CC}A and GndA on the left of the die. Only one pair need be connected, though no harm will result from both pairs being connected. On the TSSOP package, pairs of V_{CC}E and GndE connections are connected.

BARE DIE INFORMATION

Chip Layout



Pad Size 85x85 µm

Pad Centres

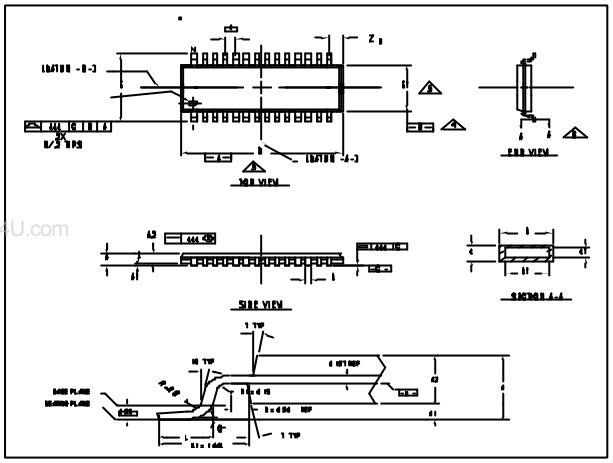
Description	X	Y
C_{AZ}-	-56.8	347.5
C_{AZ}+	-207	347.5
V_{CC}A1	-356.9	347.5
GndA1	-670	322.6
D_{IN}	-670	172.6
D_{IN}	-670	22.4
GndA2	-670	-127.6
V_{CC}A2	-670	-277.5
C_F	-451.4	-347.5
V_{SET}2	-301.3	-347.5
JAM	-151.2	-347.5

Description	X	Y
ST	15.8	-347.5
ST	166	-347.5
GndE1	670.8	-248
GndE2	670.8	-103
D_{OUT}	670.8	50.1
D_{OUT}	670.8	200.3
V_{CC}E1	670.8	347.5
V_{CC}E2	436.9	347.5
V_{REF}	243.4	347.5
V_{SET}	93.2	347.5

Pad coordinates are in µm, and are measured from the centre of the die to the centre of the pad.

PACKAGE INFORMATION

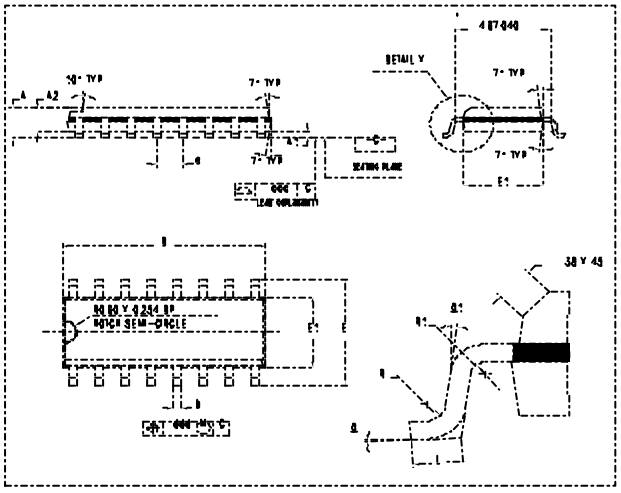
20 Lead Thin Small Shrink Outline Package (TSSOP)



Dims	Tols/Leads	20L	24L
A	MAX.	1.20	
A1		.05 MIN/.10 MAX	
A2	NOM.	.90	
D	± .05	6.50	7.80
E	± .10	6.40	
E1	± .10	4.40	
L	+.15/-.10	.60	
L1	REF.	1.00	
Zp	REF.	.325	

Dims	Tols/Leads	20L	24L
e	BASIC	.65	
b	± .05	.22	
c		.13 MIN/.20 MAX	
e	± 4°	4°	
aaa	MAX.	.10	
bbb	MAX.	.10	
ccc	MAX.	.05	
ddd	MAX.	.20	

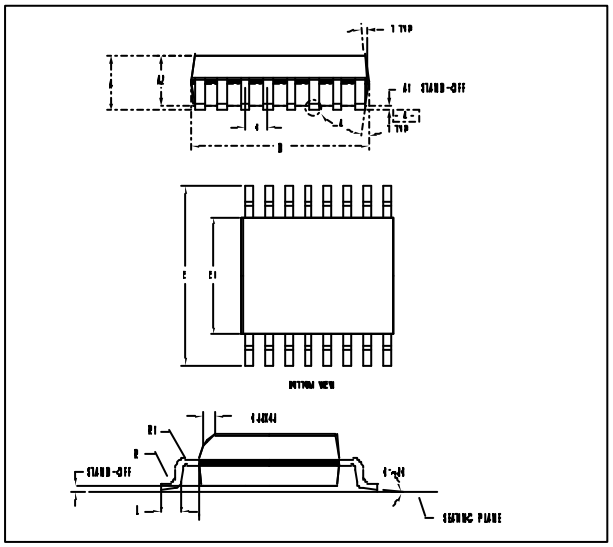
16 Lead Small Outline Package (SOIC)



Dims	Tols/N	8
A	MAX.	1.70
A1	± .05	0.17
A2	± .10	1.38
D	± .10	9.9
E	± .20	6.00
E1	± .10	3.90
L	± .05	0.5
ccc	MAX.	0.10

Dims	Tols/N	8
ddd	MAX.	0.10
e	BASIC	1.27
b	± .05	0.43
0		0°~7°
01	± 4°	7°
R	MAX.	0.20
R1	TYP.	0.13

16 Lead Quarter Small Outline Package (QSOP)



Dims	Tols/N	16
A	MAX.	1.60
A1	± .05	0.1
A2	± .10	1.40
D	± .10	4.9
E	± .20	6.00
E1	± .10	3.90
L	± .05	0.6

Dims	Tols/N	16
ccc	MAX.	0.10
ddd	MAX.	0.10
e	BASIC	0.65
b	± .05	0.25
c	± .05	.2 min .24 max
R	± .05	0.20
R1	MIN.	0.20

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