



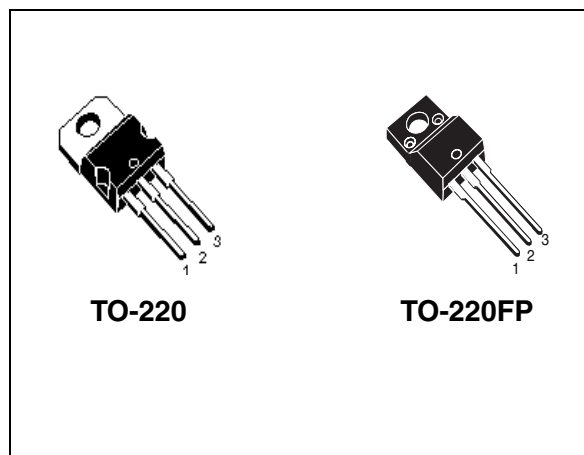
STP3HNK90Z STF3HNK90Z

N-channel 900V - 0.35Ω - 3A - TO-220 - TO-220FP
Zener-protected SuperMESH™ Power MOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STP3HNK90Z	900 V	< 0.42 Ω	3 A
STF3HNK90Z	900 V	< 0.42 Ω	3 A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



Description

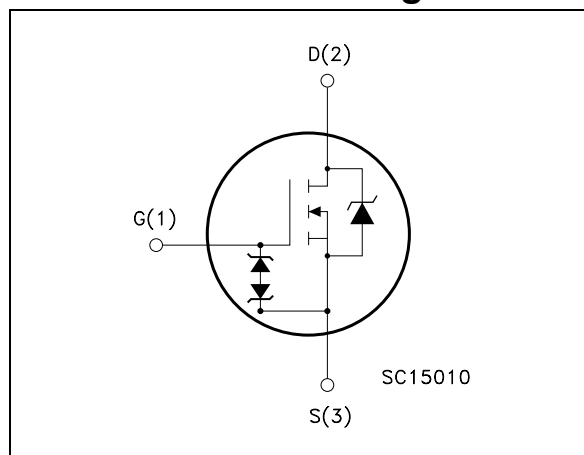
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

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Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP3HNK90Z	P3HNK90Z	TO-220	Tube
STF3HNK90Z	F3HNK90Z	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		STP3HMK90Z	STF3HMK90Z	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	800		V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	800		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	3	3 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	1.89	1.89 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	12	12 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	90	25	W
	Derating factor	0.72	0.2	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3000		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)	-	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 3A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case Max	1.38	5	°C/W
R_{thj-a}	Thermal resistance junction-ambient Max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	3	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	200	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (Open Drain)	30			V

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	900			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating},$ $T_c = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{GS} = 0$)	$V_{GS} = \pm 30V$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 1.5 A$		3.5	4.2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 1.5A$		19		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		690		pF
C_{oss}	Output capacitance			71		pF
C_{rss}	Reverse transfer capacitance			14.4		pF
$C_{osseq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 720V$		88		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450V, I_D = 1.5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 18)		23		ns
t_r	Rise time			28		ns
$t_{d(off)}$	Off-voltage rise time			42		ns
t_f	Fall time			27		ns
Q_g	Total gate charge	$V_{DD} = 720V, I_D = 3A$ $V_{GS} = 10V$		26	35	nC
Q_{gs}	Gate-source charge			5.7		nC
Q_{gd}	Gate-drain charge			13.9		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=3\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=3\text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$, $V_{DD}=50\text{V}$, $T_j=25^\circ\text{C}$ (see Figure 20)		494		ns
Q_{rr}	Reverse recovery charge			2.4		μC
I_{RRM}	Reverse recovery current			9.8		A
t_{rr}	Reverse recovery time	$I_{SD}=3\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$, $V_{DD}=50\text{V}$, $T_j=150^\circ\text{C}$ (see Figure 20)		628		ns
Q_{rr}	Reverse recovery charge			3.2		μC
I_{RRM}	Reverse recovery current			10.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

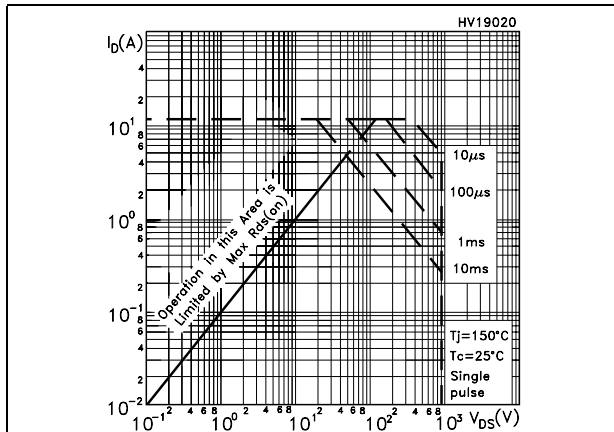


Figure 2. Thermal impedance for TO-220

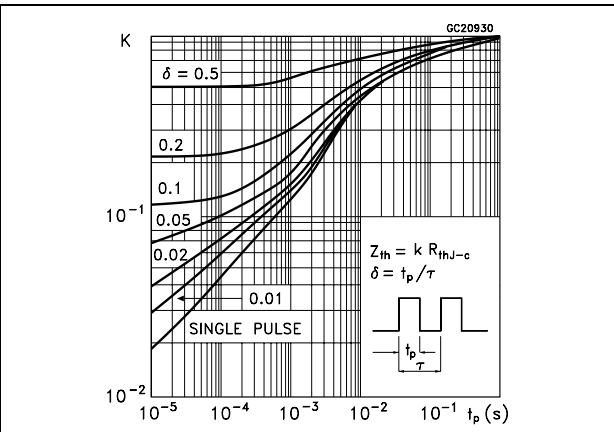


Figure 3. Safe operating area for TO-220FP

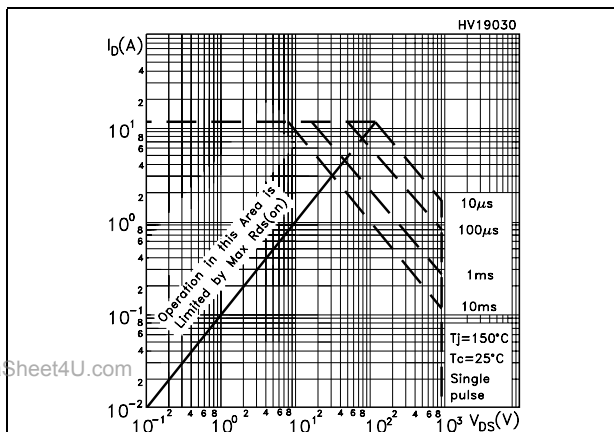


Figure 4. Thermal impedance for TO-220FP

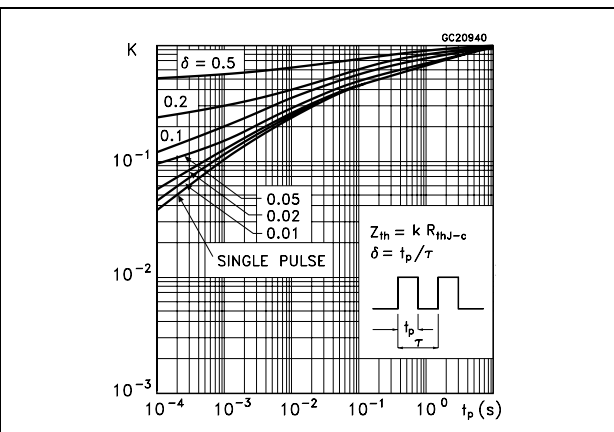


Figure 5. Output characteristics

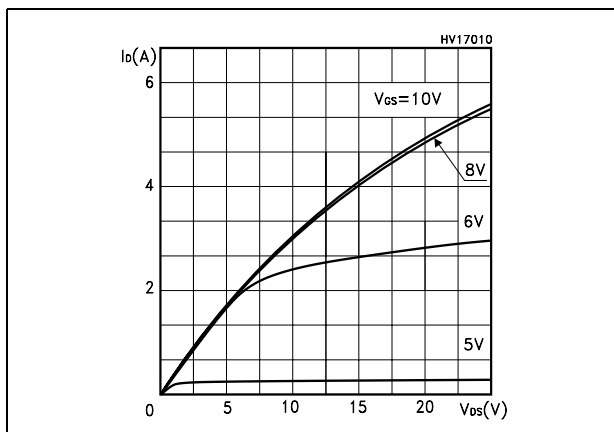
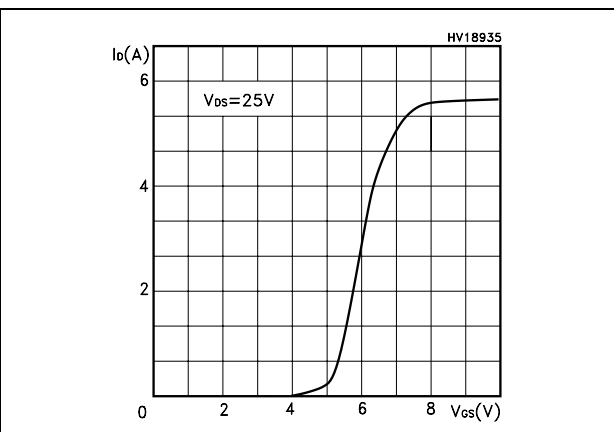


Figure 6. Transfer characteristics



Electrical characteristics

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Figure 7. Transconductance

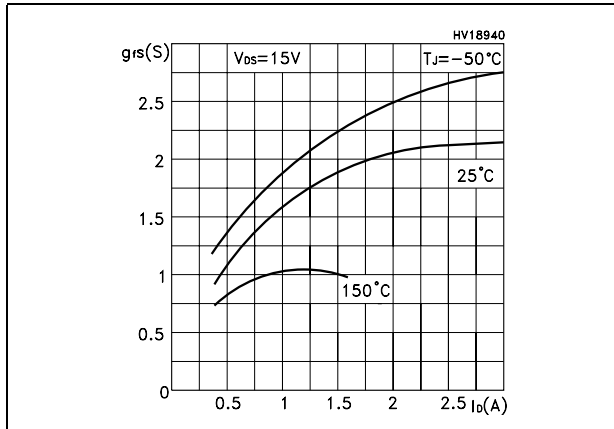


Figure 8. Static drain-source on resistance

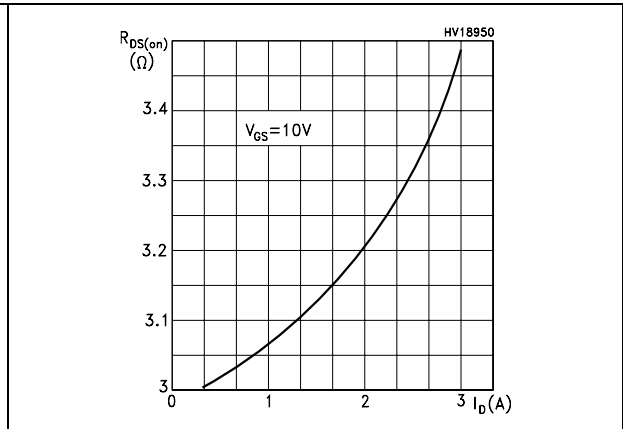


Figure 9. Gate charge vs gate-source voltage

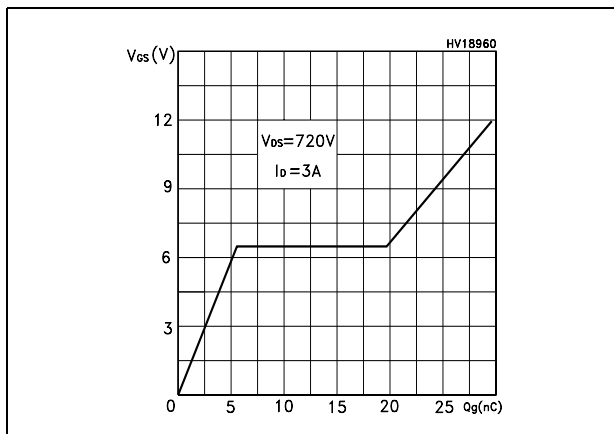


Figure 10. Capacitance variations

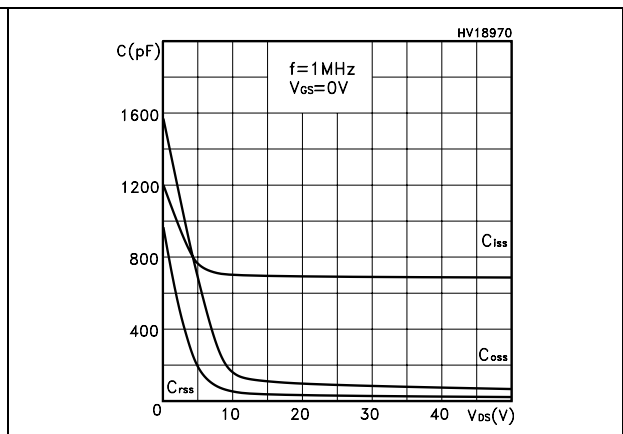


Figure 11. Normalized gate threshold voltage vs temperature

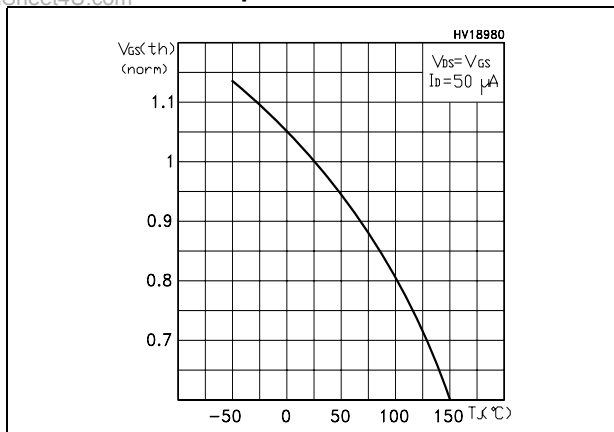


Figure 12. Normalized on resistance vs temperature

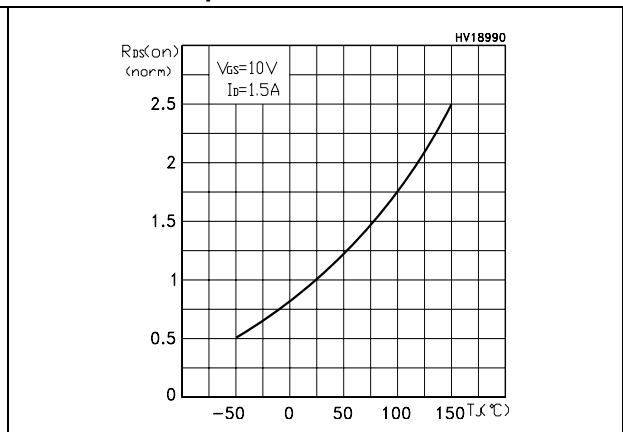


Figure 13. Source-drain diode forward characteristics

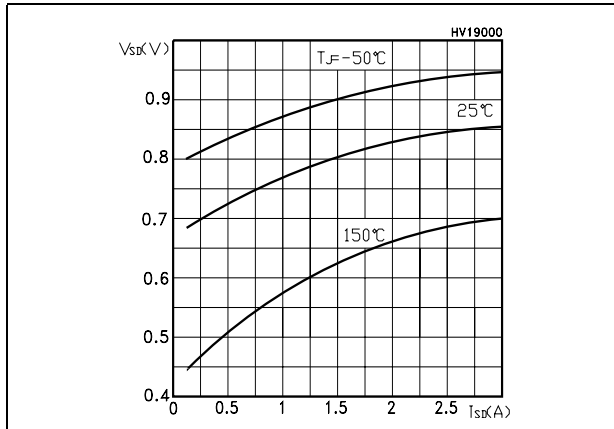


Figure 14. Normalized $B_{V_{DSS}}$ vs temperature

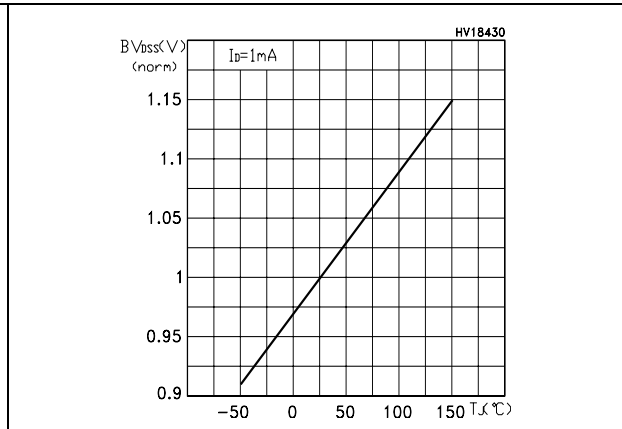
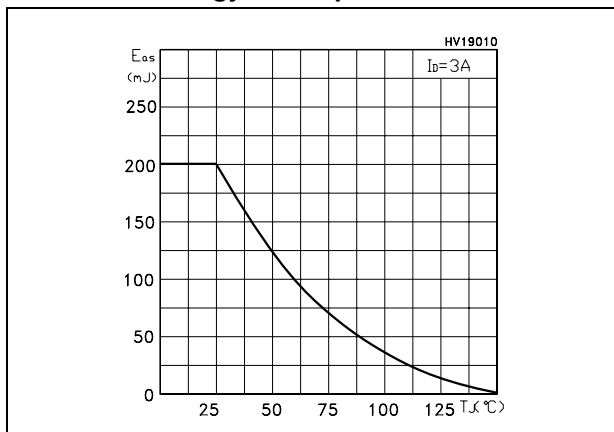


Figure 15. Maximum avalanche energy vs temperature



3 Test circuit

Figure 16. Unclamped Inductive load test circuit

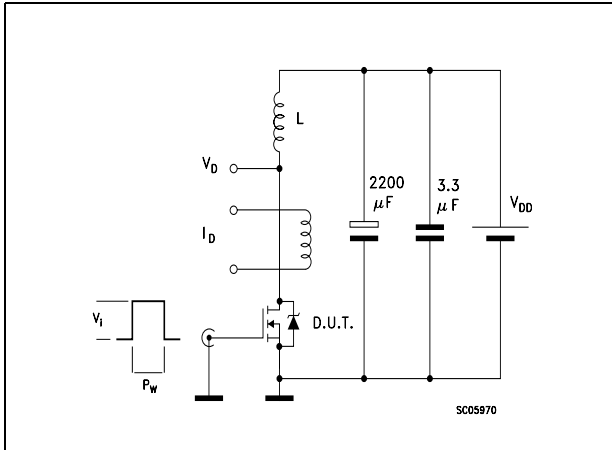


Figure 17. Unclamped Inductive waveform

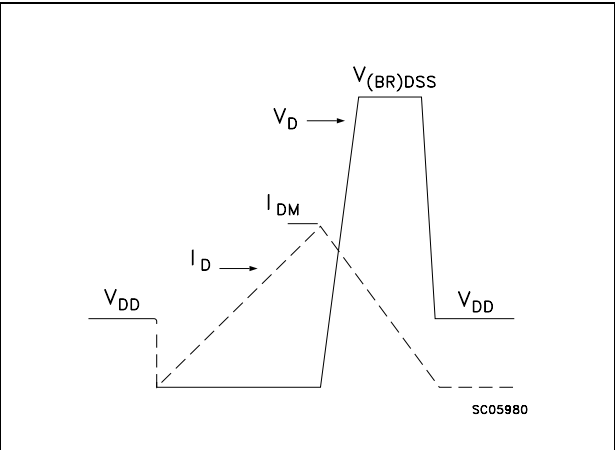


Figure 18. Switching times test circuit for resistive load

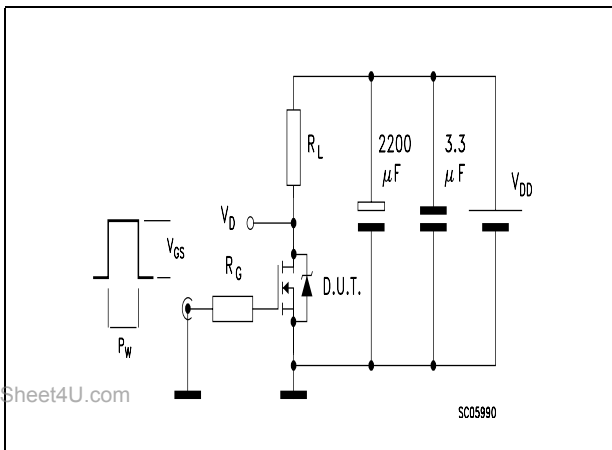


Figure 19. Gate charge test circuit

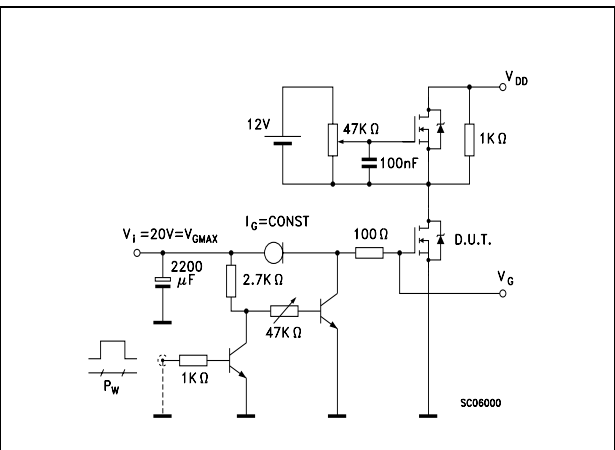
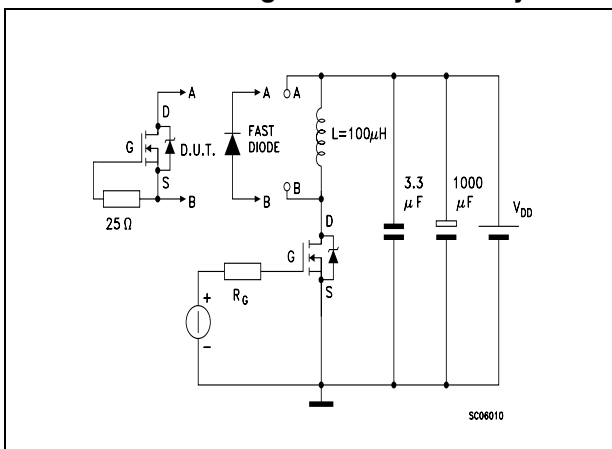


Figure 20. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

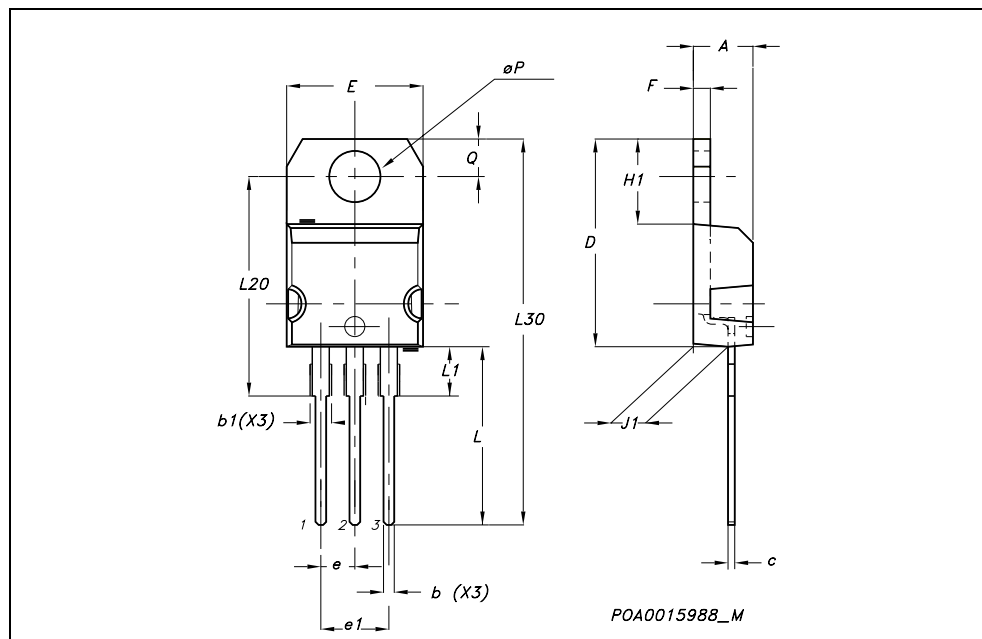
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Package mechanical data

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TO-220 MECHANICAL DATA

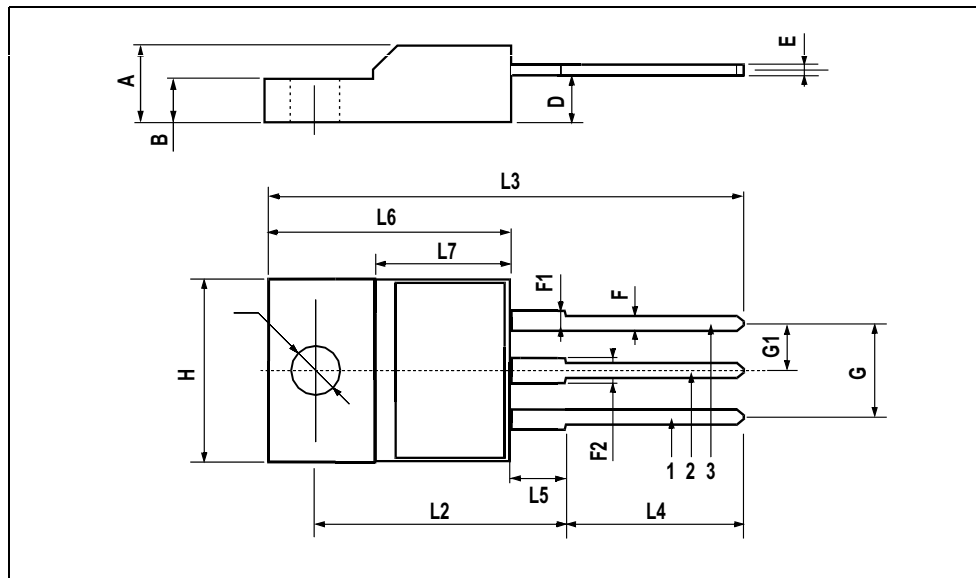
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



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TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Sep-2004	2	Complete document
10-Aug-2006	3	New template, no content change

STP3HNK90Z - STF3HNK90Z

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