INTEGRATED CIRCUITS

DATA SHEET

74HC3GU04
Inverter

Product specification
Supersedes data of 2003 Aug 18

2003 Nov 26

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FEATURES

- Wide operating voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT505-2 and SOT765-1 package
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74HC3GU04 is a high-speed Si-gate CMOS device.

The 74HC3GU04 provides the inverting single stage function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	C_L = 50 pF; V_{CC} = 4.5 V	6	ns
C_I	input capacitance		3	pF
C_{PD}	power dissipation capacitance	notes 1 and 2	5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total switching outputs;
   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	**nY**
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC3GU04DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	HU04
74HC3GU04DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	HU4

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	3Y	data output
3	2A	data input
4	GND	ground (0 V)
5	2Y	data output
6	3A	data input
7	1Y	data output
8	V_{CC}	supply voltage

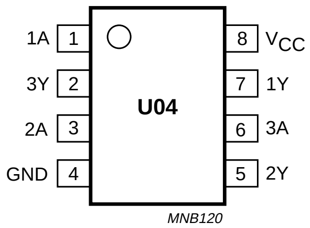


Fig.1 Pin configuration.

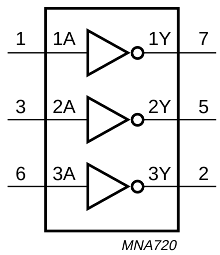


Fig.2 Logic symbol.

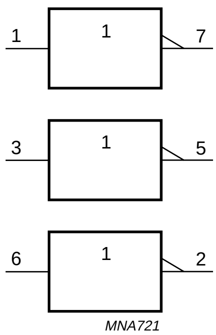


Fig.3 Logic symbol (IEEE/IEC).

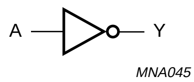


Fig.4 Logic diagram (one driver).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	ns
		V_{CC} = 4.5 V	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V; note 1	–	±20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V; note 1	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current	note 1	–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		2.0	1.7	1.1	–	V
			4.5	3.6	2.4	–	V
			6.0	4.8	3.1	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.9	0.3	V
			4.5	–	2.1	0.9	V
			6.0	–	2.9	1.2	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –20 μA	2.0	1.9	2.0	–	V
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –20 μA	6.0	5.9	6.0	–	V
		I_O = –4.0 mA	4.5	4.13	4.32	–	V
		I_O = –5.2 mA	6.0	5.63	5.81	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	2.0	–	0	0.1	V
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 20 μA	6.0	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.33	V
		I_O = 5.2 mA	6.0	–	0.16	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	6.0	–	–	10	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.7	–	–	V
			4.5	3.6	–	–	V
			6.0	4.8	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.3	V
			4.5	–	–	0.9	V
			6.0	–	–	1.2	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –20 μA	2.0	1.9	–	–	V
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –20 μA	6.0	5.9	–	–	V
		I_O = –4.0 mA	4.5	3.7	–	–	V
		I_O = –5.2 mA	6.0	5.2	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.4	V
		I_O = 5.2 mA	6.0	–	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	6.0	–	–	20	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

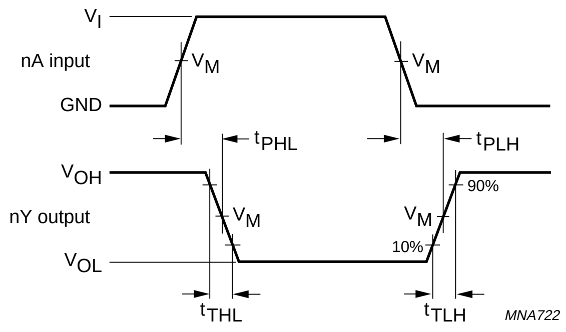
GND = 0 V; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = –40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	see Figs.5 and 6	2.0	–	13	75	ns
			4.5	–	6	15	ns
			6.0	–	5	13	ns
t_{THL}/t_{TLH}	output transition time	see Figs.5 and 6	2.0	–	18	95	ns
			4.5	–	6	19	ns
			6.0	–	5	16	ns
T_{amb} = –40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	see Figs.5 and 6	2.0	–	–	90	ns
			4.5	–	–	18	ns
			6.0	–	–	15	ns
t_{THL}/t_{TLH}	output transition time	see Figs.5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns

Note

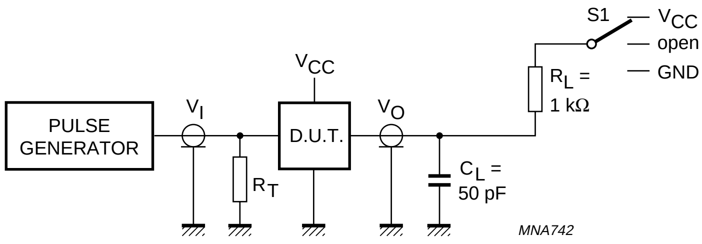
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



V_M = 50%; V_I = GND to V_{CC}.

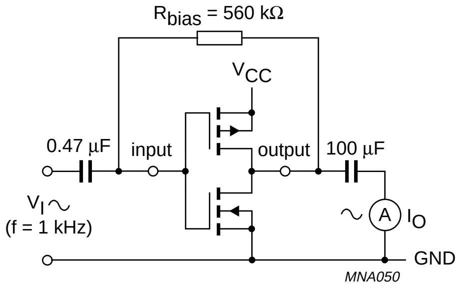
Fig.5 The input (nA) to output (nY) propagation delays and the output transition times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = load resistor.
C_L = load capacitance including jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

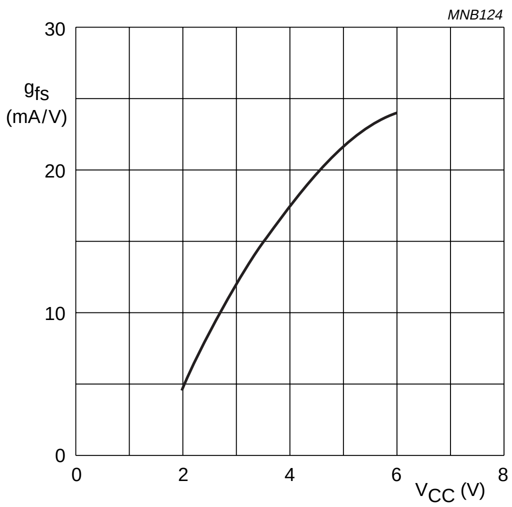
Fig.6 Load circuitry for switching times.



$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$.

V_O is constant.

Fig.7 Test set-up for measuring forward transconductance.



T_{amb} = 25 °C.

Fig.8 Typical forward transconductance (g_{fs}) as a function of the supply voltage (V_{CC}).

TYPICAL TRANSFER CHARACTERISTICS

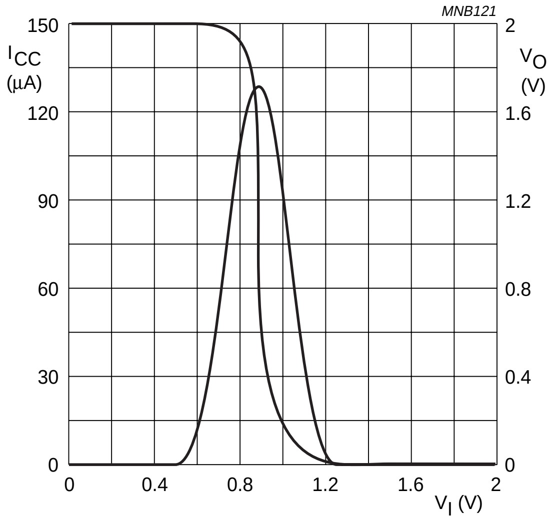


Fig.9 V_{CC} = 2.0 V; I_O = 0.

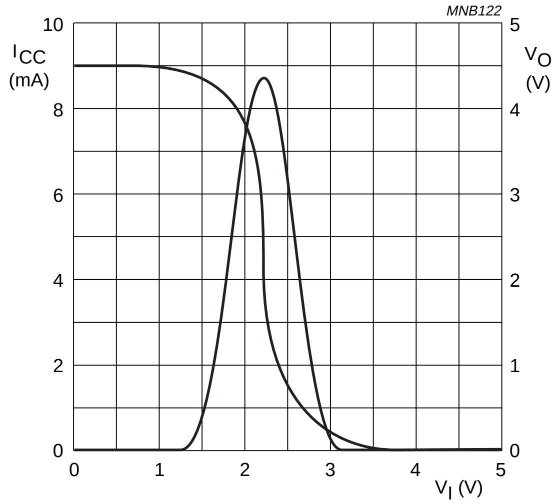


Fig.10 V_{CC} = 4.5 V; I_O = 0.

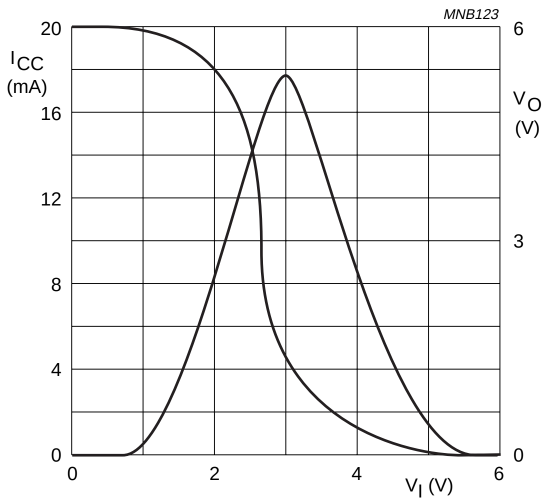
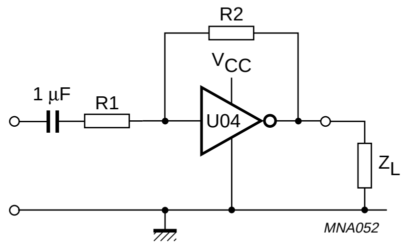


Fig.11 V_{CC} = 6.0 V; I_O = 0.

APPLICATION INFORMATION

All values given are typical unless otherwise specified.

Linear amplifier



$V_{O\,(max)\,(p-p)} \approx V_{CC} - 1.5\ V$ centered at $0.5V_{CC}$;

$$A_u = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})}$$

A_{OL} = open loop amplification.

A_u = voltage amplification.

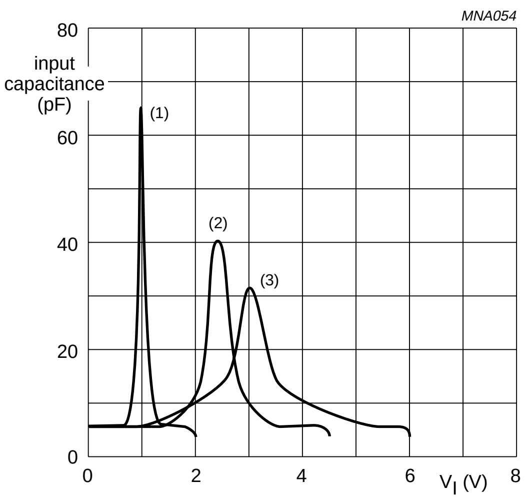
R1 ≥ 3 kΩ, R2 ≤ 1 MΩ.

Z_L > 10 kΩ; A_{OL} = 20 (typical).

Typical unity gain bandwidth product is 5 MHz.

Input capacitance see Fig.13.

Fig.12 Linear amplifier configuration.



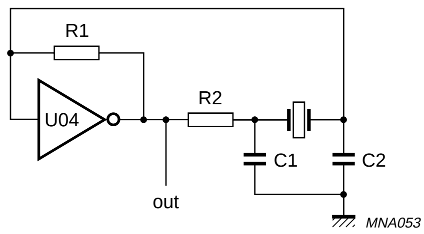
(1) V_{CC} = 2.0 V.

(2) V_{CC} = 4.5 V.

(3) V_{CC} = 6.0 V.

Fig.13 Typical input capacitance as a function of the input voltage.

Crystal oscillator



C1 = 47 pF (typical).

C2 = 22 pF (typical).

R1 = 1 to 10 MΩ (typical).

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f = 1 MHz).

Fig.14 Crystal oscillator configuration.

Table 1 External components for resonator (f < 1 MHz)

FREQUENCY (kHz)	R1 (MΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)
10 to 15.9	2.2	220	56	20
16 to 24.9	2.2	220	56	10
25 to 54.9	2.2	100	56	10
55 to 129.9	2.2	100	47	5
130 to 199.9	2.2	47	47	5
200 to 349.9	2.2	47	47	5
350 to 600	2.2	47	47	5

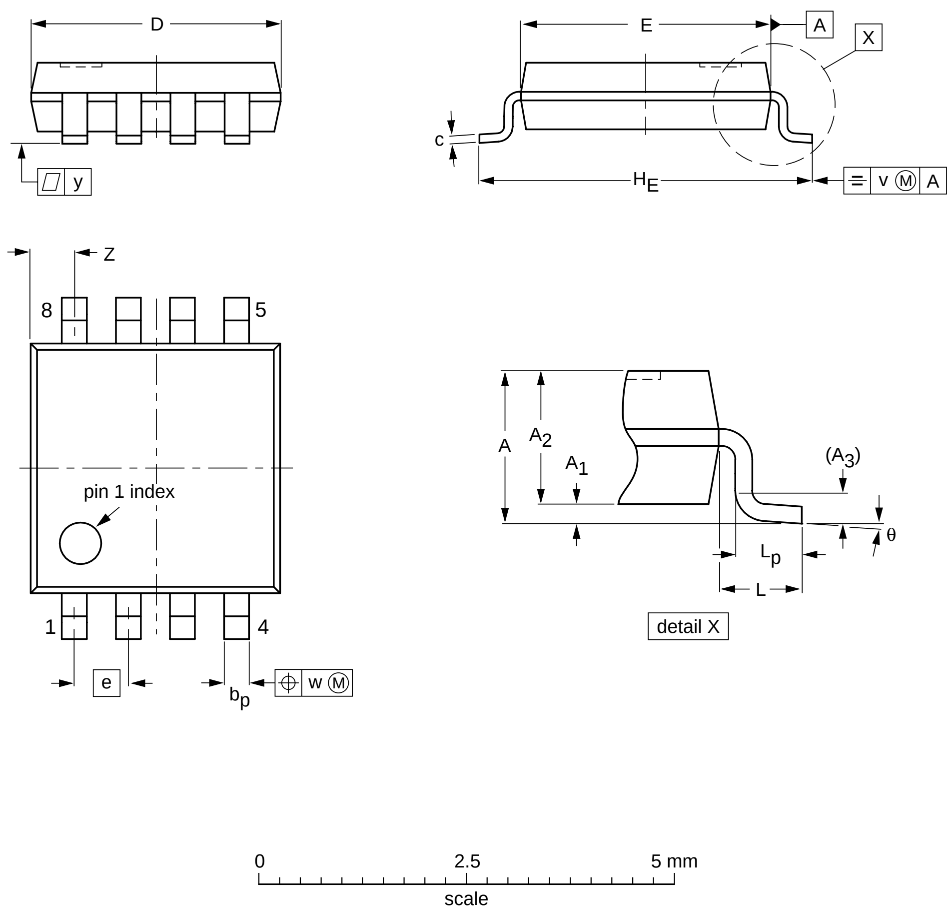
All values given are typical and must be used as an initial set-up.

Table 2 Optimum value for R2

FREQUENCY (kHz)	R2 (kΩ)	OPTIMUM FOR
3	2.0	minimum required I_{CC}
	8.0	minimum influence due to change in V_{CC}
6	1.0	minimum required I_{CC}
	4.7	minimum influence by V_{CC}
10	0.5	minimum required I_{CC}
	2.0	minimum influence by V_{CC}
14	0.5	minimum required I_{CC}
	1.0	minimum influence by V_{CC}
>14	replace R2 by C3 = 35 pF (typical)	

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

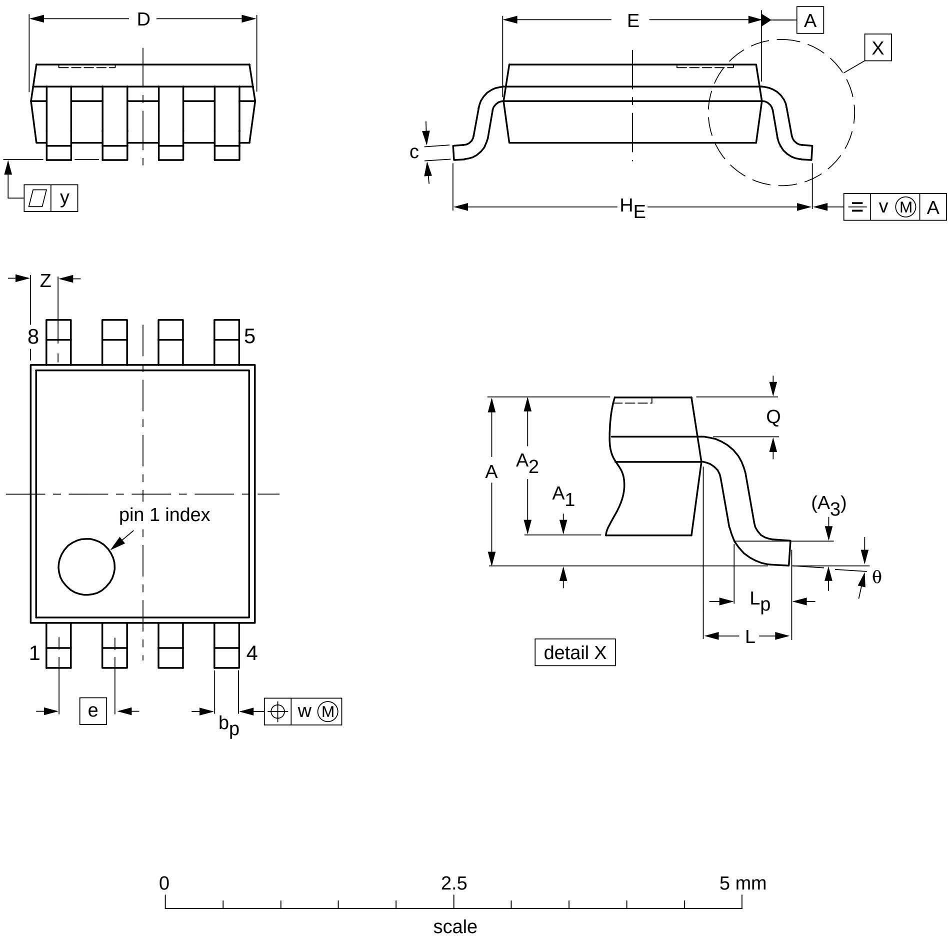
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

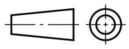
VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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