DATA SHEET

O K I A S I C P R O D U C T S

MSM30R/32R/92R
0.5µm Sea Of Gates and Customer Structured Arrays

August 2002

Oki Semiconductor

CONTENTS

Oki Semiconductor

MSM30R/32R/92R

Second-Generation 0.5μm Sea of Gates and Customer Structured Arrays

DESCRIPTION

Oki's second-generation 0.5μm ASIC products are available in both Sea Of Gates (SOG) and Customer Structured Array (CSA) architectures. The MSM30R Series, MSM32R Series, and MSM92R Series all offer increased density over their first-generation counterparts, as well as 3-V I/O buffers that are 5-V tolerant. Both the SOG-based MSM30R Series and the CSA-based MSM92R Series use a three-layer metal process on 0.5μm drawn (0.4μm L-effective) CMOS technology. The SOG-based MSM32R Series uses the same SOG base-array architecture as the MSM30R Series, but offers two metal layers instead of three. The semiconductor process is adapted from Oki's production-proven 16-Mbit DRAM manufacturing process.

The second-generation 0.5μm family retains the high speed and low power of Oki's first-generation 0.5μm MSM13R/12R/98R family. The second-generation 0.5μm family also shares the same die sizes for arrays with corresponding I/O counts, but the second-generation arrays can contain up to 60% more gates than their first-generation counterparts. The second-generation family is optimized for 3-V core operation, with optimized 3-V I/O buffers and 3-V I/O buffers that are 5-V tolerant, whereas the first-generation family offers separate I/O buffers for mixed 3-V and 5-V operation. Oki's first-generation and second-generation 0.5μm families together offer an unusually flexible mixed-voltage ASIC capability.

The 3-layer-metal MSM30R SOG Series contains 8 array bases, offering up to 448 I/O pads and over 600K raw gates. The 2-layer metal MSM32R SOG Series contains five array bases, offering up to 320 I/O pads and over 300K raw gates. These SOG array sizes are designed to fit the most popular Quad Flat Pack (QFP) and Plastic Ball Grid Array (PBGA) packages. The MSM30R and MSM32R Series' SOG architecture allows rapid prototyping turnaround times, additionally offering the most cost-effective solution for pad-limited circuits (particularly the 2-layer metal MSM32R Series).

The 3-layer-metal MSM92R CSA Series contains 36 array bases, offering a wider span of gate and I/O counts than SOG Series. Oki uses the EPOCH memory compiler from Cascade Design Automation to generate optimized single- and dual-port RAM macrocells for CSA designs. As such, the MSM92R Series is suited to memory-intensive ASICs and high-volume designs where fine tuning of package size produces significant cost or real-estate savings.

FEATURES

- 0.5μm drawn two and three-layer metal CMOS
- Optimized 3.3-V core
- Optimized 3-V I/O and 3-V I/O that is 5-V tolerant
- SOG and CSA architecture availability
- 120-ps typical gate propagation delay (for a 2-input 4x-drive NAND gate with a fan-out of 2 and 0mm of wire, operating at 3.3 V)
- Up to 1.2M raw gates and 624 pads
- User-configurable I/O with V_{SS}, V_{DD}, TTL, 3-state, and 1 mA ~ 24 mA options
- Slew-rate-controlled outputs for low-radiated noise
- Clock tree cells with ≤ 0.5-ns clock skew, worst-case (fan-out ≥ 9000 at 75 MHz)
- User-configurable single and dual-port memories
- Specialized macrocells, including phase-locked loop, GTL, PECL, and PCI cells
- Floorplanning for front-end simulation, back-end layout controls, and link to synthesis
- JTAG boundary scan and scan-path ATPG
- Support for popular CAE systems, including Cadence, IKOS, Mentor Graphics, Synopsys, Viewlogic, and Zycad

MSM30R/32R/92R FAMILY LISTING

CSA Part#	CSA Master#	SOG Part#	I/O Pads	Raw Gates	Rows [1]	Columns	Usable Gates [2]
MSM92RB01	B92R020X020	—	80	14,688	72	204	11,750
MSM92RB02	B92R024X024	—	96	22,784	89	256	18,227
MSM92RB03	B92R026X026	MSM30R0020	104	27,440	98	280	21,952
MSM92RB04	B92R030X030	—	120	37,720	115	328	30,176
MSM92RB05	B92R032X032	—	128	43,296	123	352	34,637
—	—	MSM32R0050	144	56,000	140	400	26,880
MSM92RB06	B92R036X036	MSM30R0050	144	56,000	140	400	42,000
MSM92RB07	B92R038X038	—	152	63,176	149	424	47,382
MSM92RB08	B92R040X040	—	160	70,336	157	448	52,752
MSM92RB09	B92R042X042	—	168	78,352	166	472	58,764
—	—	MSM32R0080	176	86,304	174	496	38,837
MSM92RB10	B92R044X044	MSM30R0080	176	86,304	174	496	60,413
MSM92RB11	B92R048X048	—	192	103,904	191	544	72,733
MSM92RB12	B92R050X050	—	200	114,400	200	572	80,080
—	—	MSM32R0120	208	123,968	208	596	49,587
MSM92RB13	B92R052X052	MSM30R0120	208	123,968	208	596	86,778
MSM92RB14	B92R056X056	—	224	144,900	225	644	101,430
MSM92RB15	B92R060X060	—	240	167,464	242	692	117,225
—	—	MSM32R0190	256	191,660	259	740	72,831
MSM92RB16	B92R064X064	MSM30R0190	256	191,660	259	740	126,496
MSM92RB17	B92R068X068	—	272	217,488	276	788	143,542
MSM92RB18	B92R072X072	—	288	244,948	293	836	161,666
MSM92RB19	B92R076X076	—	304	274,040	310	884	180,866
—	—	MSM32R0300	320	306,072	327	936	110,186
MSM92RB20	B92R080X080	MSM30R0300	320	306,072	327	936	195,886
MSM92RB21	B92R084X084	—	336	338,496	344	984	216,637
MSM92RB22	B92R088X088	—	352	372,552	361	1032	238,433
MSM92RB23	B92R092X092	—	368	408,240	378	1080	261,274
MSM92RB24	B92R096X096	MSM30R0440	384	445,560	395	1128	276,247
MSM92RB25	B92R100X100	—	400	484,512	412	1176	300,397
MSM92RB26	B92R104X104	—	416	525,096	429	1224	325,560
MSM92RB27	B92R108X108	—	432	569,096	446	1276	352,840
MSM92RB28	B92R112X112	—	448	613,012	463	1324	367,807
MSM92RB29	B92R118X118	—	472	682,644	489	1396	409,586
MSM92RB30	B92R122X122	—	488	730,664	506	1444	438,398
MSM92RB31	B92R126X126	—	504	780,316	523	1492	468,190
MSM92RB32	B92R132X132	—	528	857,072	548	1564	514,243
MSM92RB33	B92R138X138	—	552	941,360	574	1640	564,816
MSM92RB34	B92R144X144	—	576	1,025,488	599	1712	615,293
MSM92RB35	B92R150X150	—	600	1,115,000	625	1784	669,000
MSM92RB36	B92R156X156	—	624	1,206,400	650	1856	723,840

1. Row and column numbers are used to evaluate the number and size of mega macrocells that may be included into each array.
2. Usable gate count is design dependent and varies based upon the number of fan-outs per net, internal busses, floor plan, RAM/ROM blocks, etc.

ARRAY ARCHITECTURE

The primary components of a 0.5µm MSM30R/32R/92R circuit include:

- I/O base cells
- Configurable I/O pads for V_{DD}, V_{SS}, or I/O (optimized 3-V I/O and 3-V I/O that is 5-V tolerant)
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells containing N-channel and P-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility

Each array has 24 dedicated corner pads for power and ground use during wafer probing, with four pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and output drive transistors (V_{DDO} and V_{SSO}).

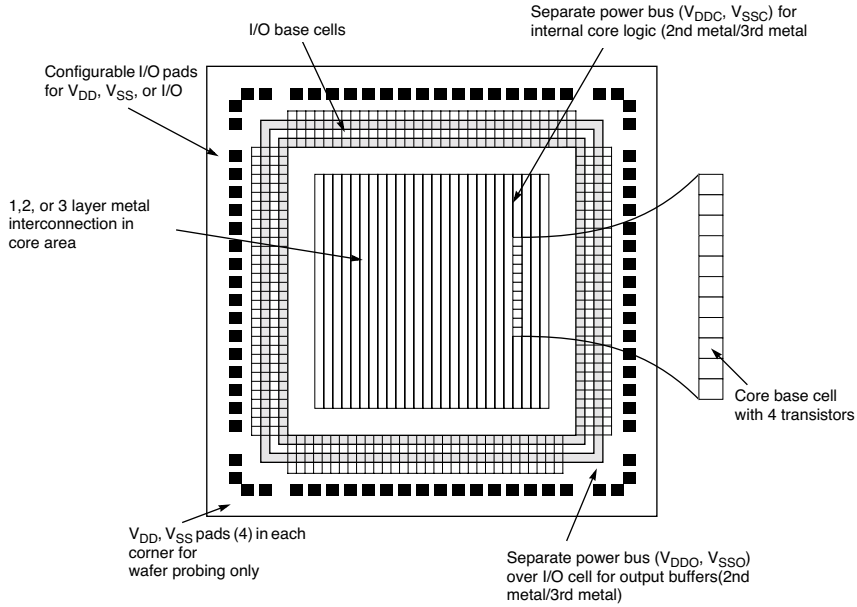


Figure 7. MSM30R0000 Array Architecture

MSM92R000 CSA Layout Methodology

The procedure to design, place, and route a CSA follows.

1. Select suitable base array frame from the available predefined sizes. To select an array size:
   - Identify the macrocell functions required and the minimum array size to hold the macrocell functions.

- Add together all the area occupied by the required random logic and macrocells and select the optimum array.

2. Make a floor plan for the design's megacells.
   - Oki Design Center engineers verify the master slice and review simulation.
   - Oki Design Center or customer engineers floorplan the array using Oki's proprietary floorplanner or HLD DP3 and customer performance specifications.
   - Using Oki CAD software, Design Center engineers remove the SOG transistors and replace them with diffused memory macrocells to the customer's specifications.

Figure 8 shows an array base after placement of the optimized memory macrocells.

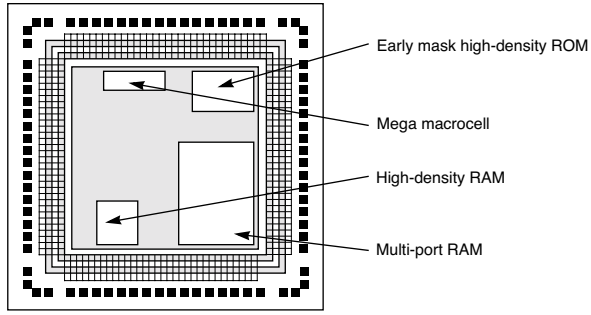


Figure 8. Optimized Memory Macrocell Floor Plan

3. Place and route logic into the array transistors.
   - Oki Design Center engineers use layout software and customer performance specifications to connect the random logic and optimized memory macrocells.

Figure 9 marks the area in which placement and routing is performed with cross hatching.

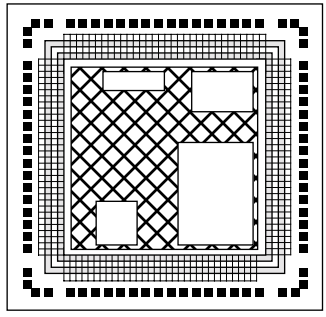


Figure 9. Random Logic Place and Route

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0 V, T_j = 25° C) [1]

Parameter		Symbol	Conditions	Rated Value	Unit
Power supply voltage		V_{DD}	-	-0.3 ~ +4.6	V
Input voltage	(Normal Buffer)		-	-0.3 ~ V_{DD}+0.3	
	(5V Tolerant Buffer)	V_I	V_{DD} = +0.3 ~ 3.6V	-0.3 ~ 6.0	
			V_{DD} < 3.0V	-0.3 ~ V_{DD}+0.3	
Output voltage	(Normal Buffer)	V_O	-	-0.3 ~ V_{DD}+0.3	
	(5V Tolerant Buffer)		V_{DD} = +0.3 ~ 3.6V	-0.3 ~ 6.0	
			V_{DD} < 3.0V	-0.3 ~ V_{DD}+0.3	
Input current	(Normal Buffer)	I_I	-	-10 ~ + 10	mA
	(5V Tolerant Buffer)		-	-6 ~ + 6	
Output current	1mA buffer	I_O	-	-6 ~ + 6	
	2mA buffer		-	-6 ~ +6	
	4mA buffer		-	-8 ~ +8	
	6mA buffer		-	-12 ~ + 12	
	8mA buffer		-	-16 ~ + 16	
	12mA buffer		-	-24 ~ + 24	
	24mA buffer		-	-48 ~ + 48	
Storage temperature		Tj	-	-65 ~ +150	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions in the other specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter		Symbol	Rated Value			Unit
			Min	Typ.	Max	
Power supply voltage	Core	V_{DD}	+3.0	+3.3	+3.6	V
Junction temperature		Tj	-40	-	+85	°C
Input rise time/fall time		tr, tf	-	2	20	ns

DC Characteristics (V_{DD} = 3.0 V ~ 3.6 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
High-level input voltage	VIH	TTL normal input	2.0	-	V_{DD}+0.3	V
		TTL 5V tolerant input	2.0	-	5.5	
Low-level input voltage	VIL	TTL normal input	-0.3	-	0.8	
		TTL 5V tolerant input	-0.3	-	0.8	
TTL-level Schmitt Trigger threshold voltage (Normal buffer)	Vt+	TTL normal input	-	-	2.0	
	Vt-		0.7	-	-	
	ΔVt	Vt+ - Vt-	0.4	-	-	
TTL-level Schmitt Trigger threshold voltage (5V tolerant buffer)	Vt+	TTL 5V tolerant input	-	-	2.0	
	Vt-		0.7	-	-	
	ΔVt	Vt+ - Vt-	0.4	-	-	
High-level output voltage (Normal buffer)	VOH	IOH=-100 μA	V_{DD}-0.2	-	-	
		IOH=-1,-2,-4,-6,-8, -12,-24 mA	2.4	-	-	
High-level output voltage (5V tolerant buffer)		IOH=-100 μA	V_{DD}-0.2	-	-	
		IOH=-1,-2,-4,-6,-8, -12 mA	2.4	-	-	
Low-level output voltage (Normal buffer)	VOL	IOL=100 μA	-	-	0.2	
		IOL=1,2,4,6,8,12,24 mA	-	-	0.4	
Low-level output voltage (5V tolerant buffer)		IOL=100 μA	-	-	0.2	
		IOL=1,2,4,6,8,12 mA	-	-	0.4	

DC Characteristics (V_{DD} = 3.0 V ~ 3.6 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C) (Continued)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
High-level input current (Normal buffer)	IIH	VIH=V_{DDIO}	-	-	1	μA
		VIH=V_{DDIO} (50kΩ pull down)	15	66	170	
High-level input current (5V tolerant buffer)		VIH=V_{DDIO}	-	-	10	
		VIH=V_{DDIO} (50kΩ pull down)	15	66	170	
		VIH=5.5V	-	-	10	
		VIH=5.5V (3k/50kΩ pull up)	-	-	250	
		VIH=5.5V (50kΩ pull down)	-	-	170	
Low-level_input current (Normal buffer)	IIL	VIL=V_{SS}	-1	-	-	
		VIL=V_{SS} (50kΩ pull up)	-170	-66	-15	
		VIL=V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA
Low-level_input current (5V tolerant buffer)		VIL=V_{SS}	-1	-	-	μA
		VIL=V_{SS} (50kΩ pull up)	-170	-66	-15	
		VIL=V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA
3-state output_ leakage current (Normal buffer)	IOZH	VOH=V_{DDIO}	-	-	1	μA
		VOH=V_{DDIO} (50kΩ pull down)	15	66	170	
	IOZL	VOL=V_{SS}	-1	-	-	
		VOL=V_{SS} (50kΩ pull up)	-170	-66	-15	
		VOL=V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA

DC Characteristics (V_{DD} = 3.0 V ~ 3.6 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C) (Continued)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
3-state output_ leakage current (5V tolerant buffer)	IOZH	VOH=V_{DDIO}	-	-	1	μA
		VOH=V_{DDIO} (50kΩ pull down)	15	66	170	
		VOH=5.5V	-	-	10	
		VOH=5.5V (3k/50kΩ pull up)	-	-	250	
		VOH=5.5V (50kΩ pull down)	-	-	170	
	IOZL	VOL=V_{SS}	-1	-	-	
		VOL=V_{SS} (50kΩ pull up)	-170	-66	-15	
		VOL=V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA

AC Characteristics (V_{DD} = 3.3 V, V_{SS} = 0 V, T_j = 25° C)

Parameter		Driving Type	Conditions [1] [2]	Rated Value [3]	Unit
Internal gate propagation delay	Inverter	1X	F/O= 2 , L= 0 mm	0.12	ns
		2X		0.10	
		4X		0.08	
	2-input NAND	1X		0.17	
		2X		0.14	
		4X		0.12	
	Inverter	1X		0.28	
		2X		0.20	
		4X		0.13	
	2-input NAND	1X	F/O= 2, standard wire length	0.36	
		2X		0.24	
		4X		0.17	
Toggle frequency			F/O= 1, L= 0 mm	630	MHz
Input buffer propagation delay	TTL level, normal input buffer		F/O= 2 ,	0.41 (typ)	ns
	TTL level, 5V tolerant input buffer		standard wire length	0.61 (typ)	
Output buffer propagation delay	Push-pull, Normal output buffer	4 mA	CL= 20 pF	1.87 (typ)	
		8 mA	CL= 50 pF	2.14 (typ)	
		12 mA	CL= 100 pF	2.71 (typ)	
	3-state, 5V tolerant output buffer	4 mA	CL= 20 pF	2.29 (typ)	
Output buffer transition times [4]	Push-pull, Normal output buffer	12 mA	CL= 75 pF	4.09 (r) (typ)	
				3.85 (f) (typ)	
	3-state, 5V tolerant output buffer	4 mA	CL= 20 pF	3.18 (r) (typ)	
				4.00 (f) (typ)	

1. Input transition time in 0.2ns / 3.3V
2. Typical condition in VDD=3.3V and Tj=25°C.
3. Rated value is calculated as an average of the L-H and H-L delay times of each macro type on a typical process.
4. Output rising and falling times are both specified over a 10%-90% range.

MACRO LIBRARY

Oki Semiconductor supports a wide range of macrocells and macrofunctions, ranging from simple hard macrocells for basic Boolean operations to large, user-parameterizable macrofunctions. The following figure illustrates the main classes of macrocells and macrofunctions available.

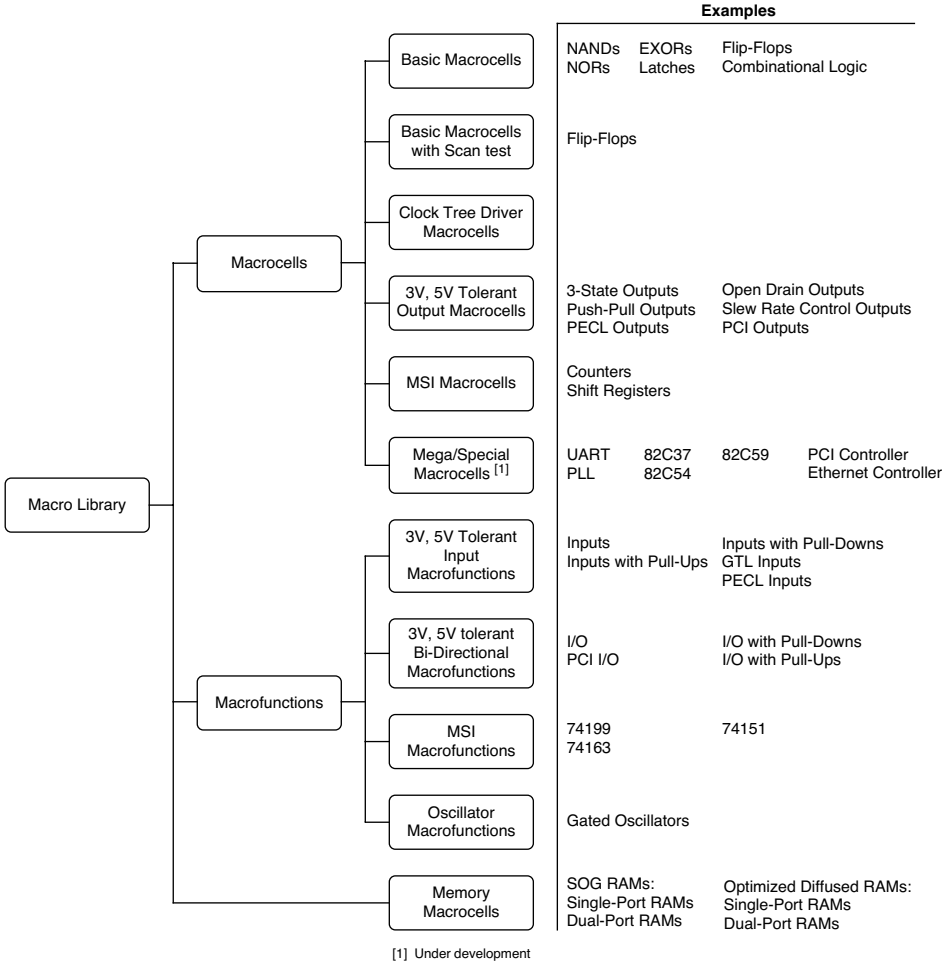


Figure 10. Oki Macrocell and Macrofunction Library

Macrocells for Driving Clock Trees

Oki offers clock-tree drivers that guarantee a skew time of less than 0.5 ns. The advanced layout software uses dynamic driver placement and sub-trunk allocation to optimize the clock-tree implementation for a particular circuit. Features of the clock-tree driver-macrocells include:

- Clock skew ≤ 0.5 ns
- Automatic fan-out balancing
- Dynamic sub-trunk allocation
- Single clock tree driver logic symbol
- Single-level clock drivers
- Automatic branch length minimization
- Dynamic driver placement
- Up to four clock trunks

The clock-skew management scheme is described in detail in Oki's *0.5µm Technology Clock Skew Management Application Note*.

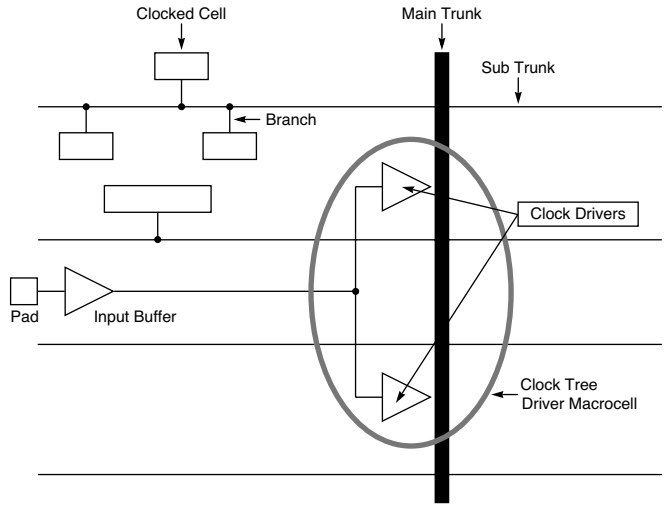


Figure 11. Clock Tree Structure

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

- Floorplanning for front-end simulation and back-end layout control
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements

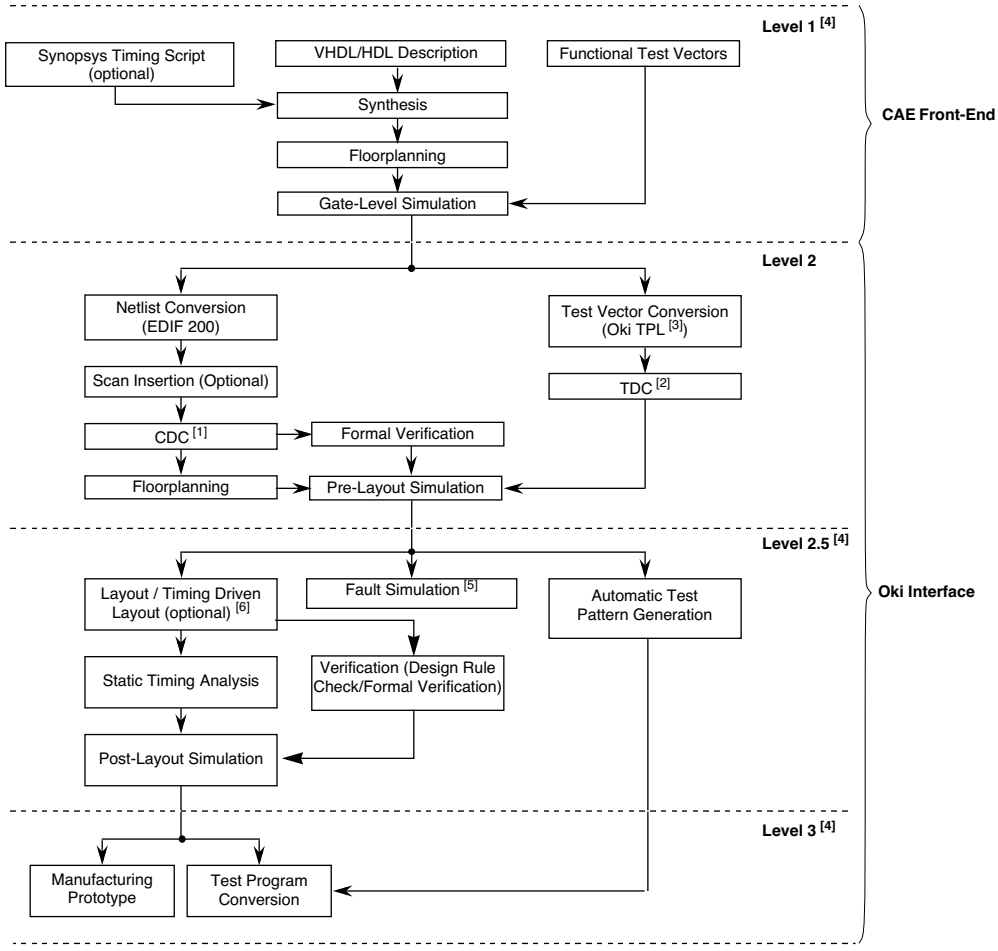
Oki Design Kit Availability

Vendor	Platform	Operating System [1]	Vendor Software/Revision [1]	Description
Cadence	Sun® [2]	Solaris	Ambit Buildgates NC-Verilog™ Verilog XL	Design Synthesis Design Simulation Design Simulation
Syntest	Sun® [2]	Solaris	Turbo Fault	Fault Simulation
Synopsys	Sun® [2]	Solaris	Design Compiler Ultra + Tetramax/ATPG Primetime DFT Compiler/Test Compiler RTL Analyzer VCS	Design synthesis Test Synthesis Static Timing Analysis (STA) Test synthesis RTL check Design Simulation
Model Technology Inc. (MTI)	Sun® [2] NT	Solaris WinNT4.0	MTI-VHDL MTI-Verilog	Design Simulation Design Simulation
Oki	Sun® [2]	Solaris	Floorplanner	Floor planning
Verplex	Sun® [2]	Solaris	Conformal	Formal Verification

1. Contact Oki Application Engineering for current software versions.
2. Sun or Sun-compatible.

Design Process

The following figure illustrates the overall IC design process, also indicating the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki's Circuit Data Check program (CDC) verifies logic design rules
[2] Oki's Test Data Check program (TDC) verifies test vector rules
[3] Oki's Test Pattern Language (TPL)
[4] Alternate Customer-Oki design interfaces available in addition to standard level 2
[5] Standard design process includes fault simulation
[6] Requires Synopsys timing script for Oki timing driven layout

Figure 12. Oki's Design Process

Automatic Test Pattern Generation

Oki's 0.5µm ASIC technologies support Automatic Test Pattern Generation (ATPG) using full scan-path design techniques, including the following:

- Increases fault coverage ≥ 95%
- Uses Synopsys Test Compiler
- Automatically inserts scan structures
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports vector compaction

ATPG methodology is described in detail in Oki's *0.5µm Scan Path Application Note*.

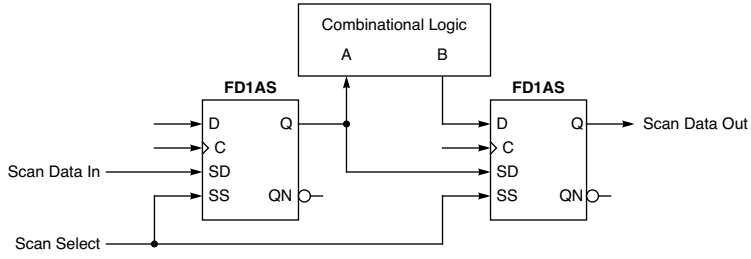


Figure 13. Full Scan Path Configuration

Floorplanning Design Flow

Oki's floorplanner can be classified as both a front-end floorplanner and a back-end floorplanner. During front-end floorplanning, logic designers use the floorplanner to generate two files: a capacitance file for pre-layout simulation, and a floorplanner interface file for layout.

During back-end floorplanning, the layout engineer transfers the floorplanner interface file to Oki's proprietary layout software, code-named Pegasus. The floorplanner interface file contains information about the placement of blocks and groups of blocks. The back-end floorplanner is automated and is transparent to logic designers.

Figure 14 shows a diagram of front-end floorplanning. *Figure 15* shows a diagram of back-end floorplanning.

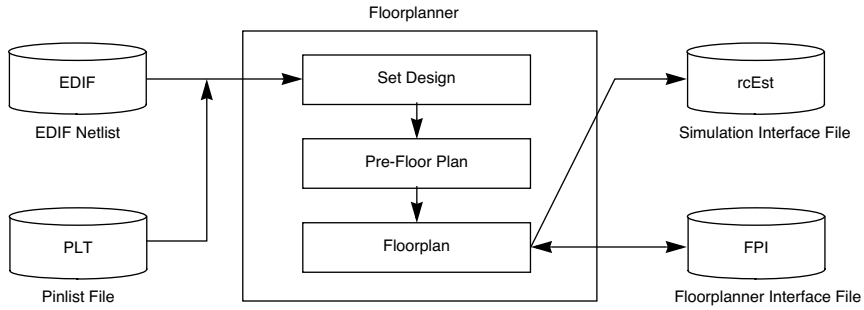


Figure 14. Front-End Floorplanning

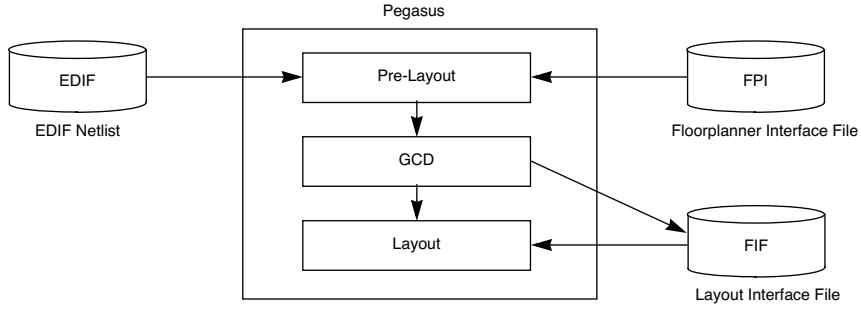


Figure 15. Back-End Floorplanning

IEEE JTAG Boundary Scan Support

Boundary scan offers efficient board-level and chip-level testing capabilities. Benefits resulting from incorporating boundary-scan logic into a design include:

- Improved chip-level and board-level testing and failure diagnostic capabilities
- Support for testing of components with limited probe access
- Easy-to-maintain testability and system self-test capability with on-board software
- Capability to fully isolate and test components on the scan path
- Built-in test logic that can be activated and monitored
- An optional Boundary Scan Identification (ID) Register

Oki's boundary scan methodology meets the JTAG Boundary Scan standard, IEEE 1149.1-1990. Oki supports boundary scan on both Sea of Gates (SOG) and Customer Structured Array (CSA) ASIC technologies. Either the customer or Oki can perform boundary-scan insertion. More information is available in Oki's *JTAG Boundary Scan Application Note.* Contact the Oki Application Engineering Department for interface options.

PACKAGE OPTIONS

MSM30R/32R/92R Package Menu

Product Name MSM92..	SOG		I/O Pads [1]	QFP									TQFP					LQFP			PBGA				FBGA	
	MSM32R	MSM30R		44	64	80	100	128	160	208	240	304	44	64	80	100	128	144	176	208	256	352	420	560	144	224
RB01			80		●	❍	❍						●													
RB02			96	❍	●	❍	❍						●		●											
RB03		0020	104	●	●	❍	❍						●	●	●	●										
RB04			120	❍	●	❍	●						●	●	●	●										
RB05			128	❍	●	❍	❍						●	●	●	●	●									
RB06	0050	0050	144	●	●	❍	●						●	●	●	●	●	●								
RB07			152	●	●	❍	❍						●	●	●	●	●	●								
RB08			160	❍	●	❍	❍						●	●	●	●	●	●								
RB09			168	❍	●	❍	❍		●				●	●	●	●	●	●	❍		●					
RB10	0080	0080	176	❍	●	❍	●	●	●				●	●	●	●	●	●	●		●					
RB11			192	❍	●	❍	❍	●	●				❍	●	●	●		●	●		●					
RB12			200	❍	●	❍	❍	●	●	❍			❍	●	●	●		●	●		●					
RB13	0120	0120	208	❍	●	❍	❍	●	●	●			●	●	●	●		●	●	●	●				●	
RB14			224		●	❍	❍	●	●	●					●	●		●	●	●	●				●	
RB15			240		●	❍	❍	●	●	●	●				●	●		●	●	●	●				●	
RB16	0190	0190	256		●	●	❍	●	●	●	●				●	●		●	●	●	●				●	
RB17			272		●	❍	❍	●	●	●					●	●		●	●	●	●	●			●	●
RB18			288		●	❍	❍	●	❍	●					●	●		●	●	●	●	●			●	●
RB19			304		●	❍	❍	●	❍	●		●				●		●	●	●	●	●			●	●
RB20	0300	0300	320		●	●	❍	●	●	●	●	●				●		●	●	●	●	●	●			●
RB21			336		●	❍	❍	●	❍	●	●	●				●		●	●	●	●	●	●			●
RB22			352			❍	❍	●	●	●	●							●	●	●	●	●	●			●
RB23			368					●	●	●	●							●	●	●	●	●	●			●
RB24		0440	384					●	●	●	●	●						●	●	●	●	●	●			
RB25			400					●	●	●	●							●	●	●	●	●	●			
RB26			416					●	●	❍	●							●	●	●		●	●			
RB27			432						●	●	●							●	●	●		●	●			
RB28			448						●	●								●	●	●		●				
RB29			472					●	❍	●									●	●		●				
RB30			488					●	●	❍									●	●		●				
RB31			504					❍	●	❍	❍	●							●	●		●				
RB32			528						●	●	●	●							●	●				●		
RB33			552																					●		
RB34			576																							
RB35			600																							
RB36			624																							

MSM30R/32R/92R Package Menu (Continued)

Product Name MSM92..	SOG		I/O Pads [1]	QFP									TQFP					LQFP			PBGA				FBGA	
	MSM 32R	MSM 30R		44	64	80	100	128	160	208	240	304	44	64	80	100	128	144	176	208	256	352	420	560	144	224
Body Size (mm)				9x10	14x14	14x20	14x20	28x28	28x28	28x28	32x32	40x40	10x10	10x10	12x12	14x14	14x14	20x20	24x24	28x28	27x27	35x35	35x35	35x35	13x13	15x15
Lead Pitch (mm)				0.8	0.8	0.8	0.65	0.8	0.65	0.5	0.5	0.5	0.8	0.5	0.5	0.5	0.4	0.5	0.5	0.5	1.27	1.27	1.27	1.00	0.8	0.8
Ball Count																					256	352	420	560	144	224
Signal I/O																					231	304	352	400	144	224
Power Balls																					12	16	32	80	-	-
Ground Balls																					13	32	36	80	-	-

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

NOTES

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