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# AK8815/16
# NTSC/PAL Digital Video Encoder

## GENERAL DESCRIPTION

The AK8815/16 is a digital video encoder which is developed for portable apparatus applications such as cellular phone etc.. ITU-R BT.601 level compatible Y, Cb,and Cr signals which correspond to square pixel are encoded into either NTSC or PAL compatible composite video signal. Interface is made in HSYNC-, VSYNC- synchronized slave-mode operation. It is controlled via a 4-wire serial interface.

## FEATURES

- NTSC-M, PAL-B, D, G, H, I encoding
- Composite Video Output
- Y:Cb:Cr 4:2:2 Square Pixel Data Input
- H/V Slave Operation
- Y filtering: 2 x over-sampling
- C filtering: 4 x over-sampling
- 9-bit DAC
- Macrovision Copy Protection Rev. 7.1 * (only AK8815 )
- VBID ( CGMS-A ) Compatible
- WSS Compatible
- On-chip Quartz Crystal Oscillator circuit
- Clock: Square Pixel data rate 24.5454 MHz ( NTSC ), 29.50 MHz ( PAL )
- Device Control I / F : 4- wire Serial Bus Interface
- On-chip Color Bar Output
- Black Burst Output
- Internal Operating Voltage: 2.7 V ~ 3.3 V
- supplying Interface Power Supply ( 1.6 V ~ 2.0 V or 2.7 V ~ 3.3 V )
- Power-down function
- Monolithic CMOS
- 57 pin FBGA ( 5 mm sq ) ( lead-free package )

(*Note) This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per -view use only, unless otherwise authorized in written by Macrovision. Reverse engineering or disassembly is prohibited.


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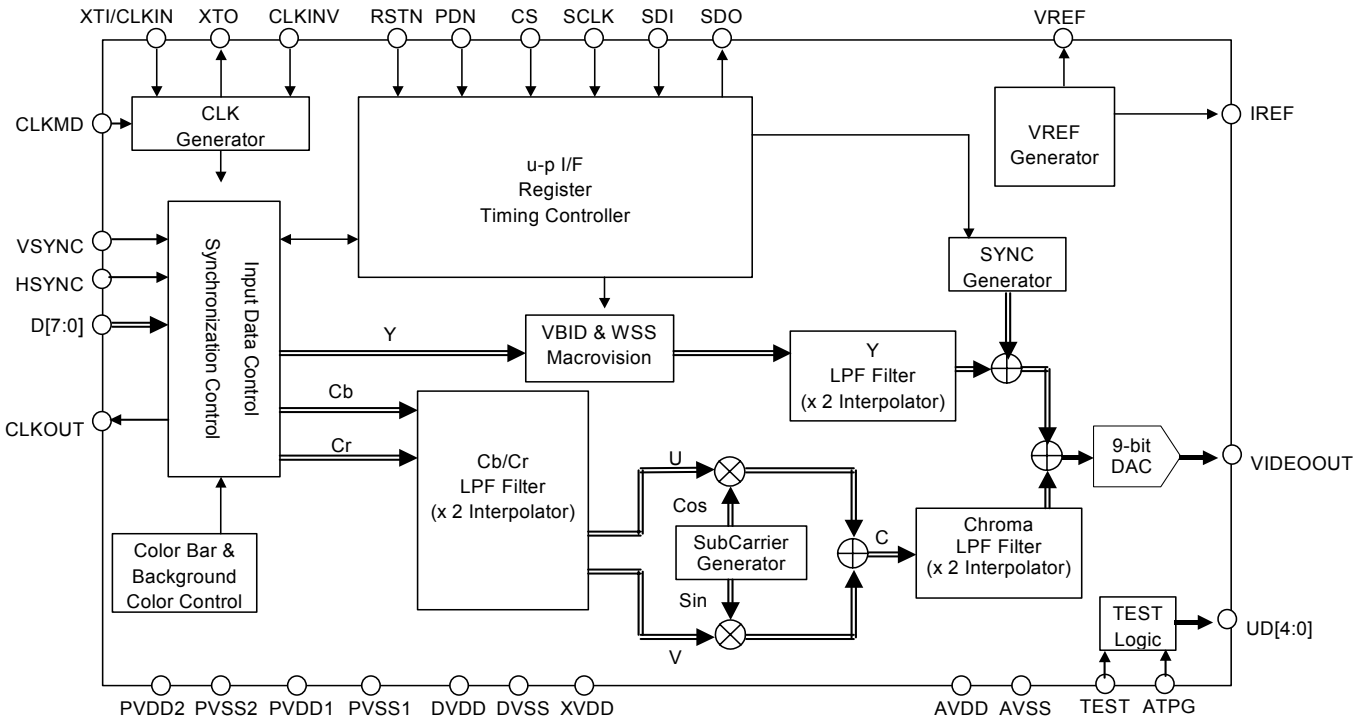
# BLOCK DIAGRAM





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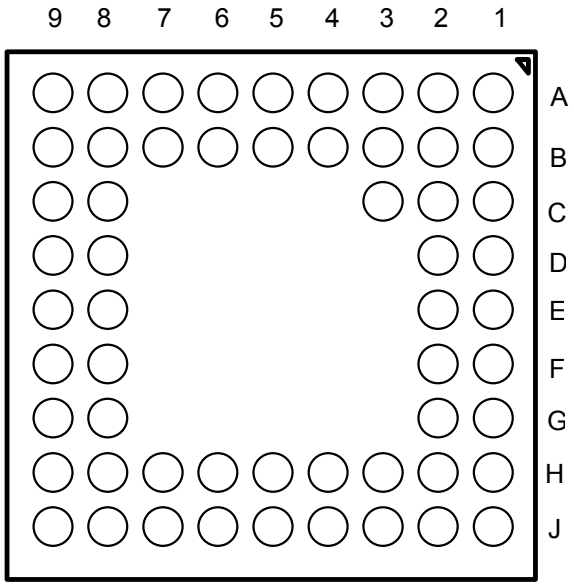
## ORDERING GUIDE

AK8815/16VG 57 pin FBGA

## PIN LAYOUT

57pin FBGA




Bottom View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## PIN FUNCTIONAL DESCRIPTION (preliminary)

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| A7 | XTI/CLKIN | I | Quartz crystal resonator connection pin ( to be grounded via a 18 pF capacitor as shown in the recommended circuit ).<br>NTSC: 24.5454 MHz / PAL: 29.50 MHz<br>Hi-Z input is acceptable to this pin at PDN = L.<br>Input from an external crystal oscillator should be connected to this pin. |
| B6 | XTO | O | Quartz crystal resonator connection pin ( to be grounded via a 22 pF capacitor as shown in the recommended circuit ).<br>NTSC: 25.5454 MHz / PAL: 29.50 MHz<br>DVSS level is output on this pin at PDN = L. |
| B5 | CLKMD | I | Clock Mode setting pin. Should be connected to either DVDD or DGND.<br>GND connection: when a crystal resonator is used<br>XVDD connection: when an external crystal oscillator is used |
| B9 | CLKOUT | O | Clock output pin. NTSC: 24.5454 MHz / PAL: 29.50 MHz<br>This becomes Hi-Z output at PDN =L. |
| B7 | CLKINV | I | “L “ : data is latched with rising edge.<br>“H” : data is latched with falling edge.<br>Internal clock is inverted (internal operation timing edge is inverted. CLKOUT is not affected). Connect to either DVDD or DGND. |
| J6 | PDN | I | Power Down Pin. After returning from PD mode to normal operation, RESET Sequence should be done to AK8815/16.<br>“L “(GND level): Power-down<br>“H “: normal operation |
| J5 | RSTN | I | Reset input pin. In order to initialize the device , an initialization must be made in accordance with the reset sequence.<br>“L “ : reset<br>“H “ : reset<br>Hi-Z input is acceptable to this pin at PDN = L. |
| J4 | SCLK | I | Serial Data clock input pin. 15 MHz ( max )<br>Hi-Z input is acceptable to this pin at PDN = L. |
| H4 | SDI | I | Serial Data input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| H3 | SDO | O | Serial Data output pin.<br>This becomes high output at PDN = L.<br>This pin interfaces one-to-one with a controller through a dedicated pin. |
| H5 | CS | I | Serial Data Chip Enable signal input pin.<br>This pin interfaces one-to-one with a controller through a dedicated pin.<br>L : disabled condition ( un-selected )<br>H : enabled condition ( selected )<br>Hi-Z input is acceptable to this pin at PDN = L. |
| H8 | D7 | I | Data Video Signal input pin (MSB).<br>Hi-Z input is acceptable to this pin at PDN = L. |
| G8 | D6 | I | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| H9 | D5 | I | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| G9 | D4 | I | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| F8 | D3 | I | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| E8 | D2 | I | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| D8 | D1 | I | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| D9 | D0 | I | Data Video Signal input pin (LSB).<br>Hi-Z input is acceptable to this pin at PDN = L. |
| J7 | HSYNC | I | Horizontal SYNC signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| H7 | VSYNC | I | Vertical SYNC signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L. |
| B3 | VREF | O | On-chip VREF output pin. AVSS level is output on this pin at PDN = L.<br>Connect this pin to Analog Ground via a 0.1 uF or larger capacitor. |


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| | | | |
|---|---|---|---|
| A2 | IREF | O | IREF output pin. Connect this pin to Analog ground via a 12 Kohm resistor ( better than +/_ 1% accuracy ). |
| C1 | VIDEOOUT | O | Video output pin. Connect this pin to Analog ground via a 390 ohm resistor resistor ( better than +/_ 1% accuracy ). |
| C2 | AVDD | P | Analog power supply pin. |
| A5 | XVDD | P | Power supply pin for crystal ( for XTAL ). |
| B2 | AVDD | P | Analog power supply pin. |
| B1 | AVSS | G | Analog ground pin. |
| D1 | DVSS | G | Digital ground pin. |
| A6 | DVSS | G | Crystal ground connection pin ( set DVSS [0 V] ). |
| A3 | AVSS | G | Analog ground pin. |
| F1 | DVDD | P | Digital power supply ( digital core power supply ) |
| F9 | DVDD | P | Digital power supply ( digital core power supply ) |
| E2 | DVSS | G | Digital ground pin ( digital core ground ) |
| E9 | DVSS | G | Digital ground pin ( digital core ground ) |
| | | | |
| C8 | PVDD1 | P | Power supply pin for chip pad.<br>I / F power supply for CLKOUT, D[7:0], HSYNC, VSYNC |
| C9 | PVSS1 | G | Ground pin for PVDD1 |
| J3 | PVDD2 | P | Power supply pin for chip pad.<br>I / F power supply for PDN, RSTN, SDO, SDI, CS, SCLK. |
| H2 | PVSS2 | G | Ground pin for PVDD2 |
| A4 | AVSS | G | Ground pin for the substrate biasing<br>Connect to Analog Ground. |
| | | | |
| B8 | TEST | I | For normal operation, connect to ground. |
| A8 | ATPG | I | For normal operation, connect to ground. |
| | | | |
| H1 | DVDD | P | Digital power supply |
| | | | |
| J2 | UD4 | O | Test output pin. For normal operation, left un-connected ( NC ). |
| G1 | UD3 | O | Test output pin. For normal operation, left un-connected ( NC ). |
| G2 | UD2 | O | Test output pin. For normal operation, left un-connected ( NC ). |
| E1 | UD1 | I/O | Test I/O pin. For normal operation, left un-connected ( NC ). |
| D2 | UD0 | I/O | Test I/O pin. For normal operation, left un-connected ( NC ). |
| | | | |
| A1 | NC | - | NC pin. |
| A9 | NC | - | NC pin. |
| J1 | NC | - | NC pin. |
| J9 | NC | - | NC pin. |
| B4 | NC | - | NC pin |
| H6 | NC | - | NC pin. |
| J8 | NC | - | NC pin. |
| F2 | NC | - | NC pin. |
| C3 | N.C. | - | Index pin |


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# ELECTRICAL CHARACTERISTICS

(1)Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply voltage (VDD) (Note1)<br>DVDD, XVDD,AVDD, PVDD1, PVDD2 | -0.3 | 4.6 | V |
| Input pin voltage (Vin) | -0.3 | VDD+0.3 | V |
| Input pin current (Iin) (Note2) | - | +/- 10 | mA |
| Storage temperature | -40 | +125 | °C |

(Note1)
When each ground pin ( DVSS, AVSS, PVSS1, PVSS2 ) is at 0 V ( voltage reference ).
In this specification, PVDD1 and PVDD2 are expressed as PVDD ( as a general comment ) hereafter.
Similarly, DVDD, XVDD are expressed as DVCC, and AVDD and AVDD as AVDD.
Each ground pin is always kept to the same reference voltage, 0 V with no potential difference.
(Note2)
Exclude Power supply pin.

(2) Recommended Operating Conditions

| Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|
| Power supply (DVDD = AVDD )<br>(Note1 ) | 2.7 | 3.0 | 3.3 | V |
| Interface power supply (Note2)<br>(PVDD = DVCC ) at 3.0 V I/F | 2.7 | .3.0 | 3.3 | V |
| Interface power supply<br>(PVDD1, 2 ) at 1.8 V I/F | 1.6 | 1.8 | 2.0 | V |
| Operating temperature (Ta) | -20 | 25 | *85* | °C |

Note 1) excluding interface power supply. 1.8 V power supply can be supplied only to the interface part.
Note 2) interface power supplies PVDD1, PVDD2 can be used as 3 V or 1.8 V power supply interface each.
But when the 1.8 V interface is not selected, same potential as DVCC is used as interface power supply.
(Example PVDD1 = 1.8 V, PVDD2 = DVDD = 3 V)
Note 3) as described at the note in item ( 1 ) above, PVDD1 and PVDD2 are expressed as PVDD in this table. Similarly, DVDD and XVDD are expressed as DVCC, and AVDD and AVDD as AVDD.

(3) DC Characteristics

[Operating voltages : DVDD 2.7 V ~ 3.3V / PVDD 2.7 V ~ 3.3 V / PVDD 1.6 V ~ 2.0 V, Temperature : -20 ~ 85°C]

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Digital input H voltage | VIH1 | 0.7PVDD | | | V | *PVDD = 3.0V* |
| | VIH2 | 0.8PVDD | | | | *PVDD = 1.8V* |
| Digital input L voltage | VIL1 | | | 0.3PVDD | V | *PVDD = 3.0V* |
| | VIL2 | | | 0.2PVDD | | *PVDD = 1.8V* |
| Digital input leakage current | IL | | | +/- 10 | uA | |
| Digital output H voltage ( excluding XTO ) | VOH1 | 2.2 | | | V | *IOH= 1mA*<br>I/O 3.0V |
| | VOH2 | 1.3 | | | | *IOH= 600uA*<br>I/O 1.8V |
| Digital output L voltage ( excluding XTO ) | VOL1 | | | 0.4 | V | IOL= 2m*A*<br>I/O 3.0V |
| | VOL2 | | | 0.4 | V | IOL= 1m*A*<br>I/O 1.8V |


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(4) Analog Characteristics

[Operating voltage : AVDD = DVCC=2.7 - 3.3 V, Temperature: -20 - 85°C]

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Resolution | | 9 | | bit | |
| Integral non-linearity ( error ) | | +/- 0.6 | +/- 2.0 | LSB | |
| Differential non-linearity ( error ) | | +/- 0.4 | +/- 1.0 | LSB | |
| Output full scale voltage | 1.21 | 1.28 | 1.35 | V | Note1) |
| Output offset voltage | | | 5.0 | mV | Note2) |
| On-chip reference voltage | 1.17 | 1.23 | 1.30 | V | |
| Reference voltage drift | | -50 | | ppm/°C | |

Note1) values are when a 390 ohm output load, a 12 Kohm IREF pin resistor and on-chip VREF are used. Full scale output current is calculated as Iout = full scale output voltage ( typ. 1.28 V ) / 390 ohm = typ. 3.28 mA.
Note2) A voltage referenced to VSS when a decimal zero voltage is input to DAC.

(5) Power Consumption

[Operating voltage : AVDD = DVCC=2.7 - 3.3 V, Temperature: -20 - 85°C]

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Total power consumption | | 24 | 36 | mA | Note3) |
| Power-down current 1 | | 10 | 100 | uA | Note4) |
| Power-down current 2 | | 1 | 10 | uA | Note5) |
| XTAL part current | | 2.0 | 3.3 | mA | Note6) |
| Analog part operating current 1 | | 6.5 | | mA | Note7) |
| Analog part operating current 2 | | 1.6 | | μA | Note8) |

Note3) NTSC mode on-chip color bar output is enabled and DAC is " on " ( no external output loads are connected , other than those recommended, connecting-components ).
Note4) measuring conditions :
input / output settings after power-down sequence are, PDN pin is at GND level, CLKOUT and SDO output are at high level ( power supply voltage ) with no external connection, input voltage on those input pins is 1/2 level of power supply which are set to accept Hi-Z input at power-down, and TEST = ATPG = GND ( or left open ).
Power supplies are AVDD = DVCC = PVDD.
Each ground pin ( DVSS, AVSS1, AVSS2, PVSS1, PVSS2 ) is always 0 V ( voltage reference ).
Note5) measuring conditions :
set AVDD = DVCC = 0 V ( potential difference with voltage reference ground is 0 V ) in power-down current 1 condition.Set those input pins to GND level which are set to accept Hi-Z input at power-down.
Power-down current 2 is PVDD power supply current at PVDD = 1.6 V ~ 1.8 V or 2.7 V ~ 3.3 V.
Note6) at RSTN = H, PDN = H
Note7) when DAC output is " ON ".
Note8) when DAC output is " OFF ".


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## (6) Crystal Oscillator Circuit Part

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Crystal resonator and externally connecting load capacitance

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Oscillating frequency | f0 | | 24.5454<br>29.5000 | | [MHz] | |
| frequency accuracy | Δf/f | | | +/-50 | [ppm] | |
| load capacitance | CL | | 15 | | [pF] | |
| effective equivalent resistance | Re | | | 100 | [Ω] | Note1) |
| parallel capacitance | C0 | | | 0.85 | [pF] | |
| externally connecting load capacitance on XTLI pin | CXI | | 18 | | [pF] | |
| externally connecting load capacitance on XTLO pin | CXO | | 22 | | [pF] | |

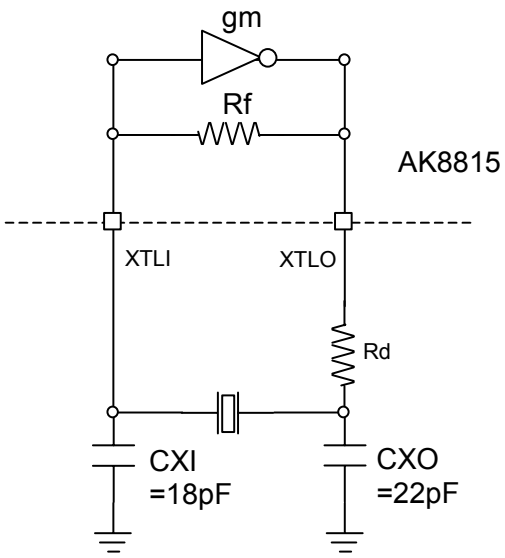
Note 1 ) effective equivalent resistance is generally given as

Re = R1 x ( 1 + CO / CL ) square

Where R1 : equivalent series resistance of crystal resonator

CO : parallel capacitance of crystal resonator

Circuit connection example




rd: Please refer the X'tal specification



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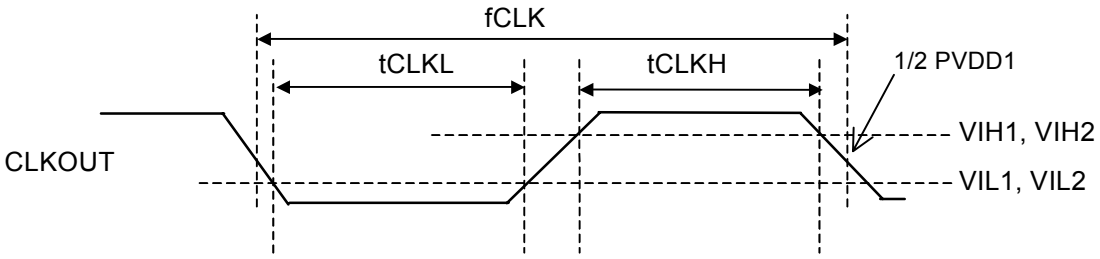
## AC TIMING

( PVDD = 2.7 V ~ 3.3 V / PVDD = 1.6 V ~ 2.0 V, Temperature : –20 ~ 85°C)
loading condition : CL = 30 pF ( at 3.0 V I/F )
CL = 15 pF ( at 1.8 V I/F )

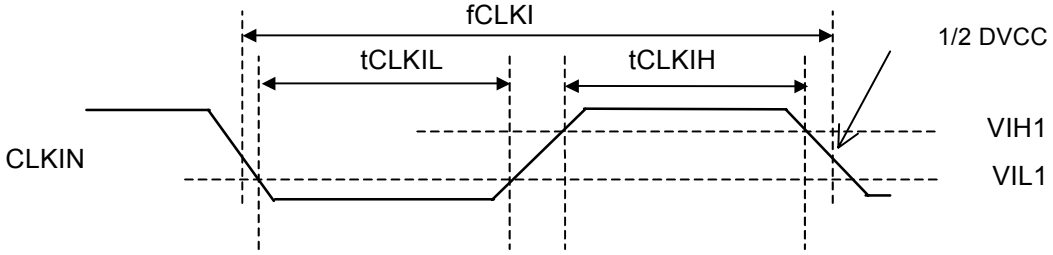
(1) CLK
( 1-1 ) CLKMD = DVSS : when a crystal resonator is connected ( +/_ 50 ppm )




| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| CLKOUT | fCLKO | | 24.5454 | | MHz | NTSC |
| | | | 29.500 | | | PAL |

tCLKIL, tCLKIH : minimum pulse width 10 nS guaranteed by design

External input clock AC timing ( DVCC = 2.7 V ~ 3.3 V : -20 ~ 85 °C )
( 1-2 ) CLKMMD = XVDD : when an external clock source is input ( +/_ 50 ppm )




| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| CLKIN | fCLKI | | 24.5454 | | MHz | NTSC |
| | | | 29.50 | | | PAL |
| CLKIN Duty | pCLKID | 40 | | 60 | % | |

tCLKIL, tCLKIH : minimum pulse width 12 nS ( tr / tf = < 2 nS at 10 % - 90 % level of power supply )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(2) Pixel Data Input Timing
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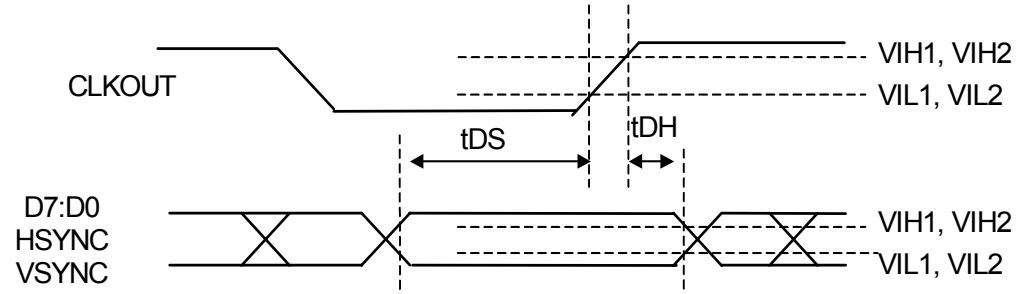


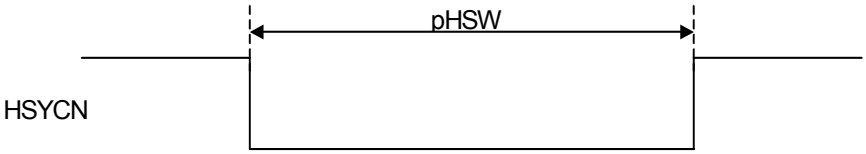

CLKINV = Low, -20 ~ 85 °C ( loading condition : CL = 30 pF at 3 V I/F / 15 pF at 1.8 V I/F )

| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Data Setup Time | tDS | 8 | | | nsec | |
| Data Hold Time | tDH | 5 | | | nsec | |

above values are specified at the AK8815/16 device pin terminal and do not include interconnection delays of pc board etc..

When CLKINV = High, similar tDS and tDH are specified at the falling edge of CLKOUT.

(3) HSYNC pulse width




| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| HSYNC Pulse Width | pHSW | 15 | 115/16 | | CLKs | NTSC (24.5454MHz) |
| | | 15 | 139 | | | PAL (29.50MHz) |

* typical values are calculated by converting the HSYNC pulse width of Analog Video specification into number of system clock pulses.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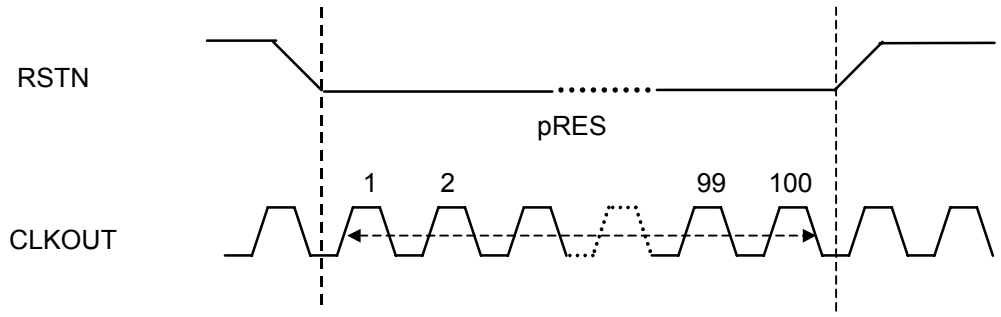
(4) Reset

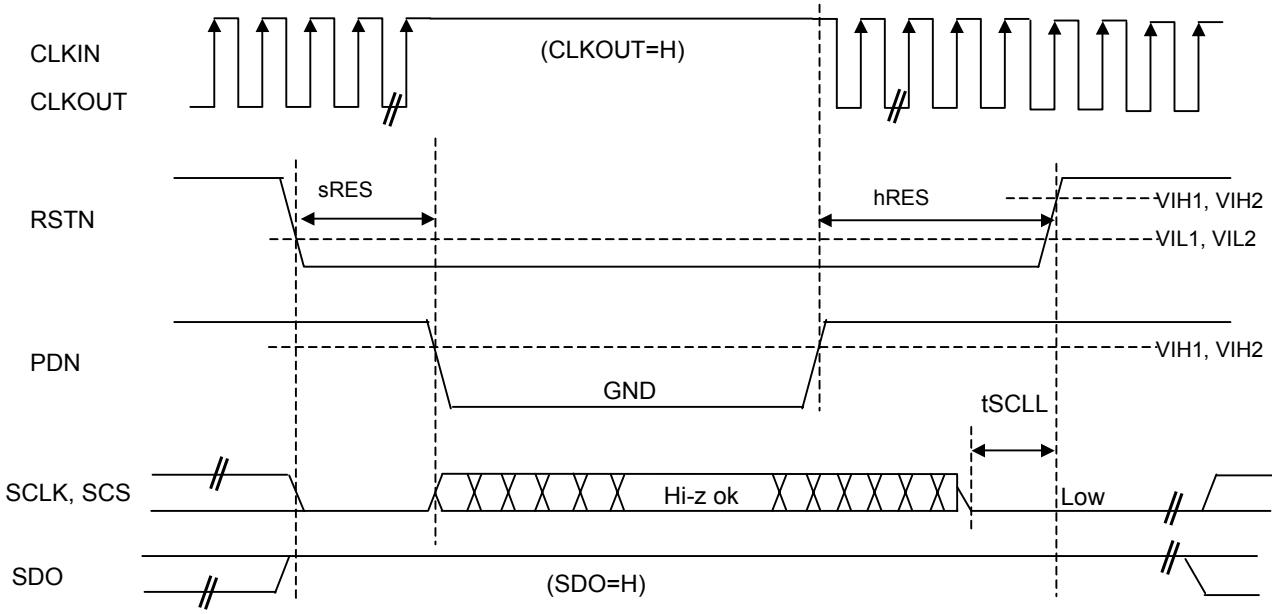
(4-1) Reset Timing




| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| RSTN Pulse Width | pRES | 100 | | | SYSCLK |

(4-2) Power Down Sequence / Reset Sequence

Before PDN setting ( PDN to low ), Reset must be enabled for a duration of longer-than-100 clock time. After PDN release ( PDN to high ), Reset must be enabled for 10 mS or longer till analog part reference voltage & current are stabilized.




| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| RSTN Pulse Width | sRES | 100 | | | SYSCLK |
| Time from PDN to high to RSTN to high | hRES | 10 | | | msec |
| SCL low duration before RSTN to rise | tSCLL | 50 | | | nsec |

at power-down, all control signals must surely be set to either power supply or ground level of the selected power supply, and not to ViH / ViL levels.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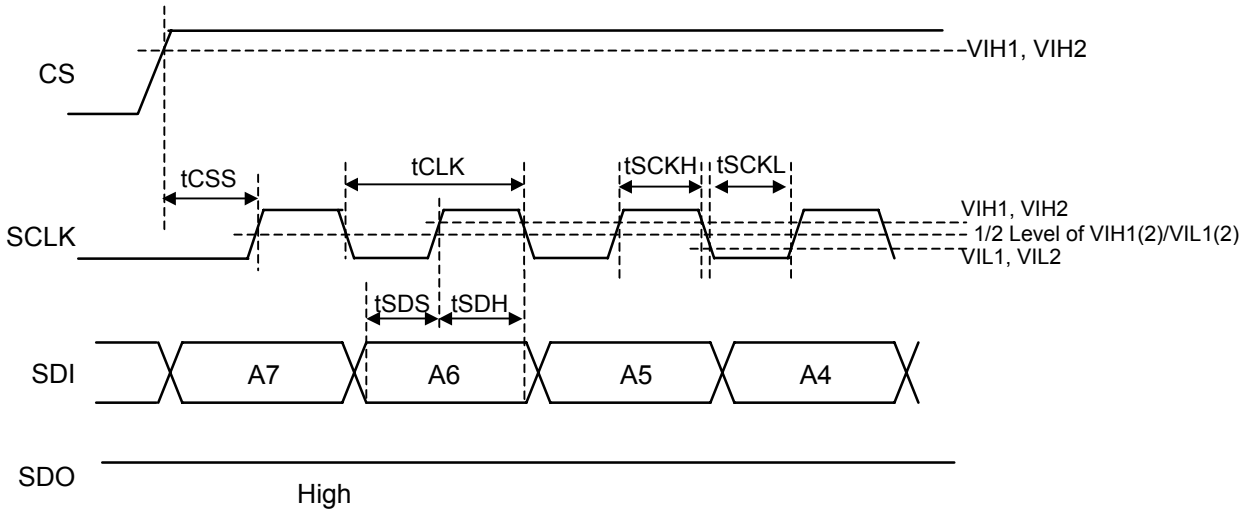
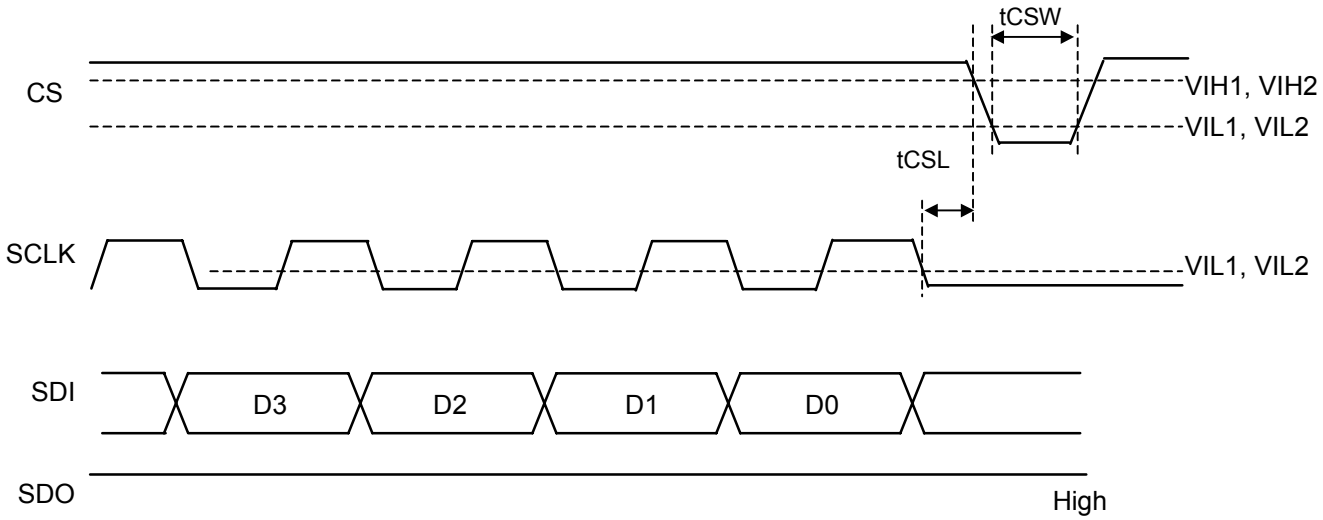
( 5 ) Serial I / F Timing waveform

( 5-1 ) Write / Read data input timing




( 5-2 ) Write data input timing





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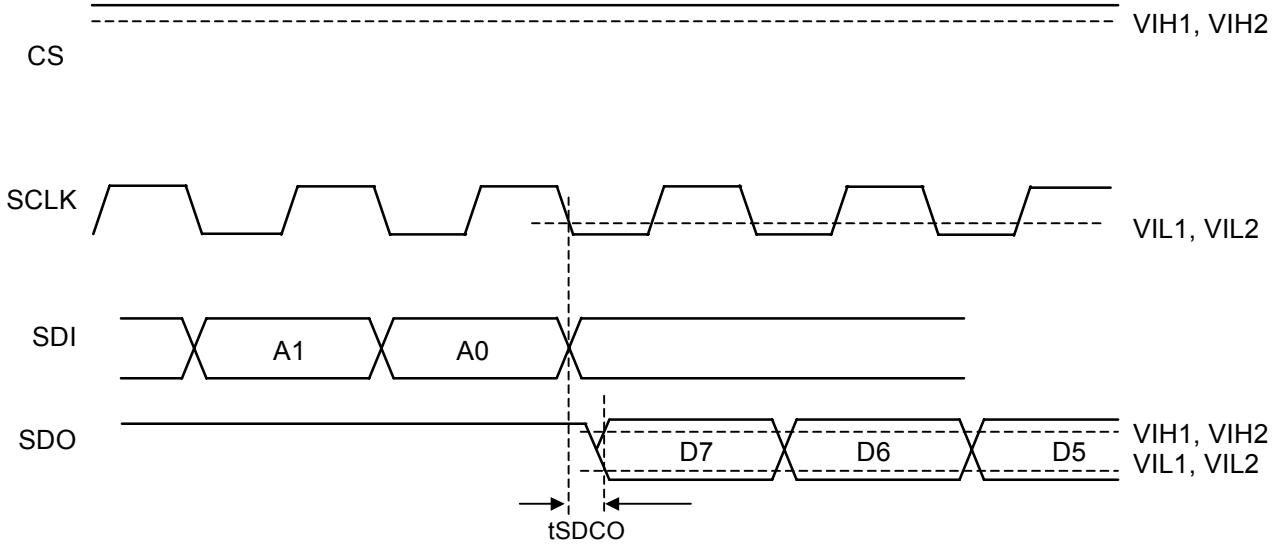
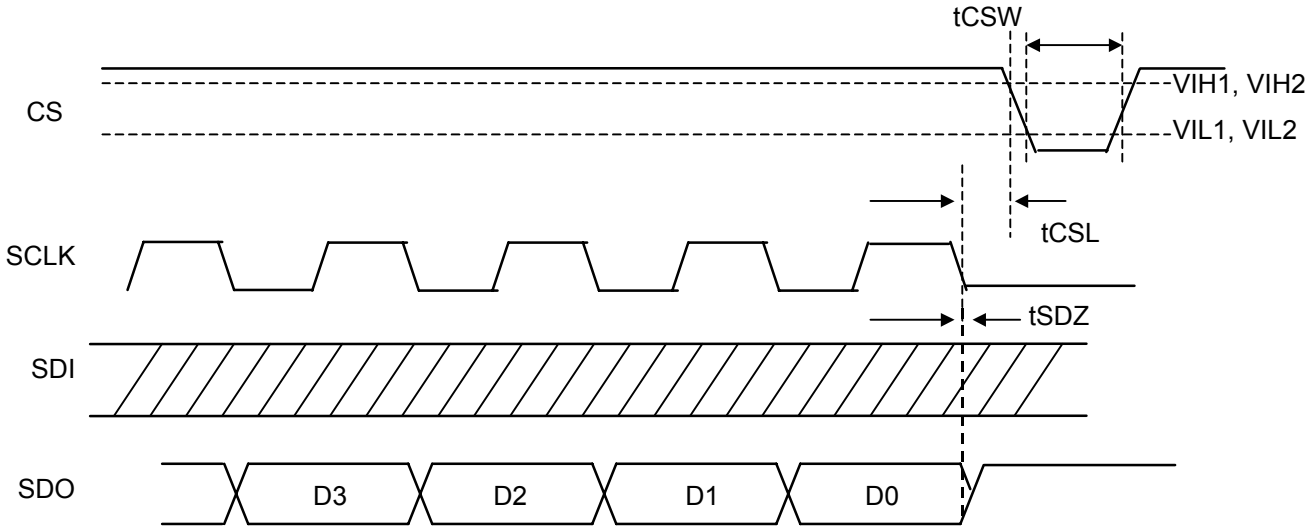
( 5-3 ) Read data output timing




( 5-4 ) Read data output timing 2




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Time from CS to high to SCLK to high | tCSS | 20 | | | nsec |
| SCLK Frequency | tCLK | | | 15 | MHz |
| SCLK “high” duration | tSCKH | 26 | | | nsec |
| SCLK “low” duration | tSCKL | 26 | | | nsec |
| Data set-up time | tSDS | 15 | | | nsec |
| Data hold time | tSDH | 10 | | | nsec |
| Time from 15/16$^{th}$ SCLK to low to CS to low | tCSL | 20 | | | nsec |
| CS “low” duration | tCSW | 60 | | | nsec |
| SDO output delay time | tSDCO | | | 20 | nsec |
| SDO output hold time | tSDH | 0 | | | nsec |

When to execute sequential write/read to/from register, CS must be kept to low once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# FUNCTIONAL OUTLINE

( 1 ) Reset
( 1-1 ) Reset of Serial Interface part ( asynchronous reset )
Reset is made by setting RSTN pin to low.
( 1-2 ) Reset of other than Serial Interface blocks
Reset is made by keeping RSTN pin low for a longer than 100 clock time, in normal operation.
( 1-3 ) at Power-On-Reset ( including power-down release case )
Follow the power-on-reset sequence.
At the completion of each initialization, all internal registers are set to default values ( refer to Register Map ).
Right after the reset, Video output of the AK8815/16 is put into Hi-Z condition.

( 2 ) Power-Down
It is possible to put the device into power-down mode by setting the AK8815/16 power-down pin to GND.
Transition to power-down mode should be followed by the power-down sequence. As for the recover from the power-down mode, it should be followed by the power-down release sequence.

( 3 ) Master Clock
As a master clock of the AK8815/16, either a crystal resonator or a crystal oscillator can be used. Either of the operation mode ( a crystal resonator or a crystal oscillator ) is selected by CLKMD pin.
Crystal resonator mode : CLKMD DVSS
Crystal oscillator mode : CLKMD XVDD

When a crystal resonator is used, connect a resonator between XTI pin and XTO pin.
An oscillating frequency to be used differs in NTSC encoding operation and in PAL encoding operation.
A clock frequency to be used is as follows :
in NTSC encoding operation : 24.5454 MHz
in PAL encoding operation : 29.50 MHz
When a crystal oscillator is used, connect it to XTI pin.
When CLKINV = L, same rising clock as CLKOUT rise is used as an internal encoder clock, but when CLKINV = H,
internal encoder is operated by using an inverted clock.
Even when CLKINV is altered, clock phase of CLKOUT is not changed.

( 4 ) Video Signal Interface
Video input signal ( data ) is processed in slave operation mode which is synchronized with HSYNC / VSYNC.
When CLKINV = DVSS, external input is latched at the rising edge of clock

( 5 ) Pixel Data
Input data to the AK8815/16 is YCbCr ( 4:2:2 ).
Data with Y : 15/16 ~ 235 and CbCr : 15/16 ~ 240 should be input.

( 6 ) Video Signal Conversion
Video Re-Composition module converts the multiplexed data ( ITU-R BT.601 Level Y, Cb, Cr ) into interlaced NTSC-M and PAL-B, D, G, H, I data. Video encoding setting is done by " Mode Register ".


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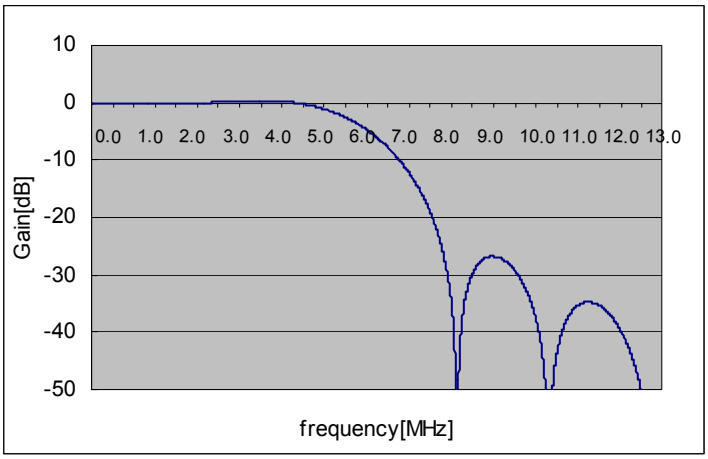
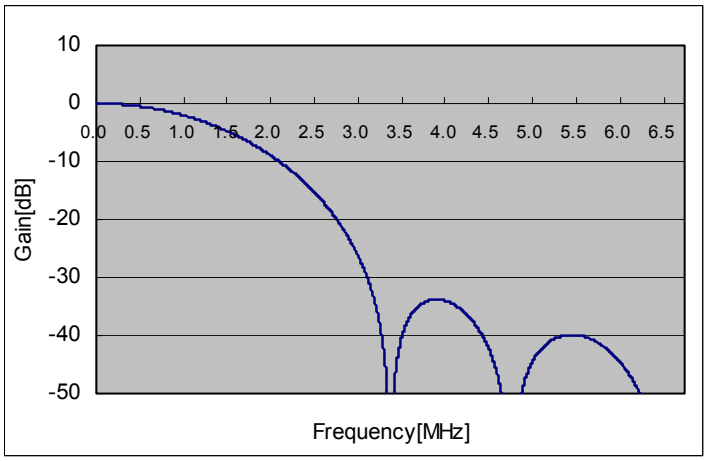
( 7 ) Luminance Signal Filter ( Luma Filter )
Luminance signal is output via LPF ( see x2 Luma Filter in the block diagram ).

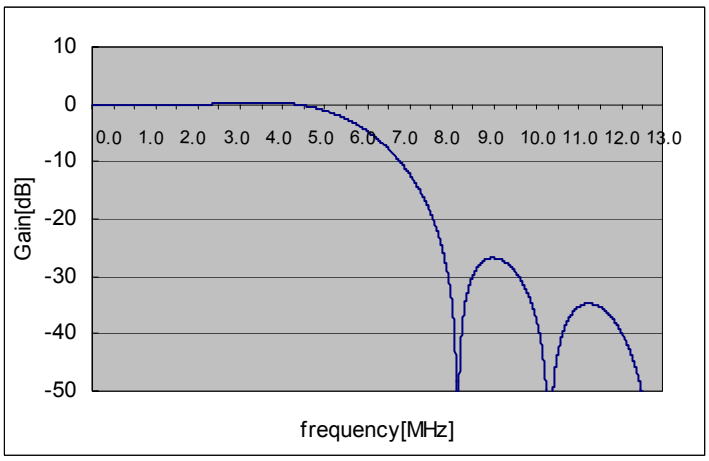



( 8 ) Chroma Signal Filter ( Chroma Filter )
Chroma input signal components ( Cb, Cr ) prior to the modulation go through a 1.3 MHz Band Limiting Filter ( see 4:2:2 to 4:4:4 x2 interpolator in the block diagram ).
Chroma signal which is modulated by the sub-carrier is output via a low pass filter ( Chroma LPF in the block diagram ).
Frequency response of each filter is shown below.

4:2:2 to 4:4:4 Interpolator Filter




x 2 Interpolator Filter





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( 9 ) Color Burst Signal

Burst signal is generated by a 32 bit digital frequency synthesizer.
Color Burst Frequency is selected by mode setting of NTSC / PAL.

| Standerd | Subcarrier Freq (MHz) | Video Process 1 VMOD-bit |
|---|---|---|
| NTSC-M | 3.57954545 | 0 |
| PAL-B,D,G,H,I | 4.43361875 | 1 |

Burst Signal Table

( 10 ) Video DAC

The AK8815/16 has a 9 Bit resolution, current-drive DAC as a video DAC which runs at 29.5 / 24.5454 MHz clock frequency.
This DAC is designed to output 1.28 V o-p at full scale under the following conditions –
loading resistance of 390 ohms, VREF at 1.23 V and IREF pin resistor of 12 Kohms.
Here IREF pin resistor means a resistor connected between [ IREF ] pin and ground. DAC output voltage can be adjusted by adjusting IREF pin resistor.
[ VREF ] pin should be connected to ground via a 0.1 uF or larger capacitor.
DAC output can be turned “ON” or “OFF” by register setting and current consumption can be lowered.
When the output is turned off, it is put into high impedance condition.
On-chip VREF circuit is kept active and only the DAC output is turned off then.


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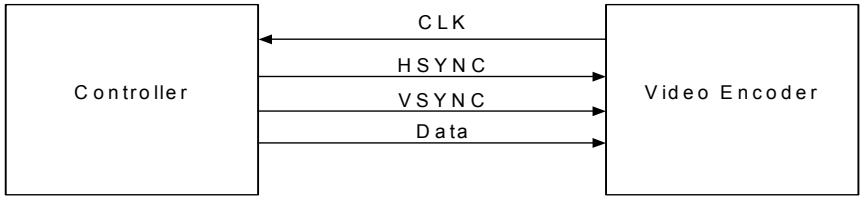
( 11 ) Video Data Interface timing
( 1-1 ) Video interface
The AK8815/16 operates in slave mode which is synchronized with the HSYNC / VSYNC sync signals.

A system operational outline is as follows –
Operation clock of the controller device which feeds data to the video encoder is fed from the video encoder. And such timing signals as HSYNC and VSYNC of the controller are generated by the same clock timing.
The AK8815/16 synchronizes its operation with the generated HSYNC and VSYNC signals.




In normal operation, the AK8815/16 checks HSYNC and VSYNC changes at each CLK edge ( CLK synchronized ).
A Pixel when HSYNC is identified to get low is recognized to be H0 ( zero ), and the 236$^{th}$ data ( NTSC ) or the 310$^{th}$ data ( PAL ) is taken as Cb0 square pixel data.
Video field is recognized by VSYNC relation over HSYNC.
Field recognition is made as follows :
The AK8815/16 distinguishes at every Field if it is Odd Field ( 1$^{st}$ Field ) or not. Even Field Sync signal is not usually
input.

1 ) When VSYNC timing pulse signal fed to the AK8815/16 becomes low from high while HSYNC input signal is at low, this Field is interpreted as Odd Field.
The Horizontal line where Odd Field identification is made, functions as Line 4 in NTSC mode and Line 1 in PAL mode ( even when both VSYNC and HSYNC are identified to get low simultaneously, it is processed as Odd Field. But it is recommended to input those signals with more than a few clock margin ).

2 ) The AK8815/16 continues operation in self-running mode , based on the sync signals which are fed just before, if Horizontal / Vertical Sync signals are not fed every time in such timing and pulse count as expected in the Video Standard Specifications.
But it is recommended to input those sync signals in the specified timing every time in order to prevent erroneous operation.

3 ) All other VSYNC than those identified to be Odd Field are processed as Even Field.
But a use of VSYNC pulse other than in ODD Field synchronization is not assumed for normal operation.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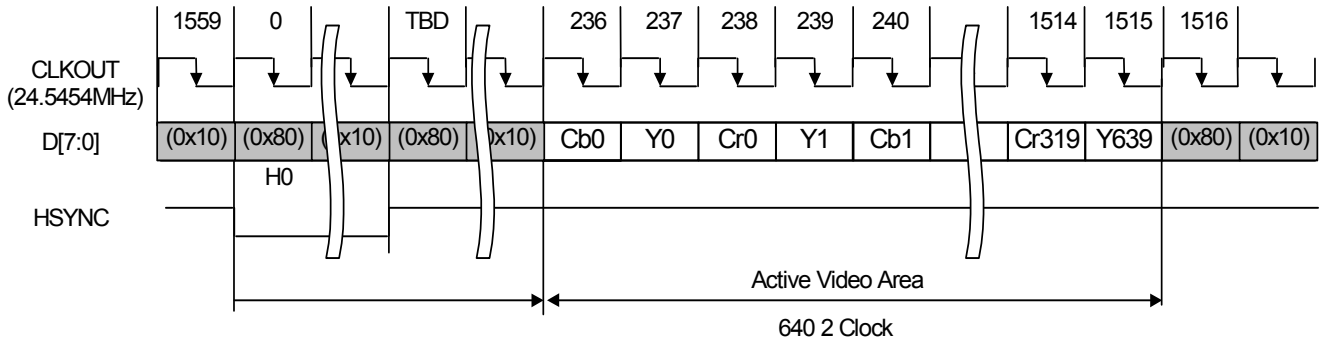
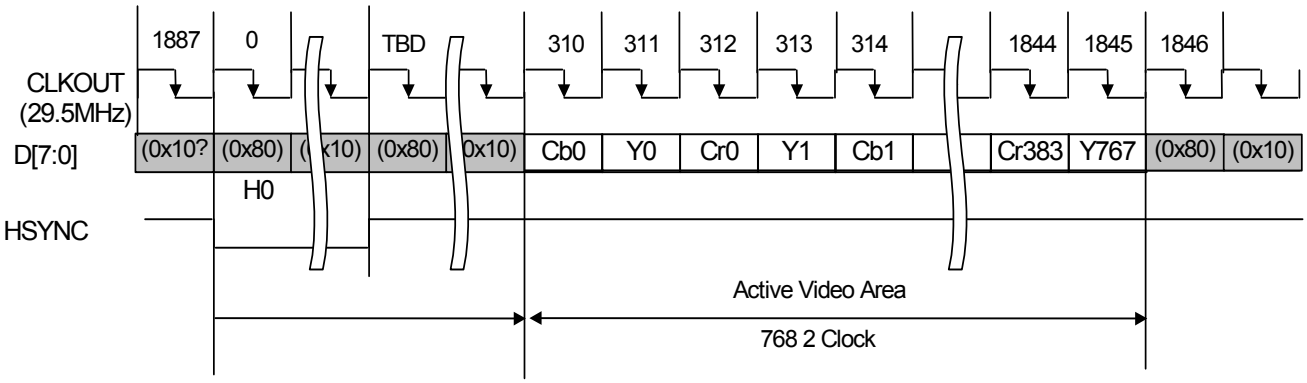
( 1- 2 ) Pixel Data in each line
( 1 ) NTSC




* ) when D [7:0], HSYNC and CLKOUT are in same phase relation as a timing example above, the AK8815/16 takes input data at the falling edge of each CLKOUT if CLKINV = H.
* ) as an input data other than during active video period, Black level ( C / Y = 0x80 / 0x10 ) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

(2) PAL




* ) when D [7:0], HSYNC and CLKOUT are in same phase relation as a timing example above, the AK8815/16 takes input data at the falling edge of each CLKOUT if INV = H.
* ) as an input data other than during active video period, Black level ( C / Y = 0x80 / 0x10 ) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.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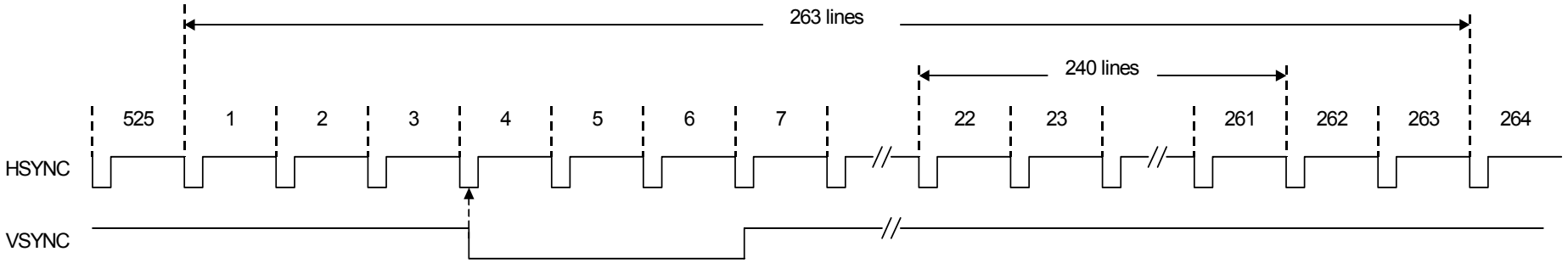
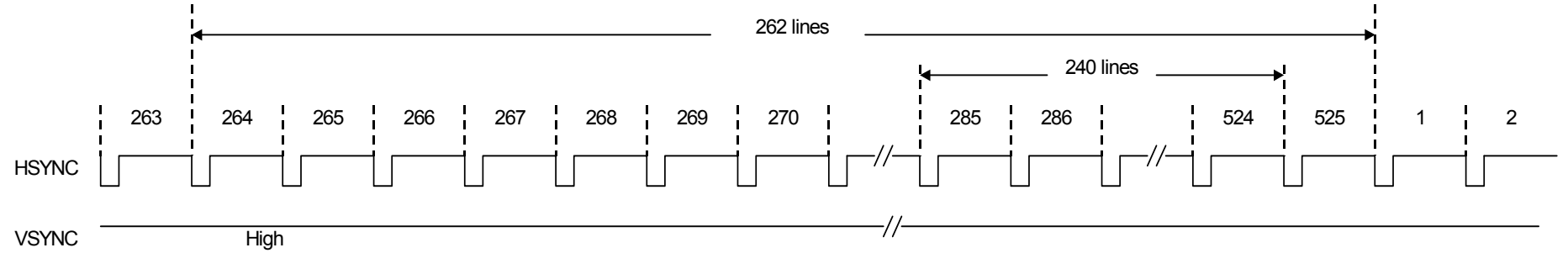
( 1-3 ) HSYNC and VSYNC relation in each Frame
( 1 ) NTSC ( Frame ) 525 Line 480 active lines

The First Field ( ODD )




* ) VSYNC negative-going occurs during HSYNC = L at Line 4.
VSYNC positive-going can occurs at arbitrary location, but keep VSYNC low for 3 line duration time as a rough idea.

The Second Field ( EVEN )




* ) VSYNC negative-going is not required for the Second Field. It is required for the First Field only.

When VSYNC is input in the specified timing (described below ) at the Second Field, the line and the field are set once as the Second Field.
But since the Burst cycle etc. is referenced to the First Field, VSYNC synchronization
cannot be made with the Second Field only. System synchronization must be made to reference the VSYNC synchronization at the First Field.
When to input VSYNC at the Second Field, it should be done after the first 1/2 H of the 266$^{th}$ Line and before the falling edge of the 267$^{th}$ HSYNC ( if HSYNC falling edge timing of the 266$^{th}$ Line is counted as the 0$^{th}$ clock, VSYNC should be fallen after the 780$^{th}$ Clock and before the 1559$^{th}$ Clock ).

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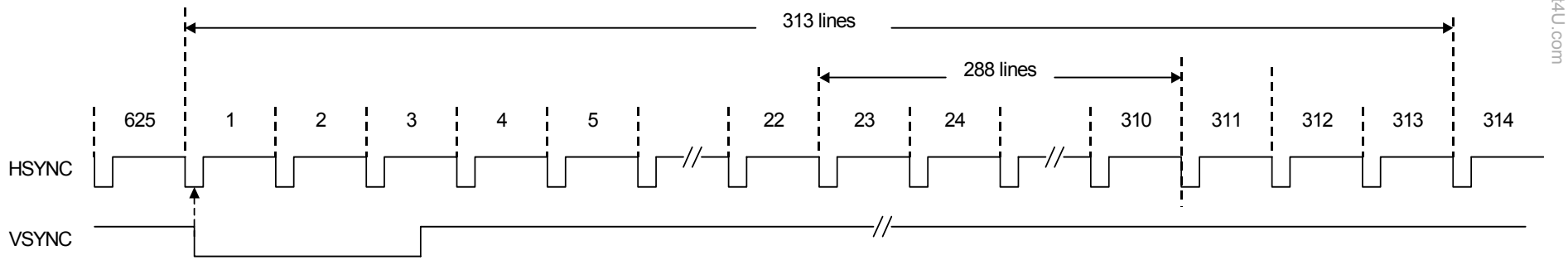
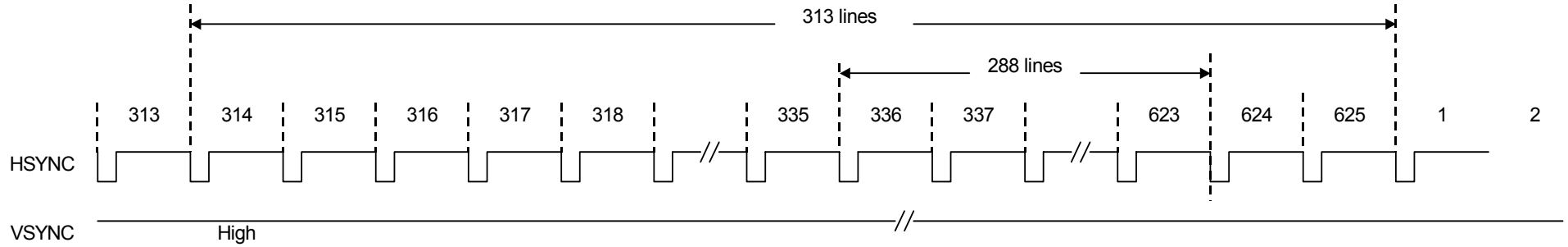
( 2 ) PAL ( Frame ) 625 Line 576 active lines
The First Field ( ODD )




* ) VSYNC negative-going occurs during HSYNC = L at Line 1.
VSYNC positive-going can occur at arbitrary location, but as a rough idea, keep VSYNC low for 2.5, or 2 or 3 line duration time.

The Second Field ( EVEN )




* ) VSYNC negative-going is not required for the Second Field. It is required for the First Field only.

When VSYNC is input in the specified timing (described below) at the Second Field, the line and the field are set once as the Second Field.
But since the Burst cycle etc. is referenced to the First Field, VSYNC synchronization cannot be made at the Second Field only.
System synchronization must be made to reference the VSYNC synchronization at the First Field.
When to input VSYNC at the Second Field, it should be done after the first 1/2 H of the 313$^{th}$ Line and before the falling edge of the 314$^{th}$ HSYNC ( if HSYNC falling edge timing of the 313$^{th}$ line is counted as the 0$^{th}$ clock, VSYNC should be fallen after the 944$^{th}$ clock and before the 1887$^{th}$ clock ).

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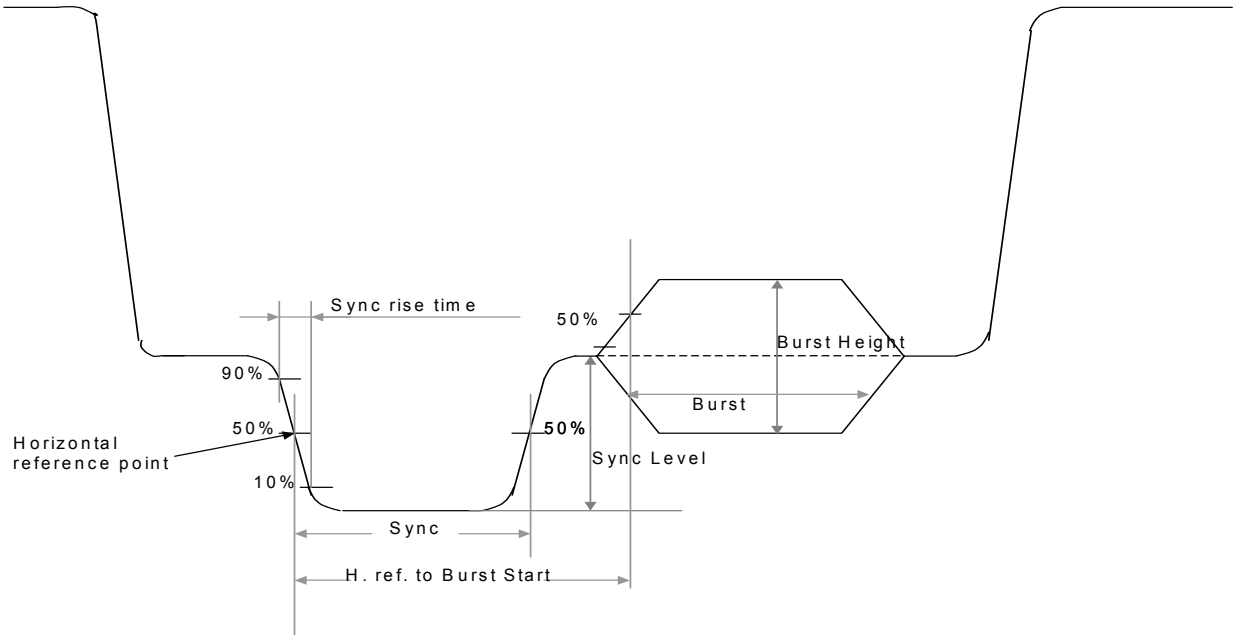
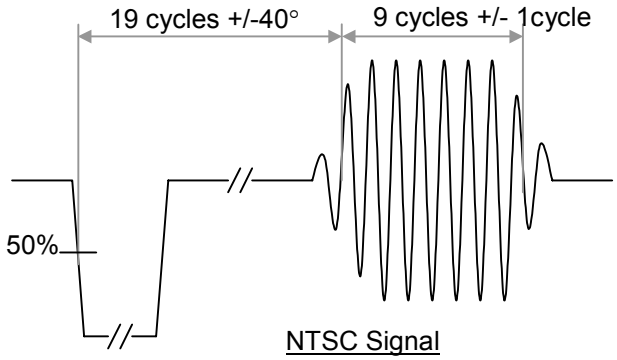
( 2-1 ) SYNC Signal waveform, Burst Waveform generator
( 2-1-1 ) NTSC-J




| | measurement point | value | Consumer Quality tolerance | units |
|---|---|---|---|---|
| Total line period(derived) | | 63.556 | | usec |
| Sync Level | | 40 | +/- 3 | IRE |
| Sync rise time | 10% - 90% | 140 | Max 250 | nsec |
| Horizontal Sync width | 50% | 4.7 | +/- 0.1 | usec |
| Horizontal reference point to burst start | 50% | 19 | defined by SC/H | cycles |
| Burst * | 50% | 9 | +/- 1 | cycles |
| Burst Height ** | | 40 | +/- 3 | IRE |

* there is a case where tolerance of Sync rise time is added to Sync width tolerance.

* Measurement of Burst time length is made between the Burst start point which is defined as the zero-cross point, preceding the first half-cycle of the sub-carrier where Burst amplitude becomes higher than 50 % level and the Burst end point, defined in the same manner.





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( 2-1-2 ) Vertical Sync Signal timing ( NTSC )
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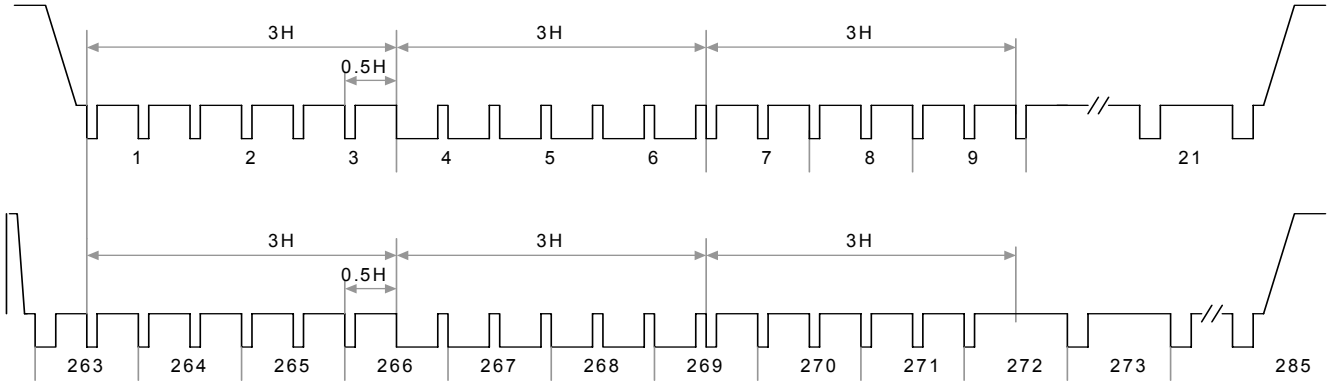


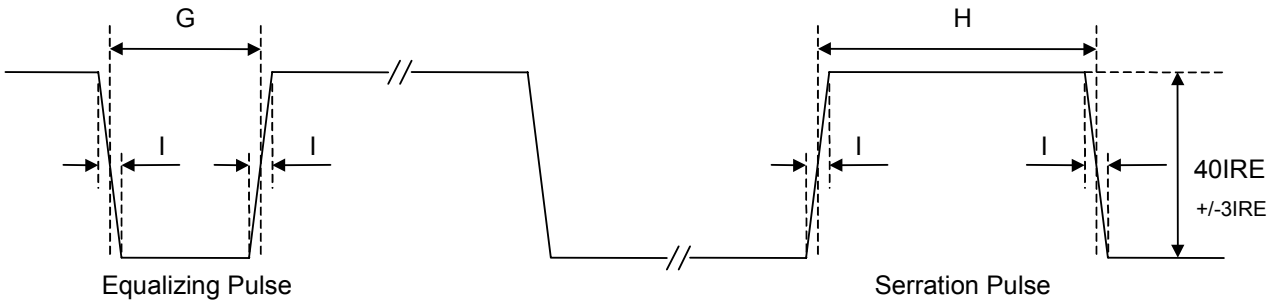


Equalizing Pulse and Serration Pulse

| Symbol | | Measurement point | Value | Recommended tolerance | units |
|---|---|---|---|---|---|
| G | Pre-equalizing pulse width | 50% | 2.3 | +/- 0.1 | usec |
| H | Vertical serration pulse width | 50% | 4.7 | +/- 0.2 | usec |
| G | Post-equalizing pulse width | 50% | 2.3 | +/- 0.1 | usec |
| I | Sync rise time | | 140 | Max 250 | nsec |

* there is a case where tolerance of Sync rise time is added to Pulse width tolerance.


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( 2-1-3 ) PAL-B, D, G, H, I
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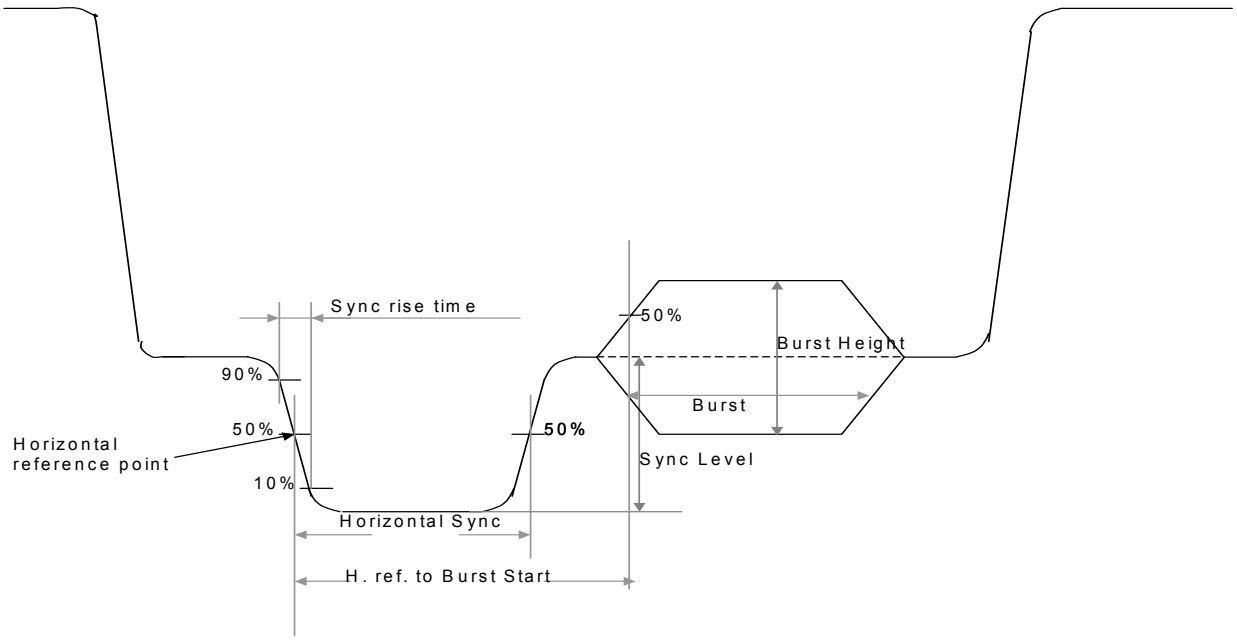


| | measurement point | value | Consumer Quality tolerance | units |
|---|---|---|---|---|
| Total line period(derived) | | 64.0 | | usec |
| Sync Level | | 300 | +/- 20 | mV |
| Sync rise time | 10% - 90% | 0.2 | Max 0.3 | usec |
| Horizontal Sync width | 50% | 4.7 | +/- 0.2 | usec |
| Horizontal reference point to burst start | 50% | 5.6 | +/- 0.1 | usec |
| Burst * | 50% | 10 | +/- 1 | cycles |
| Burst Height ** | | 300 | +/- 30 | mV |

* there is case where tolerance of Sync rise time is added to Sync width tolerance.


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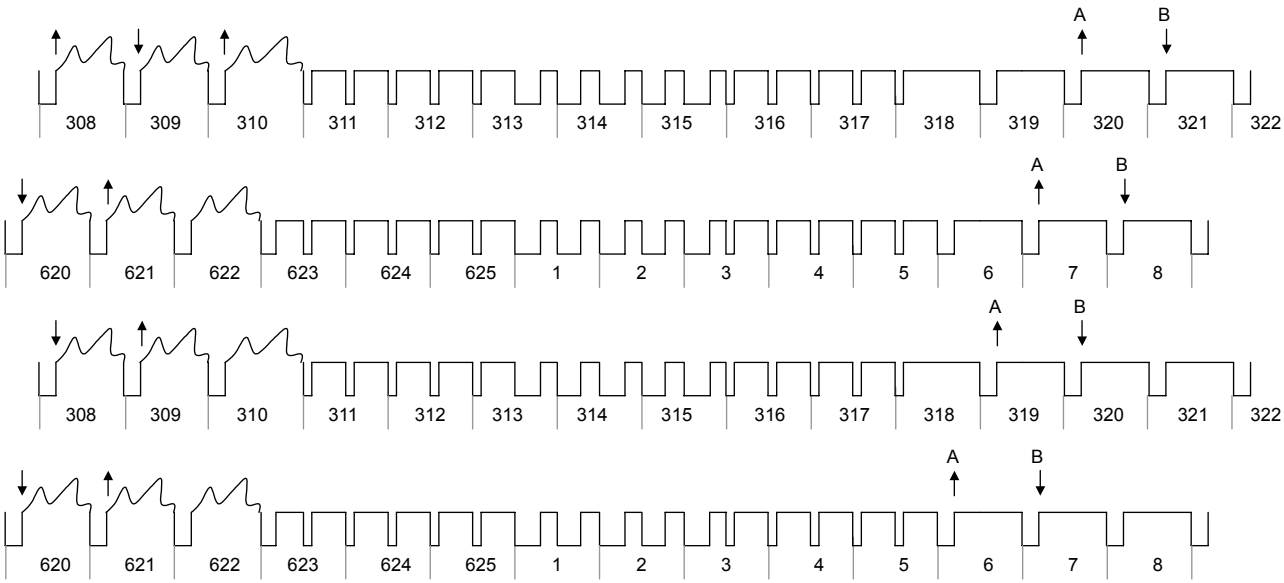
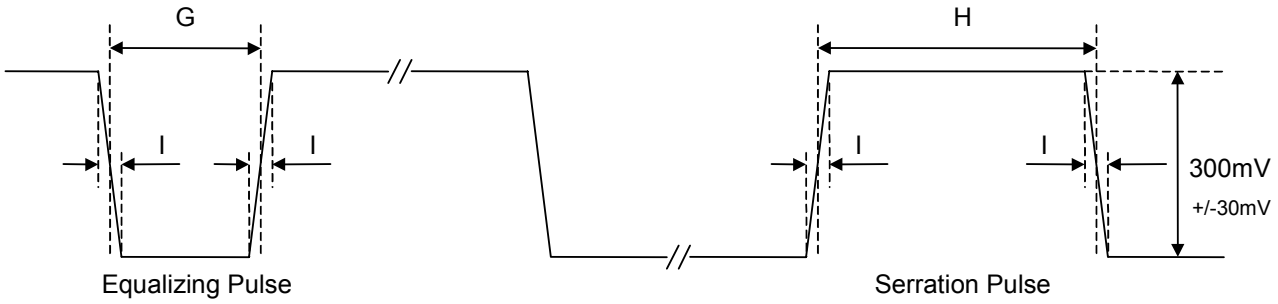
( 2-1-4 ) Vertical Sync Signal timing and Burst Phase PAL-B, D, G, H, I

PAL-B,D,G,H,I




A : Phase of Burst : nominal Value + 135°
B : Phase of Burst : nominal Value - 135°

Since Burst frequency and Line frequency are not practically in integer-multiple relation, specified phase value is not exactly 135 degrees.
Diagram below shows phase direction.




Equalizing Pulse and Serration Pulse

| Symbol | | Measurement point | Value | Recommended tolerance | units |
|---|---|---|---|---|---|
| G | Pre-equalizing pulse width | 50% | 2.35 | +/- 0.1 | usec |
| H | Vertical serration pulse width | 50% | 4.7 | +/- 0.2 | usec |
| G | Post-equalizing pulse width | 50% | 2.35 | +/- 0.1 | usec |
| I | Sync rise time | | 200 | Max 300 | nsec |

* there is a case where tolerance of Sync rise time is added to Pulse width tolerance.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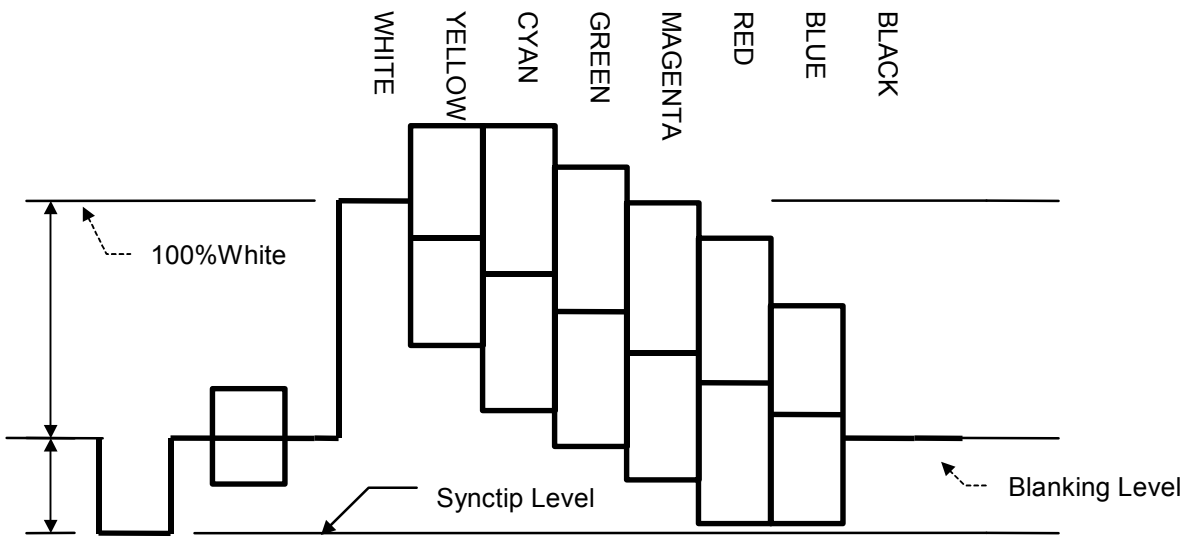
( 12 ) On-chip Color Bar
The AK8815/16 can output Color Bar signal.
Color Bar signal to be generated has 100 % amplitude and 100 % Saturation levels.
Color Bar signal is output by setting register.
When to output Color Bar signal, there are 2 modes of operation – one is external Sync timing mode for normal operation, and the other is internal self-operation mode.

In internal self-operating mode, required timing is internally generated automatically. Namely, it is no need to input synchronization timing from outside of the chip.
Operation mode setting is done by Mode Register.
When BBG-bit is set, BBG-bit is prioritized ( Black Burst is output ).




The following values are code for ITU-R. BT601

| | WHITE | YELLOW | CYAN | GREEN | MAGENTA | RED | BLUE | BLACK |
|---|---|---|---|---|---|---|---|---|
| Cb | 128 | 15/16 | 15/166 | 54 | 202 | 90 | 240 | 128 |
| Y | 235 | 210 | 170 | 145 | 106 | 81 | 41 | 15/16 |
| Cr | 128 | 146 | 15/16 | 34 | 222 | 240 | 110 | 128 |

( 13 ) Black Burst Signal generation function
The AK8815/16 can output Black Burst signal ( Black level output ).
When to output Black Burst signal, there are 2 modes of operation – one is external Sync timing mode for normal operation , and the other is internal self-operation mode.

In internal self-operation mode, required timing is internally generated automatically. Namely, it is no need to input synchronization timing from outside of the chip.
When BBG-bit of [ Mode Register ] is set to “1”, same operation is processed as in the case where fixed-15/16 Y signal and fixed-128 Pb / Pr signal outputs are input.
Operation mode setting is done by Mode Register setting.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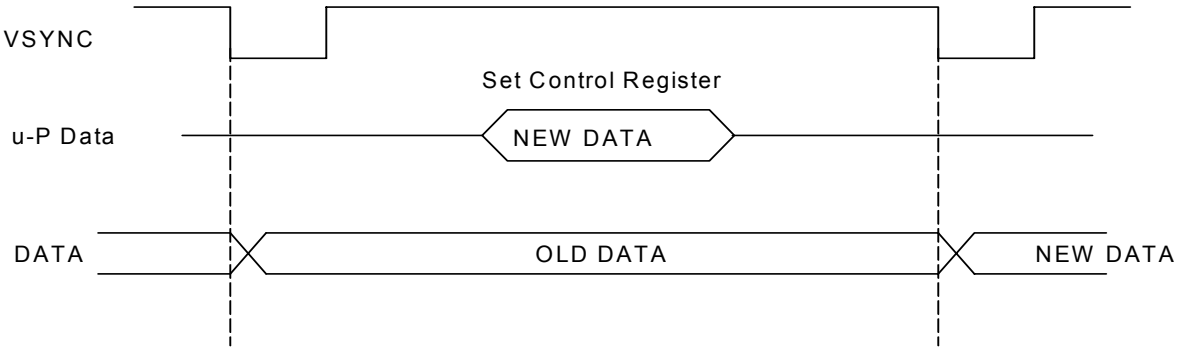
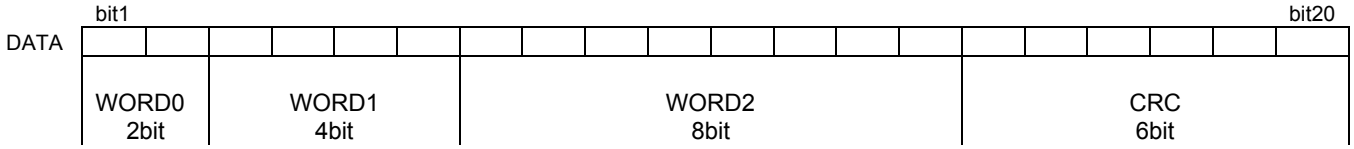
(14) Video ID

The AK8815/16 supports to encode the Video ID ( EIAJ CPR-1204 ) which distinguishes the aspect ratio etc..
This is also used as CGMS ( Copy Generation Management System ).
Turning “ON/OFF” of this function is made by setting both VMOD-bit = 0 and VBID-bit = 1 of { Mode Register (0x00) }. And data to be set is written into { VBID / WSS Data1 & 2 Registers ( 0x01,0x02 )}.
Video ID information is the highest order of priority information among VBI information ( when simultaneous outputs occur with Macrovision signaling, only the VBI information is super-imposed on this line ).

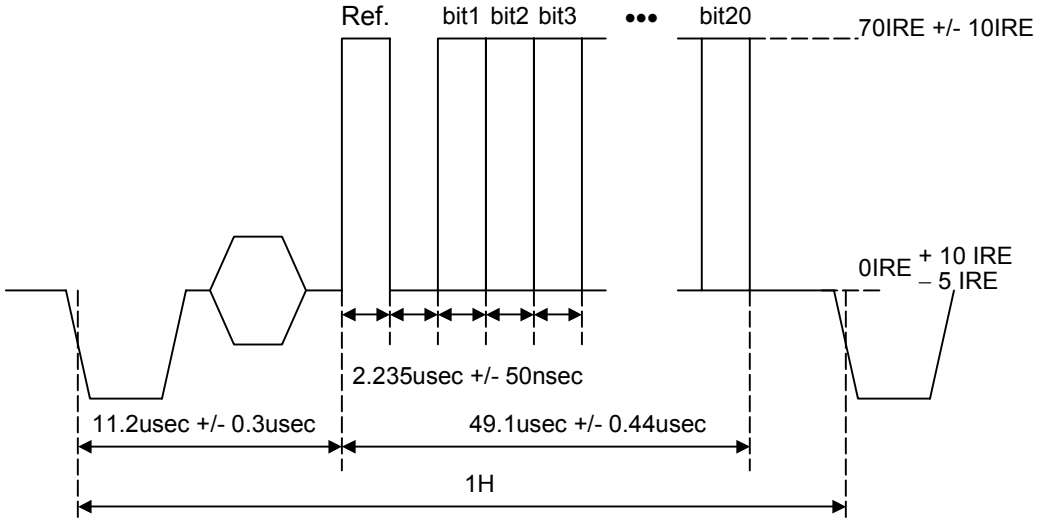
VBID Data Update timing .




VBID Code assignment
20 bit data is configured with WORD0 = 2 bit, WORD1 = 4 bit, WORD2 = 8 bit and CRC = 6 bit.
CRC is automatically calculated and added by the AK8815/16.
Default values of CRC polynomial expression X6 + X + 1 are all ones.
-data configuration




VBID Waveform




| | 525/60 System |
|---|---|
| Amplitude | 70IRE |
| Encode Line | 20/283 |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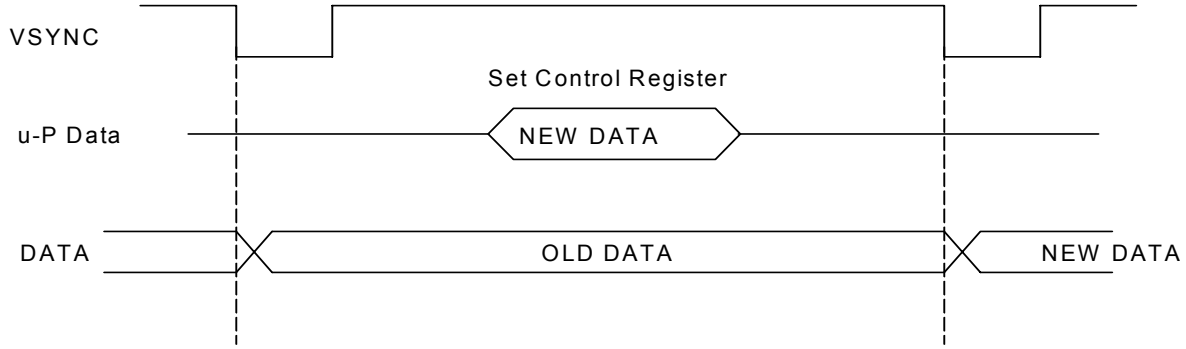
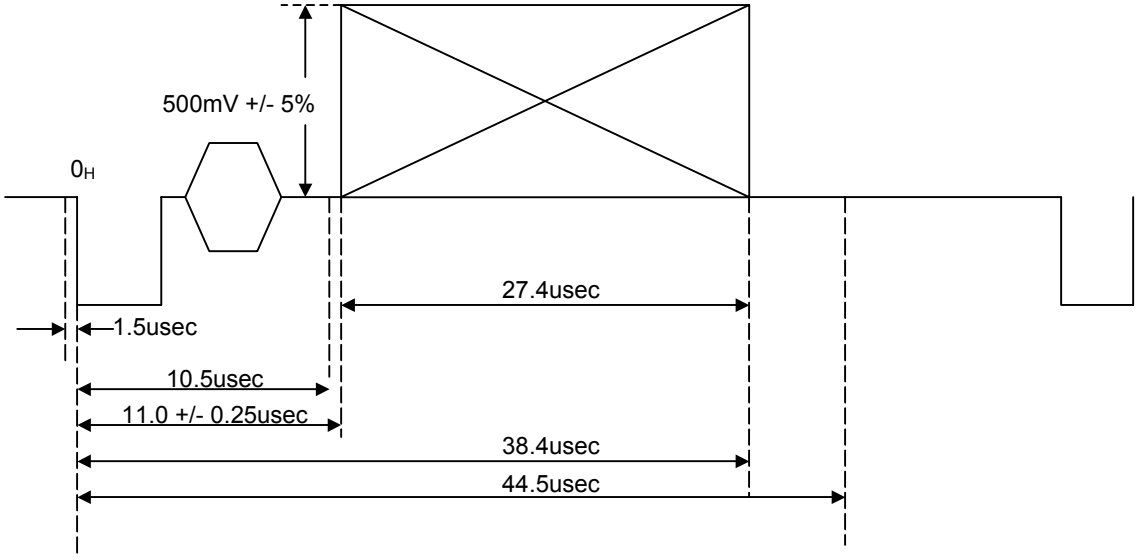
( 15 ) WSS function

The AK8815/16 supports to encode the WSS ( ITU-R. BT.1119 ) which distinguishes the aspect ratio and sets CGMS-A etc..
Turning “ON/OFF“ of this function is made by setting both VMOD-bit = 1 and WSS-bit = 1 of { Mode Register ( 0x00 ) }. And data to be set is written into { VBID / WSS Data1 & 2 Registers ( 0x01, 0x02 )}.

WSS Data Update timing




WSS Waveform




Encode line : former half of Line 23 ( Blank output during latter half )
Coding : Bi-phase modulation coding
Clock : 5 MHz ( Ts = 200 nS )
Encoding details as follows

| Run-in | Start code | Group 1<br>Aspect ratio | Group 2<br>Enhanced Services | Group 3<br>Subtitles | Group4 Reserved |
|---|---|---|---|---|---|
| 29 elements | 24 elements | 24 elements | 24 elements | 18 elements | 18 elements |
| | | Bit numbering<br>0 1 2 3<br>LSB MSB<br>0 : 000111<br>1 : 111000 | Bit numbering<br>4 5 6 7<br>LSB MSB<br>0 : 000111<br>1 : 111000 | Bit numbering<br>8 9 10<br>LSB MSB<br>0 : 000111<br>1 : 111000 | Bit numbering<br>11 12 13<br>LSB MSB<br>0 : 000111<br>1 : 111000 |
| 0x1F1C71C7 | 0x1E3C1F | | | | |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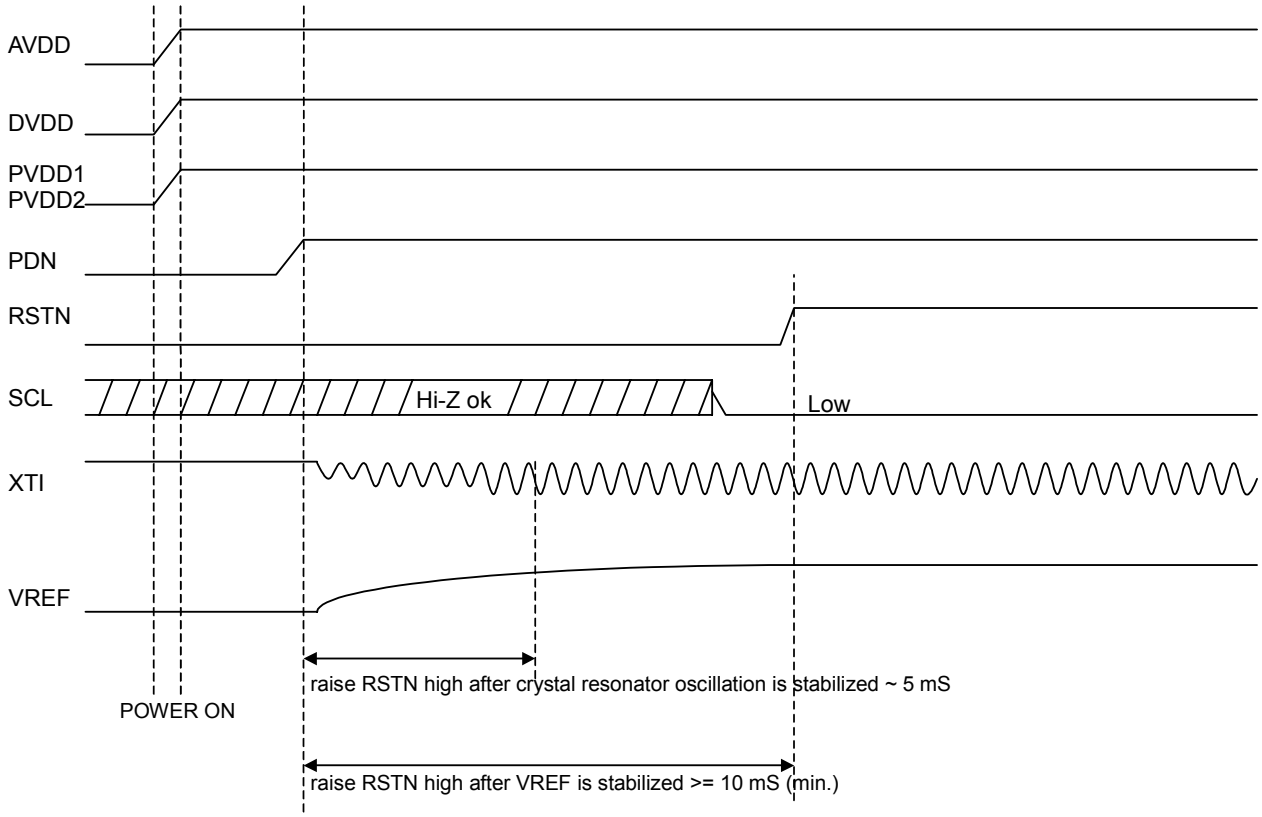
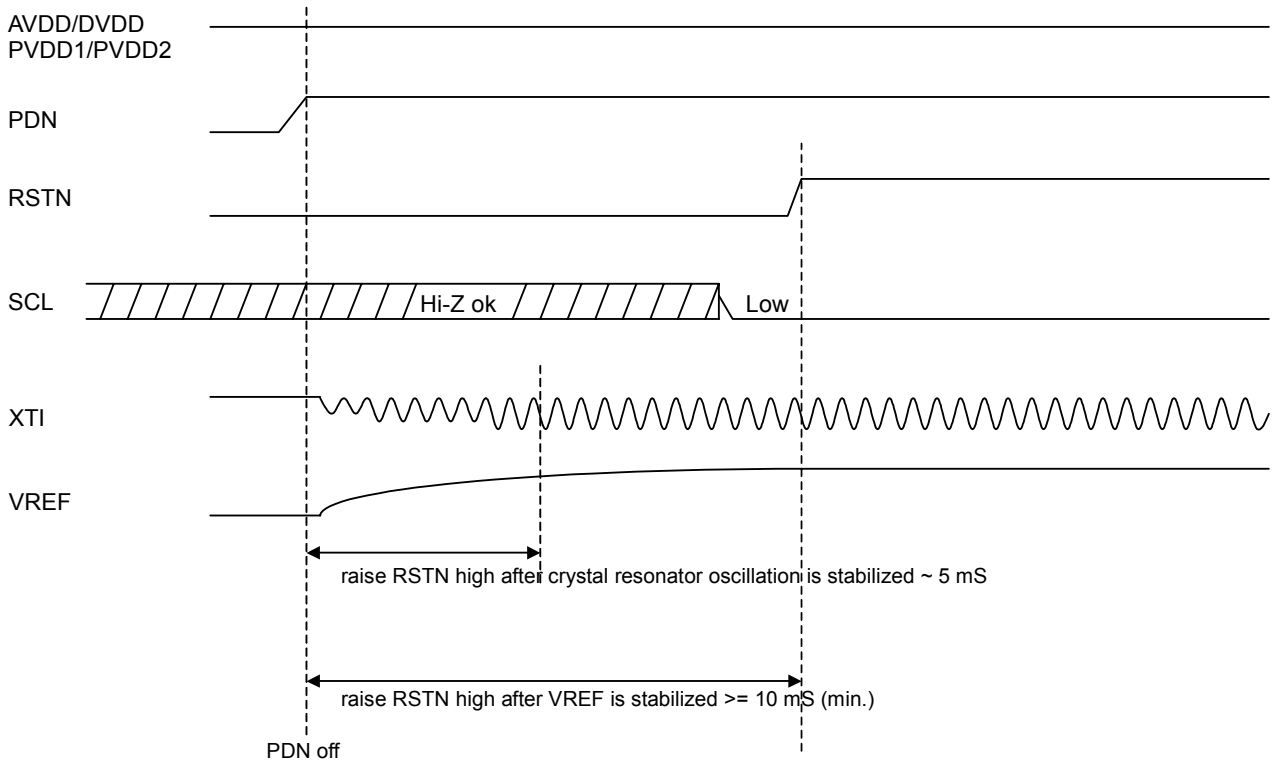
# POWER UP SEQUENCE

Power-Up Sequence ( power supply turn-on sequence )




Power-Down Release sequence





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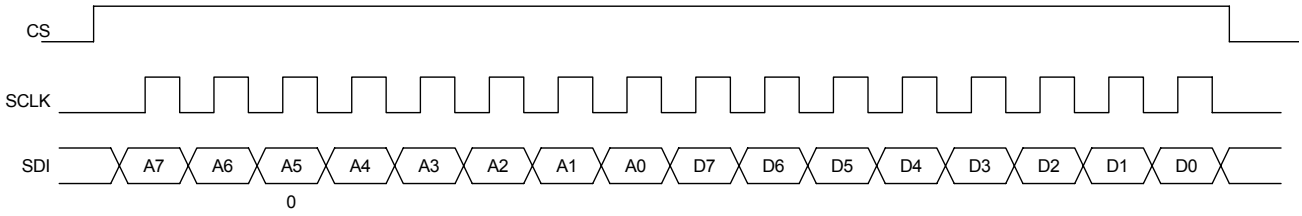
# DEVICE CONTROL SEQUENCE

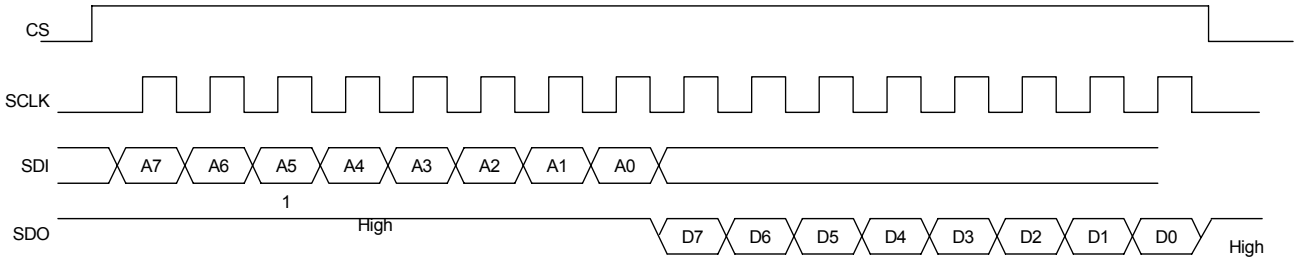
Device Control Interface

following modes of operations are controlled via 4-wire serial interface.
Hi-Z inputs to CS, SCLK, and SDI pins are inhibited, except at power-down ( PDN pin = low ).

Write Sequence: A5=0




Read Sequence: A5=1




A5 bit becomes an identification tab A5 1 : Read
A5 0 : Write
CS must be set to low at every address change.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# REGISTER MAP

| Address | Register | Default | R/W | Function |
|---|---|---|---|---|
| 0x00 | Mode Register | 0x00 | R/W | Mode set Register |
| 0x01 | VBID/WSS Data 1 Register | 0x00 | R/W | VBID data is set, WSS data is set |
| 0x02 | VBID/WSS Data 2 Register | 0x00 | R/W | VBID data is set, WSS data is set |
| 0x03 | Device ID and Revision ID Register | 0x06 | R | Register for Device ID and Revision ID |
| 0x04 | Reserved | 0x00 | R/W | |
| 0x05 | Input Control Register | 0x00 | R/W | input control register for out-of-standard quality input signal |
| 0x06 | Reserved | 0x0f | R/W | |
| 0x07 | Reserved | 0xfc | R/W | |
| 0x08 | Reserved | 0x20 | R/W | |
| 0x09 | Reserved | 0xd0 | R/W | |
| 0x0A | Reserved | 0x6f | R/W | |
| 0x0B | Reserved | 0x0f | R/W | |
| 0x0C | Reserved | 0x00 | R/W | |
| 0x0D | Reserved | 0x00 | R/W | |
| 0x0E | Reserved | 0x0c | R/W | |
| | | | | |
| 0x10 | Reserved | 0xe3 | R/W | |
| 0x11 | Reserved | 0xf3 | R/W | |
| 0x12 | Reserved | 0x09 | R/W | |
| 0x13 | Reserved | 0xbd | R/W | |
| 0x14 | Reserved | 0x66 | R/W | |
| 0x15 | Reserved | 0xb5 | R/W | |
| 0x15/16 | Reserved | 0x90 | R/W | |
| 0x17 | Reserved | 0xb2 | R/W | |
| 0x18 | Reserved | 0x7d | R/W | |
| | | | | |


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## Mode Register (R/W) [Address 0x00]

**Sub Address 0x00** **Default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| DAC | BBG | CBG | MAS | WSS | VBID | SCR | VMOD |
| Default Value | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SYS1_REG Definition

| BIT | Register Name | | R/W | Definition |
|---|---|---|---|---|
| bit 0 | VMOD | Video Mode bit | R/W | 0: NTSC<br>1: PAL |
| bit 1 | SCR | Sub-Carrier Reset bit | R/W | 0: Sub-Carrier Reset off<br>1: Sub-Carrier Reset |
| bit 2 | VBID | VBID Set Register | R/W | 0: VBID OFF<br>1: VBID ON |
| bit 3 | WSS | WSS Set Register | R/W | 0: WSS OFF<br>1: WSS ON |
| bit 4 | MASMD | Master Mode bit | R/W | Master Mode bit to set Sync mode when Color Bar signal and Black Burst signal are generated<br>0 : operation by an external Sync timing<br>1 : operation by an internal self-operating mode ( master mode ) |
| bit 5 | CBG | Color Bar Generator bit | R/W | 0: OFF<br>1: ON<br>when BBG is set, BBG is prioritized. |
| bit 6 | BBG | Black Burst Generator bit | R/W | 0: OFF<br>1: ON |
| bit 7 | DAC | DAC Set bit | R/W | 0: DAC OFF<br>1: DAC ON |


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**VBID/WSS 1 Register (R/W) [Address 0x01]**
**VBID/WSS 2 Register (R/W) [Address 0x02]**

Video ID and WSS data setting are made. A common data register is used for both video ID and WSS data. When VBID bit of mode register is set in NTSC mode, data is for VBID data ,and when WSS bit of mode register is set in PAL mode, data is for WSS data.

When VBID-bit is “1” and VMOD-bit is “0” in mode register, the following bits are assigned.

**Sub Address 0x01** **default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| VBID7 | VBID8 | VBID9 | VBID10 | VBID11 | VBID12 | VBID13 | VBID14 |
| Default Value | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Sub Address 0x02** **default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | VBID1 | VBID2 | VBID3 | VBID4 | VBID5 | VBID6 |
| Default Value | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note ) “0” should be written into reserved bits.
VBID1 ---- VBID14 above correspond to the bit 1 ---- bit 14 which are described at { VBID Data Code Assignment } in { ( 14 ) Video ID } section.
A 6-bit CRC code from bit 15 ~ bit 20 is automatically added by the AK8815/16.
Data is retained till data is updated to a new one.

Following bits are assigned when WSS-bit is “1” and VMOD-bit is “1” in mode register.

**Sub Address 0x01** **default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| G2-7 | G2-6 | G2-5 | G2-4 | G1-3 | G1-2 | G1-1 | G1-0 |
| Default Value | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Sub Address 0x02** **default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | G4-13 | G412 | G4-11 | G3-10 | G3-9 | G3-8 |
| Default Value | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note ) WSS data is written with 0x01 first, then 0x02 in this order.
When the 2nd byte ( 0x02 ) of WSS data is written, the AK8815/16 interprets that data is updated to a new one and then encodes it to the next video line ( Line 23 ).
Data is retained till data is updated to a new one.


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## Device ID and Revision ID Register (R) [Address 0x03]

**Sub Address 0x03** **default Value 0x06**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| REV3 | REV2 | REV1 | REV0 | DEV3 | DEV2 | DEV1 | DEV0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Device ID and Revision ID Register Definition

| BIT | Register Name | | R/W | Definition |
|---|---|---|---|---|
| bit 0 ~ bit 3 | DEV0 ~ DEV2 | Device ID bit | R | Device ID bit to indicate Device ID. |
| bit 4 ~ bit 7 | REV0 ~ REV3 | Revision ID bit | R | Revision ID bit to indicate Revision ID. Revision ID is updated When a possible software modification is made. It is 0x00. |

## Reserved Register (R) [Address 0x04]

**Sub Address 0x03** **default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Device ID and Revision ID Register Definition

| BIT | Register Name | | R/W | Definition |
|---|---|---|---|---|
| bit 0 ~ bit 7 | Reserved | Reserved bit | R/W | Reserved |

## Input Control Register (R/W) [Address 0x05]

This is an out-of-standard quality input signal control register.

**Sub Address 0x05** **default Value 0x00**

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| FLT | CBCR | VD2 | VD1 | VD0 | HD2 | HD1 | HD0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Adjustment of Sync input timing is made

| BIT | Register Name | | R/W | Definition |
|---|---|---|---|---|
| bit 0 ~ bit 2 | HD0 ~ HD2 | HSYNC Input Delay | R/W | HSYNC signal input is delayed by the set value. HD [ 2:0 ] system clock count delay ( + 0 ~ + 7 CLK delay ) |
| bit 3 ~ bit 5 | VD0 ~ VD2 | VSYNC Input Delay | R/W | VD0 ~ VD2 VSYNC Input Delay VSYNC signal input is delayed by the set value. VD [ 2:0 ] system clock count delay ( + 0 ~ + 7 CLK delay ) |
| bit 6 | CBCR | Exchange CbCr | R/W | Cb, Cr timing data are interchanged at CBCR = 1. |
| bit 7 | FLT | Y Flat Data | R/W | Y input data is linear- interpolated ( averaging most adjacent data ). |


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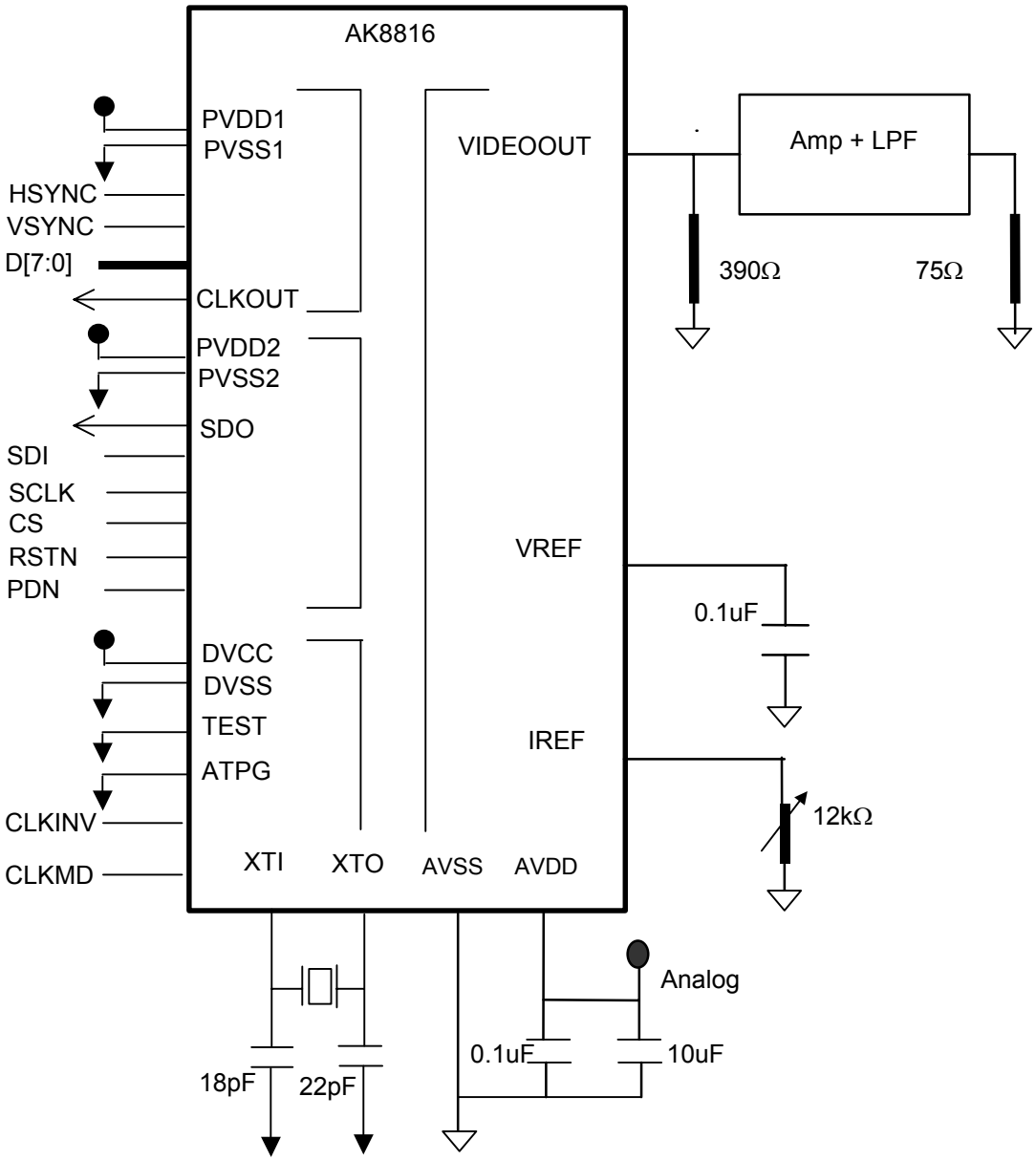
## SYSTEM CONNECTION EXAMPLE





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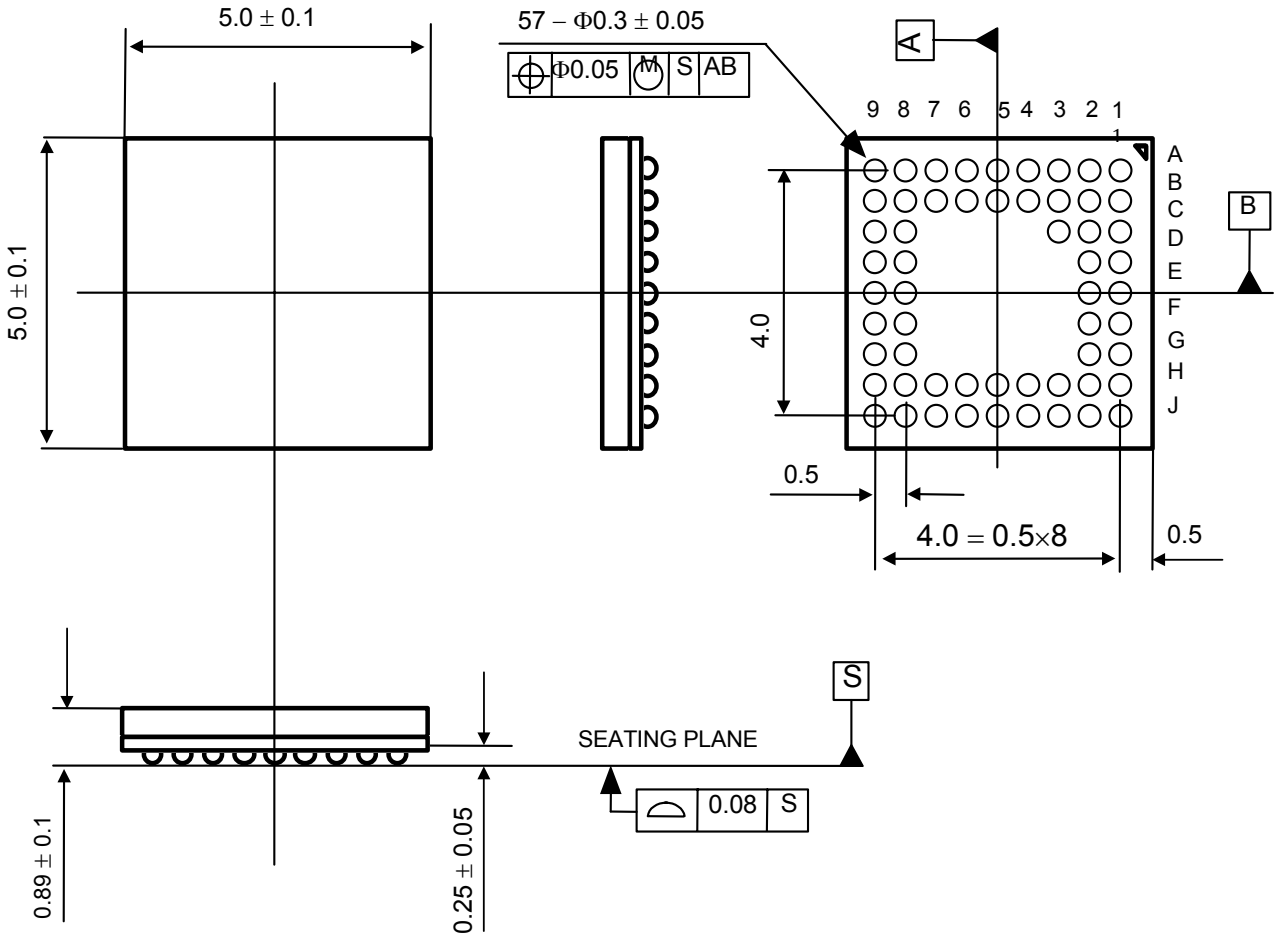
# PACKAGE

Package Outline dimension
57 pin FBGA
-package drawing




Package & Lead frame material

Package molding compound: Epoxy

Interposer material: BT resin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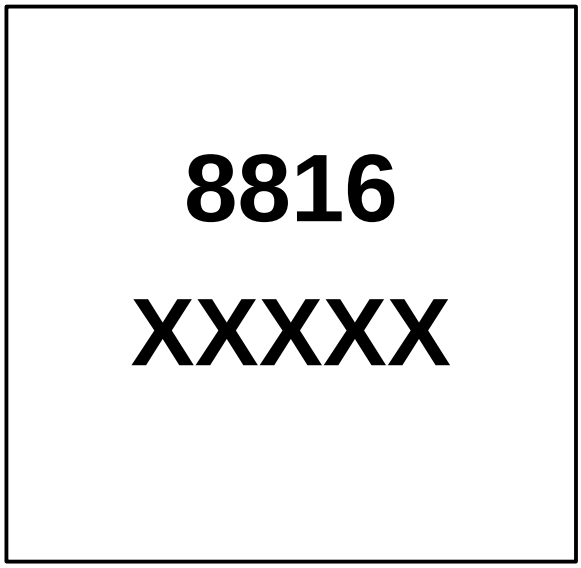
## MARKING




a. Package type : BGA
b. Pin count : 57 pins ( 1 pin for index )
c. Product number : 8815
d. Factory control code : xxxxx ( 5 digits )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