Winbond

W86C450/P

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

GENERAL DESCRIPTION

The W86C450/P is an improved specification version of the W86C250A Universal Asynchronous Receiver/Transmitter (UART). The improved specifications ensure compatibility with the state-of-the-art CPUs. Functionally, the W86C450/P is equivalent to the INS8250A of the National Semiconductor. The W86C450/P is fabricated using WINBOND's CMOS process.

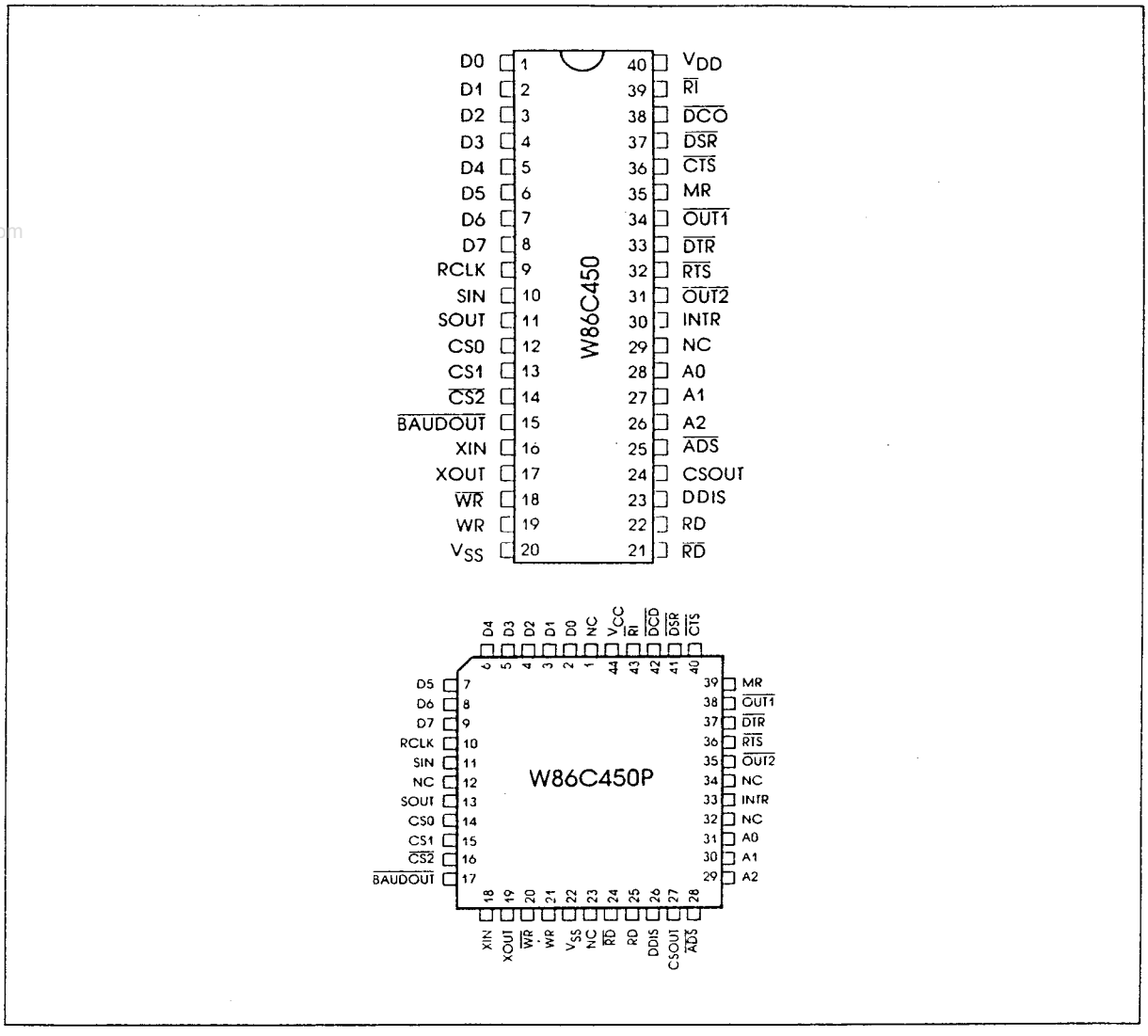
The W86C450/P performs serial-to-parallel conversion an data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the W86C450/P at any time during the functional operation. Status information reported includes the type and condition operation. Status information reported includes the type and condition of the transfer operations being performed by the W86C450/P, as well as any error conditions (parity, overrun, framing, or break interrupt).

The W86C450/P includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producing 16×clock for driving the internal transmitter logic. Provisions are also included to use this 16×clock to capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

FEATURES

- Easily interfaces to most popular microprocessors.
- Adds or deletes standard asynchronous communication bit (start, stop, and parity) to or from serial data stream.
- Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allow division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16×clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
  - -5, 6, 7, or 8-bit characters
  - -Even, odd, or no-parity bit generation and detection
  - -1, 1.5 or 2-stop bit generation.
  - -Baud generation (DC to 56K baud).
- False start bit detection.
- Complete status reporting capabilities.
- TRI-STATE TTL drive capabilities for bidirectional data bus and control bus.
- Line break generation and detection.
- Internal diagnostic capabilities:
  - -Loopback controls for communications link fault isolation.
  - -Break, parity, overrun, framing error simulation.
- Fully prioritized interrupt system controls.

PIN CONFIGURATION



PIN DESCRIPTIONS

The following describes the function of all the W86C450/P (UART) pins. Some of these descriptions reference internal circuits. In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents logic 1 (+2.4V nominal).

A. INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12 ~ 14 (P14 ~ 16)*: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables

*Pn means the nth pin of W86C450P, n = 1 ~ 44.

communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the T_{CSW} parameter.

Read (RD, $\overline{RD}$), Pins22 and 21 (P25,24)*: When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected UART register.

Write (WR, $\overline{WR}$), Pins 19 and 18 (P21,20)*: When WR is high or $\overline{WR}$ is low while the chip is selected. the CPU can write control words or data into the selected UART register.

Address Strobe ($\overline{ADS}$), Pin 25 (P28)*: The positive edge of an active Address Strobe ($\overline{ADS}$), signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

Notes:

1. Only an active RD or $\overline{RD}$ input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low or the $\overline{RD}$ input permanently high, when it is not used.
2. Only an active WR or $\overline{WR}$ input is required to transfer data to the UART duning a write operation. Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.
3. An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or wite operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 ~ 28 (P31 ~ 29)*: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Receiver Clock (RCLK), Pin 9 (P10)*: This inputs is the 16×baudrate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10 (P11)*: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear Send ($\overline{CTS}$), Pin 36 (P40)*: When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 ($\overline{CTS}$) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter.

*Pn means the nth pin of W86C450P, n = 1 ~ 44.

Register Addresses

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read). Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Note:

Whenever the $\overline{CTS}$ bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM MODEM Status Interrupt is enabled.

Master Reset (MR), Pin 35 (P39)*: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals ($\overline{SOUT}$, $\overline{INTR}$, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 1.) This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

Table 1. **UART Reset Functions**

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	OOOO0000 (Note 1)
Interrupt Identification Register	Master Reset	OOOOO001
Line Control Register	Master Reset	00000000
MODEM Control Register	Master Reset	OOO00000
Line Status Register	Master Reset	O1100000
MODEM Status Register	Master Reset	XXXX0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High

*Pn means the nth pin of W86C450P, n=1~44.

Notes:
1. O bits are permanently low.
2. Bits 7-4 are driven by the input signals.

Data Set Ready ($\overline{DSR}$), Pin 37 (P41)*: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 ($\overline{DSR}$) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM States Register.

Data Carrier Detect ($\overline{DCD}$) Pin 38 (P42)*: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 ($\overline{DCD}$) of the MODEM Status Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver.

Ring Indicator ($\overline{RI}$), Pin 39 (P43)*: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6(RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.

Notes:
1. Whenever The $\overline{DSR}$ bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
2. Whenever the $\overline{DCD}$ bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
3. Whenever the $\overline{RI}$ bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status interrupt is enabled.

V_{DD}, Pin 40 (P44): +5V supply.

V_{SS}, Pin 20 (P22): Ground (0V) reference.

B. OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33 (P37)*: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Request to Send ($\overline{RTS}$), Pin 32 (P36)*: When low, this informs the MODEM or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 ($\overline{RTS}$) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

*Pn means the nth pin of W86C450P, n=1~44.

Output 1 ($\overline{OUT1}$), Pin 34 (P38)*: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Output 2 ($\overline{OUT\ 2}$), Pin 31 (P35)*: This user-designated output can be set to an active low, by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Chip Select Out (CSOUT), Pin 24 (P27)*: When high, it indicates that the chip has been selected by active, CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deslected.

Driver Disable (DDIS), Pin 23 (P26)*: This goes low whenever the CPU is reading data from the UART. It can disable or control the direction at a data bus transceiver between the CPU and the UART (see Typical interface for a high Capacity Data Bus).

Baud Out ($\overline{BAUDOUT}$), Pin 15 (P17)*: This is the 16 x clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTR), Pin 30 (P33)*: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Line Status; Received Data Available; Trans-mitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11 (P13)*: This is the composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation or when the transmitter is idle.

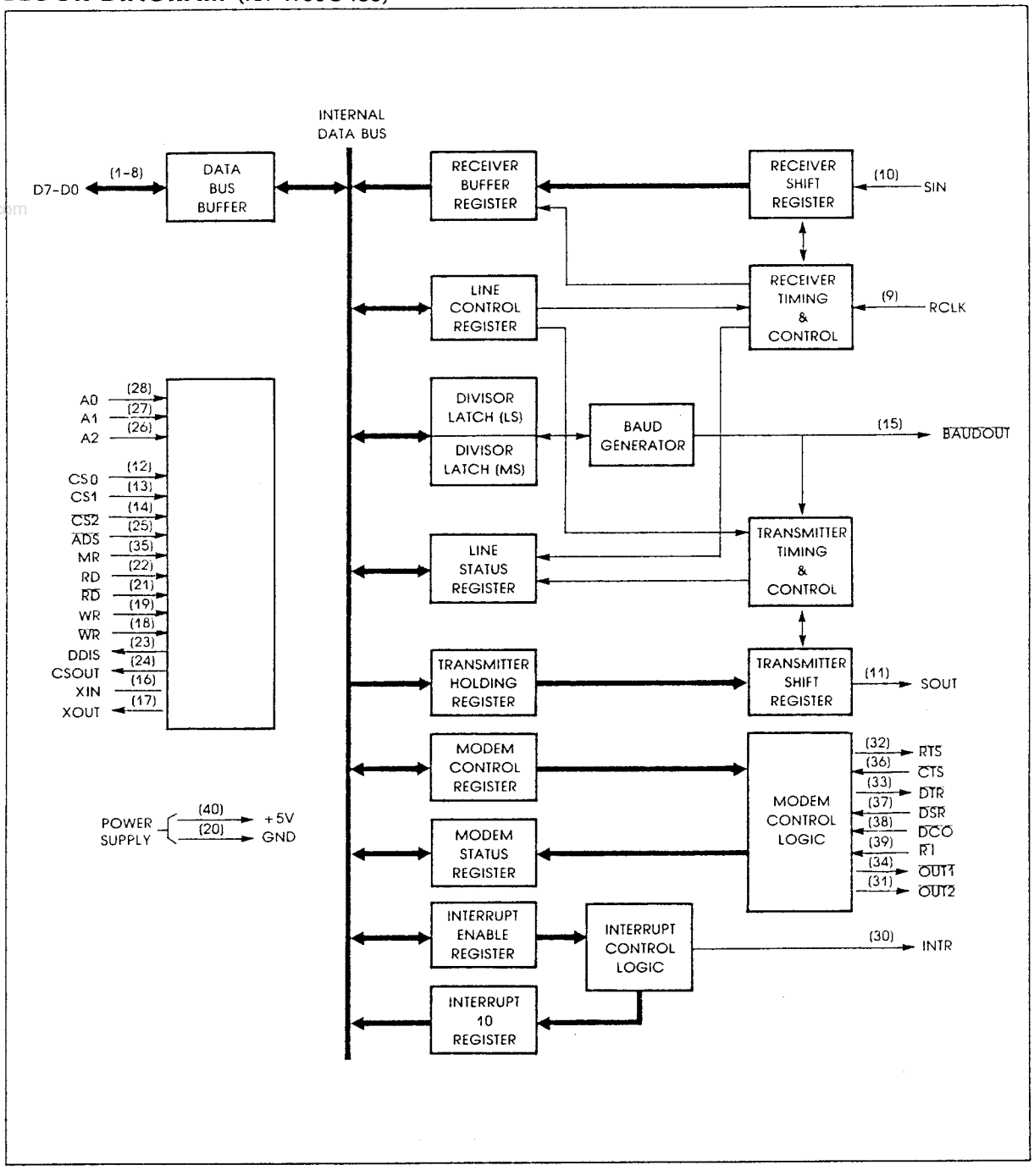
C. INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus, Pins 1 ~ 8 (P2 ~ 9)*: This bus is comprised of eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D7-D0 Data Bus.

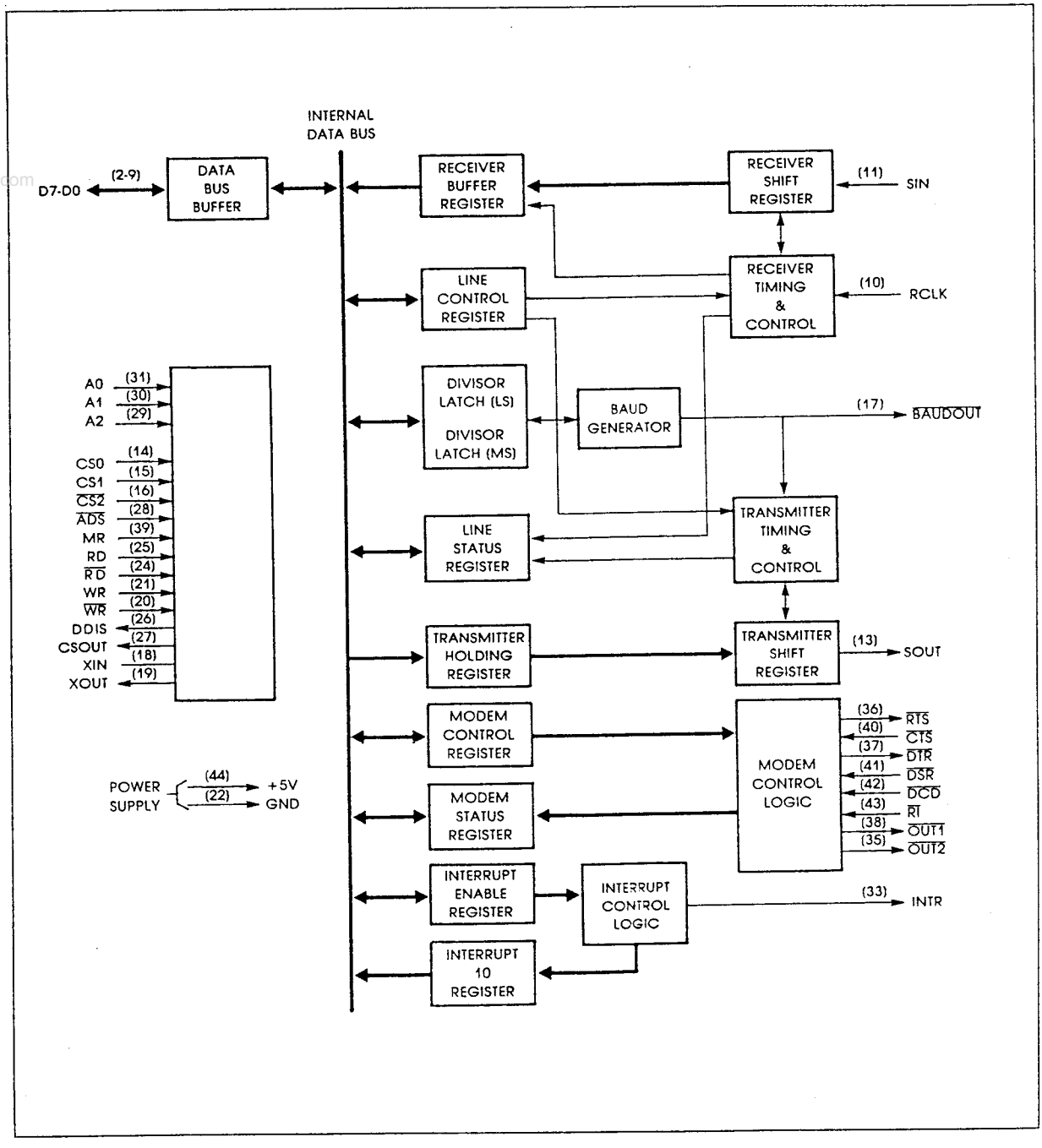
External Clock Input/Output (XIN, XOUT) Pins 16 and 17 (P18, 19)*: These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the UART via XIN (see typical oscillator network illustration).

*Pn means the nth pin of W86C450P, n = 1 ~ 44.

BLOCK DIAGRAM (for W86C450)



(for W86C450P)



REGISTERS

The system programmer may access any of the UART registers summarized in Table 2 via the CPU. These registers control UART operations including transmissions and reception of data. Each register bit in Table 2 has its name and reset state shown.

Table 2. **Summary of Registers**

	REGISTER ADDRESS										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
BIT NO.	RECEIVER BUFFER REGISTER (READ ONLY)	TRANSMITTER HOLDING REGISTER (WRITE ONLY)	INTERRUPT ENABLE REGISTER	INTERRUPT IDENT. REGISTER (READ ONLY)	LINE CONTROL REGISTER	MODEM CONTROL REGISTER	LINE STATUS REGISTER	MODEM STATUS REGISTER	SCRATCH REG-ISTER	DIVISOR LATCH (LS)	DIVISON LATCH (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Received Data Available	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	BIT 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Daba Bit 2	Data Bit 2	Receiver Line Status	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator	Bit 2	Bit 2	Bit 10
3	Data Bot 3	Data Bit 3	MODEM Status	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

A. LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

Table 2 shows the contents of the LCR. Details on each bit are as follows:

BIT 1	BIT 0	CHARACTER LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7- or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Selected bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3,4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0, Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

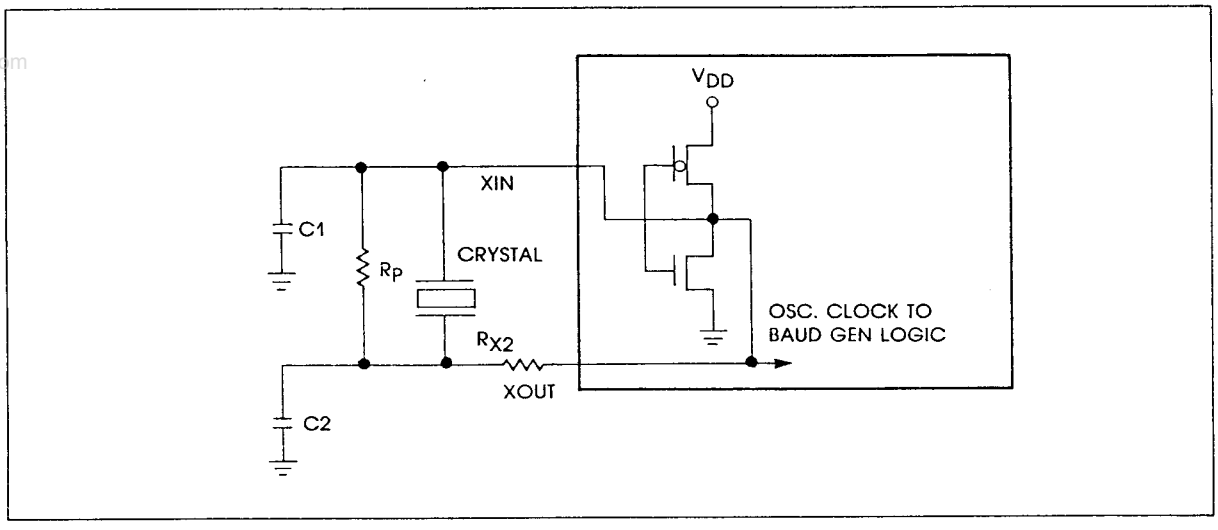
Note:
This feature enables the CPU to alert a terminal in a computer communications system. If the following squence is used, no erroneous or extraneous characters will be transmitted because of the break.

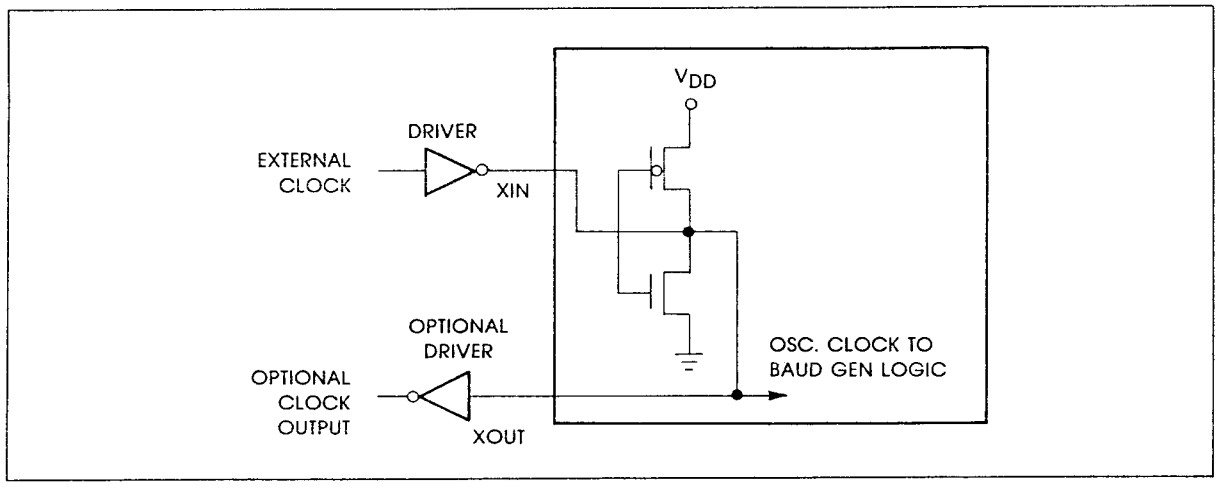
1. Load an all 0s, pad character, in response the THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

Duning the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

B. TYPICAL CLOCK CIRCUITS





Typical Oscillator Networks

CRYSTAL	Rp	Rx2	C1	C2
1.8 - 3.1 MHz	1M	1.5k	10 - 30 pF	40 - 60 pF

C. PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 3.1 MHz and dividing it by any divisor from 1 to $2^{16} - 1$. The output frequency of the Baud Generator is 16 × th Baud [divisor# = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table 3 provide decimal divisors to use with crystal frequencies of 1.8432 MHz and 3.072MHz respectively for common baud rates. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a division of 0 is not recommended.

Note:

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

Table 3. **Baud Rates Using 1.8432 MHz Crystal and 3.072 MHz Crystal**

DESIRED BAUD RATE	DECIMAL DIVISOR USED TO GENERATE 16 × CLOCK		PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL	
	1.8432M	3.072M	1.8432M	3.72M
50	2304	3840	—	—
75	1536	2560	—	—
110	1047	1745	0.026	0.026
134.5	857	1428	0.058	0.034
150	768	1280	—	—
300	384	640	—	—
600	192	320	—	—
1200	96	160	—	—
1800	64	107	—	0.312
2000	58	96	0.69	—
2400	48	80	—	—
3600	32	53	—	0.628
4800	24	40	—	—
7200	16	27	—	1.23
9600	12	20	—	—
19200	6	20	—	—
38400	3	5	—	—
56000	2	—	2.86	—

D. LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. Table 2 shows the contents of the Line Status Register. Details on each bit are as follows:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is a logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contens of the Line Status Register. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whwnever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the SIN pin to be logical 1 for at least 1/2 bit time.

Note:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 whenever the CPU loads the Transmitter Holding Register.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note:
The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

E. INTERRUPT IDENTIFICATION REGISTER (IIR)

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is completed. Table 2 shows the contents of the IIR. Details on each bit are as follows:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bit 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Talbe 4.

Bit 3 through 7: These five bits of the IIR are always logic 0.

Table 4. **Interrupt Control Functions**

IIR				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register

(Continued)

IIR				INTERRUPT SET AND FUNCTIONS		
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or auxiliary Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

F. INTERRUPT ENABLE REGISTER

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table 2 shows the contents of the IER. Details on each bit are as follows:

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

G. MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table 2 and are described below. Table 2 shows the contents of the MCR. Details on each bit are as follows:

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note:
The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary used-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur. The transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$ are internally connected to the four MODEM Control inputs. The MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

H. MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Table 2 shows the contents of the MSR. Details on each bit are as follows:

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the

RI input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is to a 1, this bit is equivalent to OUT 2 in the MCR.

I. SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYM.	RATING	UNIT
Supply Voltage	$V_{DD}-V_{SS}$	−0.3 ~ 7	V
Input Voltage	V_I	−0.3 ~ 7	V
Operating Temp.	T_{OPR}	0 ~ 70	°C
Storage Temp.	T_{TG}	−65 ~ 150	°C
Power Dissipation	P_D	400	mW

D.C. CHARACTERISTICS

(V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{ILX}	Clock input	−0.5	—	0.8	V
	V_{IHX}		2.0	—	V_{DD}	V
Input Voltage	V_{IL}	Other inputs	−0.5	—	0.8	V
	V_{IH}		2.0	—	V_{DD}	V
Output Voltage	V_{OL}	I_{OL} = 1.6mA on all output	—	—	0.4	V
	V_{OH}	I_{OH} = −1.0mA on all output	2.4	—	—	V

(Continued)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average Power Supply Current (V_{DD})	I_{CCA}	V_{DD}=5.25V, T_A=25°C No load on output SIN, DSR, DCD, CTS, RI=2.4V All other inputs = 0.4V Baud Rate Generator is 4 MHz Baud Rate is 50k	—	—	10	mA
Input Leakage	I_{IL}	V_{DD}=5.25V, V_{SS}=0V All other pins floating V_{IN}=0V, 5.25V	—	—	±10	μA
Clock Leakage	I_{CL}		—	—	±10	μA
Tri-state Leakage	I_{OZ}	V_{DD}=5.25V, V_{SS}=0V V_{OUT}=0V, 5.25V 1) Chip deselected 2) WRITE mode, chip selected	—	—	±20	μA
MR Schmitt Vil	M_{ILMR}		—	—	0.8	V
MR Schmitt Vih	V_{IHMR}		2.0	—	—	V

CAPACITANCE

(T_A=25°C, V_{DD}=V_{SS}=0V)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock Input Cap.	C_{XI}	fc = 1MHz Unmeasured pins returned to V_{SS}	—	15	20	pF
Clock Output Cap.	C_{XO}		—	20	30	pF
Input Capacitance	C_I		—	6	10	pF
Output Capacitance	C_O		—	10	20	pF

A.C. CHARACTERISTICS

(V_{DD}=5.0V ±5%, V_{SS}=0V, T_A=0°C TO 70°C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Address Strobe Width	T_{ADS}		60	—	nS
Address Hold Time	T_{AH}		0	—	nS
RD, $\overline{RD}$ Delay From Address	T_{AR}	(Note 1)	60	—	nS
Address Set Up Time	T_{AS}		60	—	nS
WR, $\overline{WR}$ Delay from Address	T_{AW}	(Note 1)	60	—	nS
Chip Select Hold Time	T_{CH}		0	—	nS
Chip Select Setup Time	T_{CS}		60	—	nS

(Continued)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Chip Select Output Delay from Select	T_{CSC}	@100pF loading (Note 1)	—	100	nS
RD, $\overline{RD}$ Delay from Chip Select	T_{CSR}	(Note 1)	50	—	nS
WR, $\overline{WR}$ Delay from Select	T_{CSW}	(Note 1)	50	—	nS
Data Hold Time	T_{DH}		40	—	nS
Data Setup Time	T_{DS}		40	—	nS
RD, $\overline{RD}$ to Floating Data Delay	T_{HZ}	@100pF loading (Note 2)	0	100	nS
Master Reset Pulse Width	T_{MR}		5	—	μS
Address Hold Time from RD, $\overline{RD}$	T_{RA}	(Note 1)	20	—	nS
Read Cycle Delay	T_{RC}		175	—	nS
Chip Select Hold Time from RD, $\overline{RD}$	T_{RCS}	(Note 1)	20	—	nS
RD, $\overline{RD}$ Strobe Width	T_{RD}		125	—	nS
RD, RD to Drive Disable Delay	T_{RDD}	@100pF loading (Note 2)	—	60	nS
Delay from RD, RD to Data	T_{RVD}	@100pF loading	—	125	nS
Address Hold Time from WR, $\overline{WR}$	T_{WA}	(Note 1)	20	—	nS
Write Cycle Delay	T_{WC}		200	—	nS
Chip Select Hold Time from, WR, $\overline{WR}$	T_{WCS}	(Note 1)	20	—	nS
WR, $\overline{WR}$ Strobe Width	T_{WR}		100	—	nS
Duration of Clock High Pulse	T_{XH}	External Clock	140	—	nS
Duration of Clock Low Pulse	T_{XL}	(3.1 MHz Max.)	140	—	nS
Read Cycle = $T_{AR}+T_{RD}+T_{RC}$	RC		360	—	nS
Write Cycle = $T_{AW}+T_{WR}+T_{WC}$	WC		360	—	nS
Baud Generator					
Baud Divisor	N		1	$2^{16}-1$	nS
Baud O/P Positive Edge Delay	T_{BHD}	100 pF Load	—	175	nS
Baud O/P Negative Edge Delay	T_{BLD}	100 pF Load	—	175	nS
Baud Output Upt Time	T_{HW}	fx = 3MHz, ÷3, 100pF Load	250	—	nS
Baud Output Down Time	T_{LW}	fx = 2MHz, ÷2, 100pF Load	425	—	nS
Receiver					
Delay from RD, $\overline{RD}$ (RD RBR or RD LSR) to Reset Interrupt	T_{RINT}	100 pF Load	—	1	μS
Delay from RCLK to Sample Time	T_{SCD}		—	2	μS

(Continued)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	T_{SINT}		—	1	RCLK Cycles (Note2)
Transmitter					
Delay from WR, $\overline{WR}$ (WR THR) to Reset Interrupt	T_{HR}	100pF Load	—	193	nS
Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	T_{IR}	100pF Load	—	250	nS
Delay from Initial Write INTR Reset to Transmit Start	T_{IRS}		1	8	B.C.
Delay from Initial Write to Interrupt	T_{SI}		9	16	B.C.
Delay from Stop to Interrupt (THRE)			8	8	B.C.
Modem Control					B.C. = BAUDOUT Cycles
Delay from WR, $\overline{WR}$ (WR MCR) to Output	T_{MDO}	100pF Load	—	200	nS
Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	T_{RIM}	100pF Load	—	250	nS
Delay to Set Interrupt from MODEM Input	T_{SIM}	100pF Load	—	250	nS

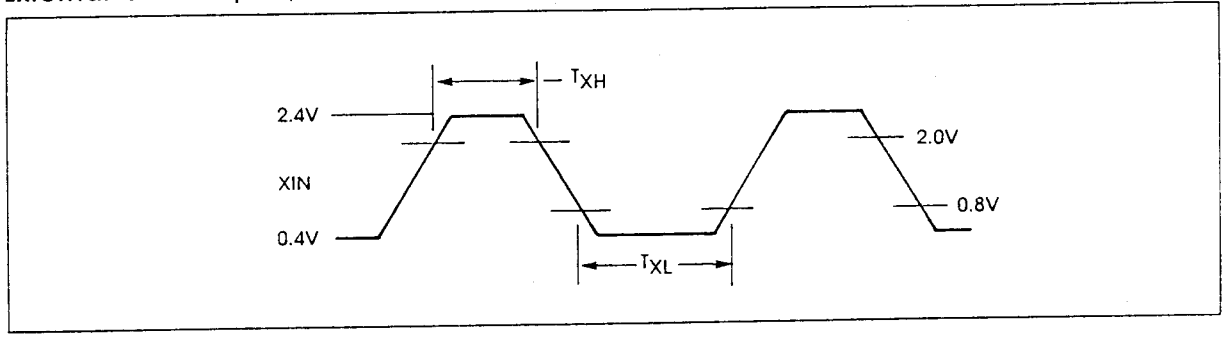
Notes:

1. Applicable only when $\overline{ADS}$ is tied low.
2. Charge and dischange time is determined by V_{OL}, V_{OH} and the external loading.

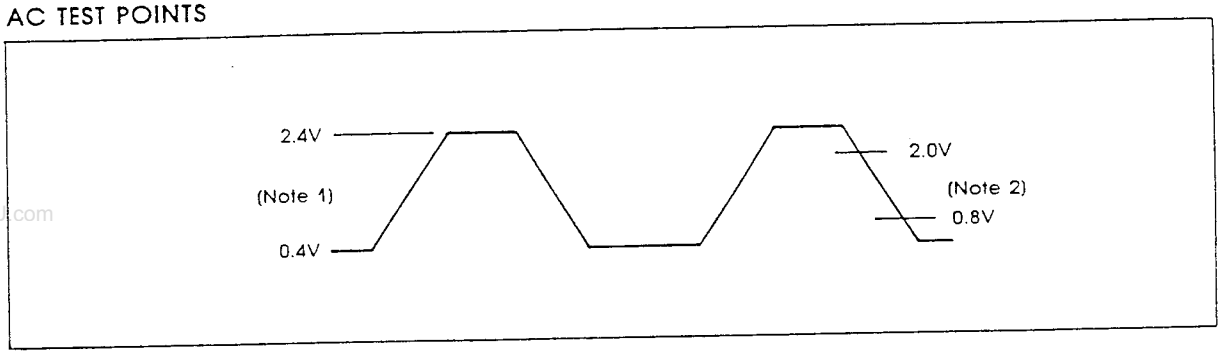
TIMING WAVEFORM

(All timings are referenced to valid 0 and valid 1)

External Clock Input (3.1 MHz Max.)



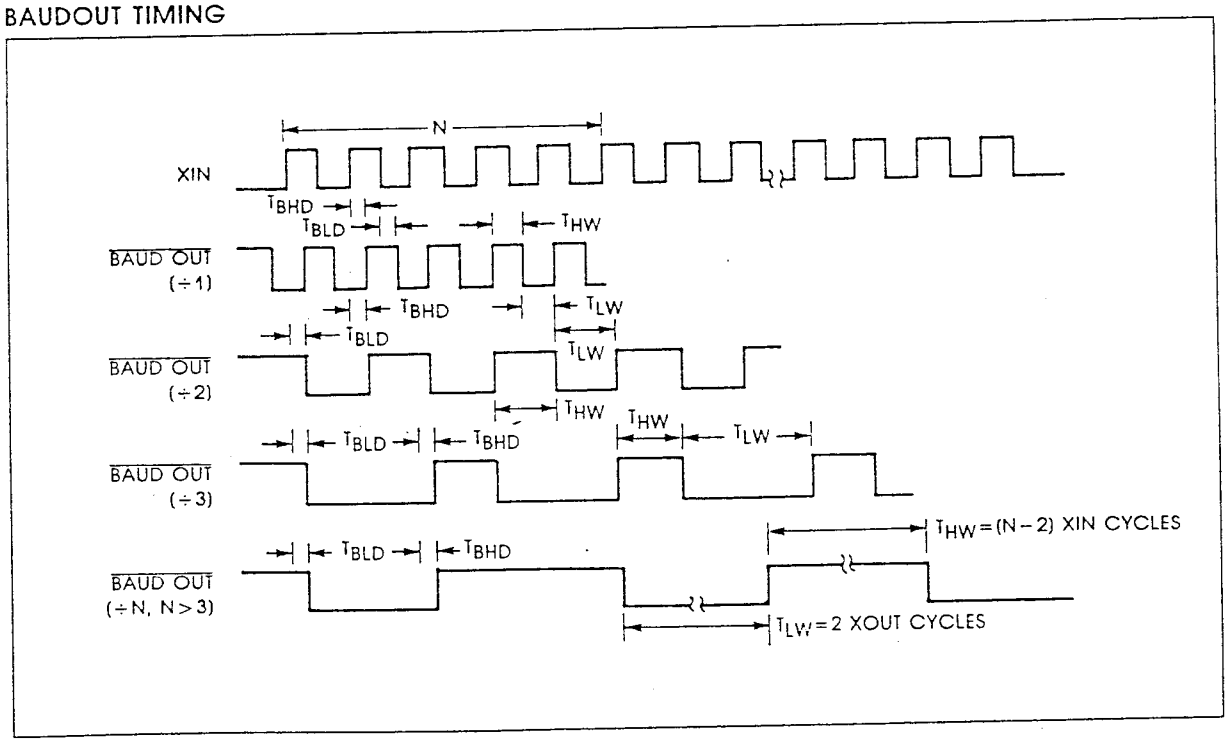
AC TEST POINTS



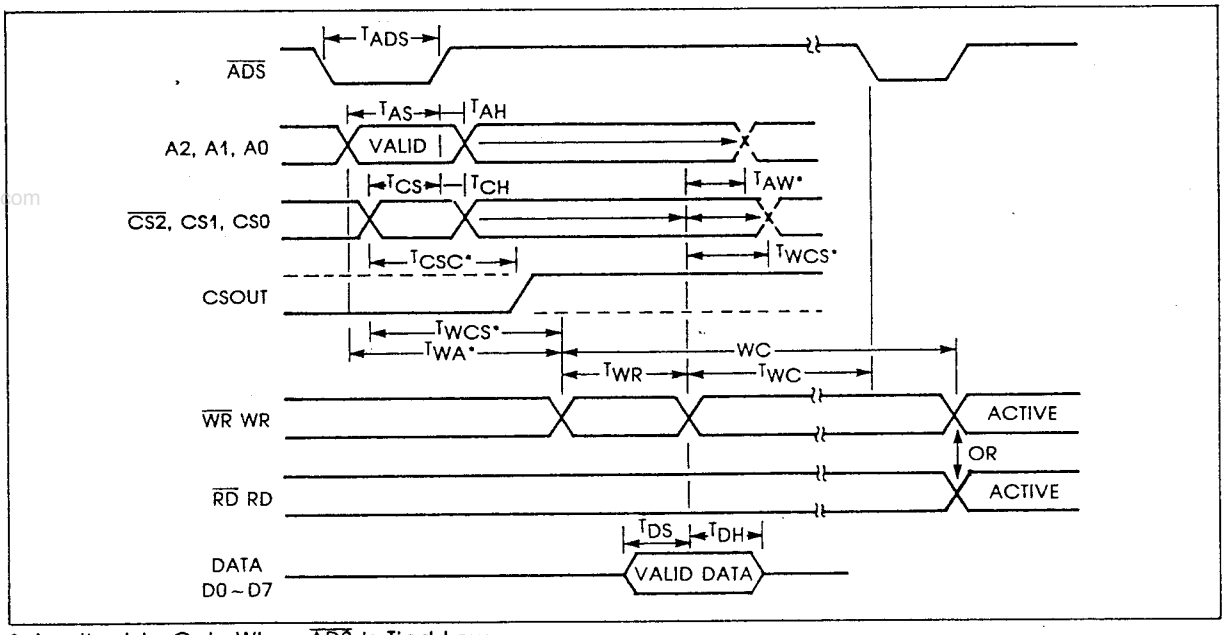
Notes:

1. The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
2. The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

BAUDOUT TIMING

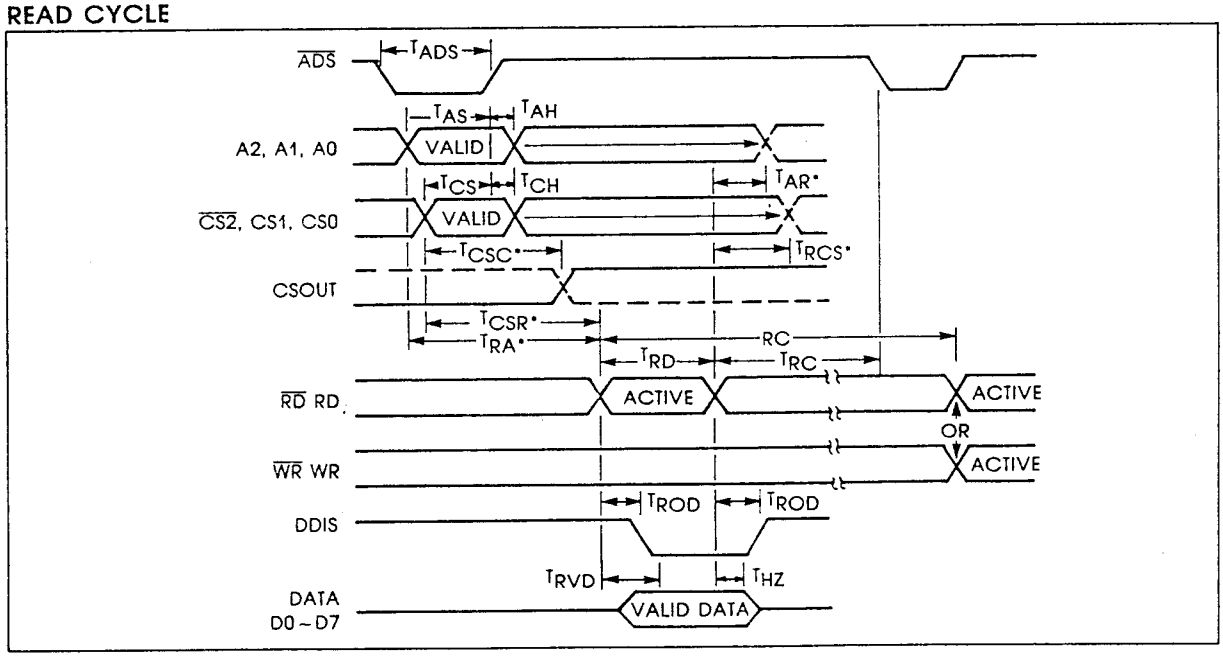


WRITE CYCLE



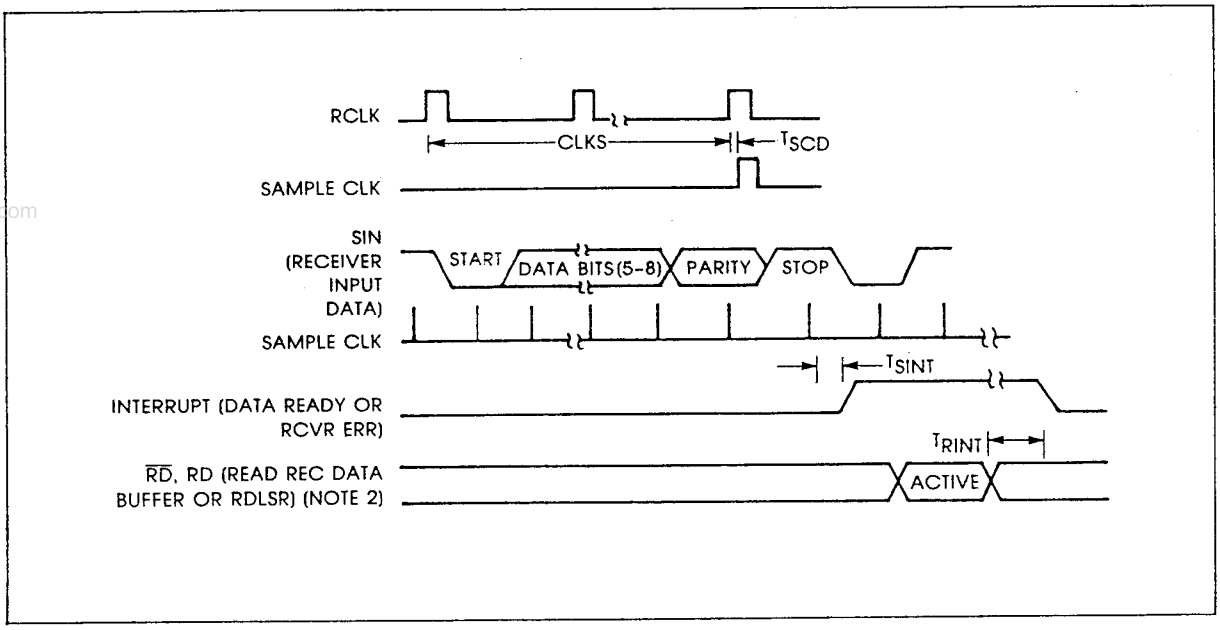
* Applicable Only When $\overline{ADS}$ is Tied Low.

READ CYCLE

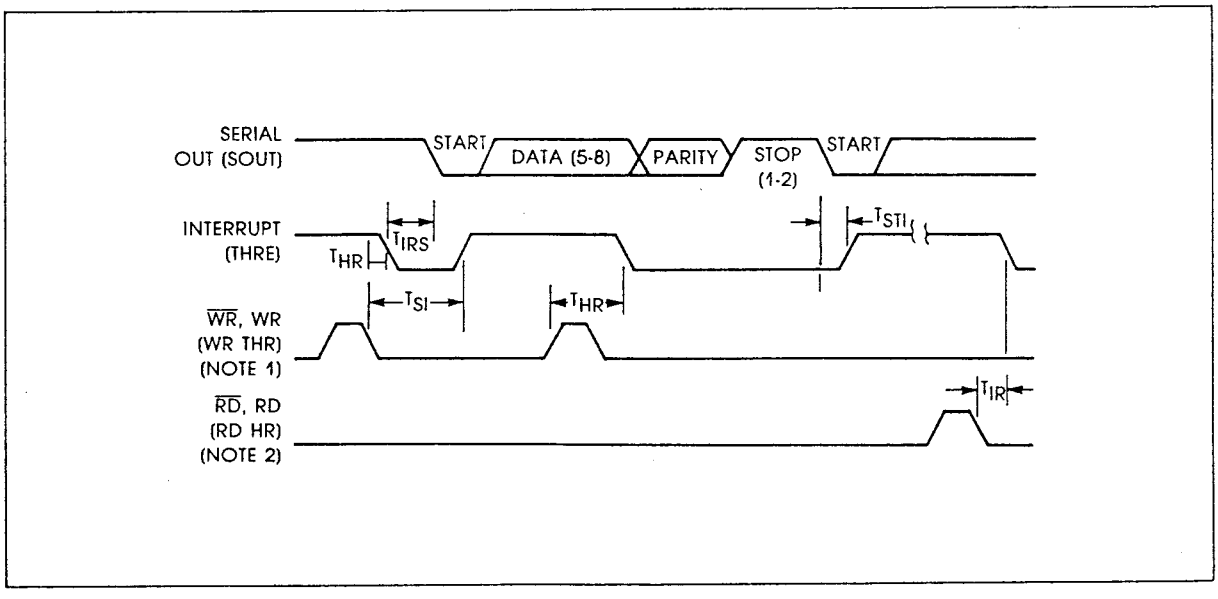


* Applicable Only When $\overline{ADS}$ is tied Low.

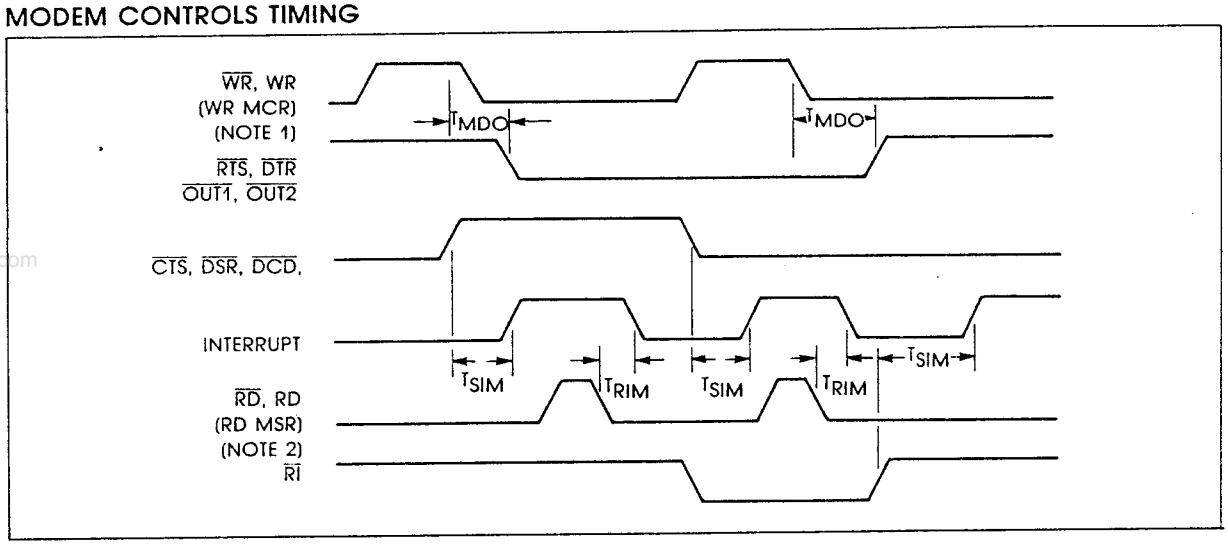
RECEIVER TIMING



TRANSMITTER TIMING



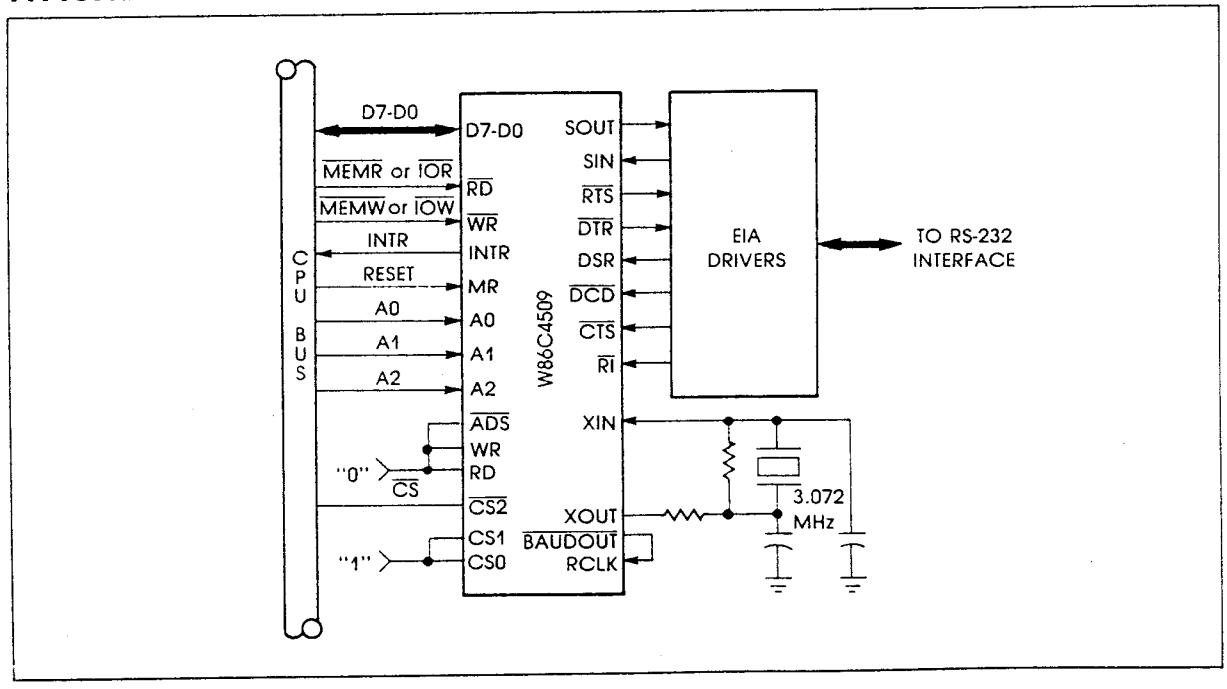
MODEM CONTROLS TIMING



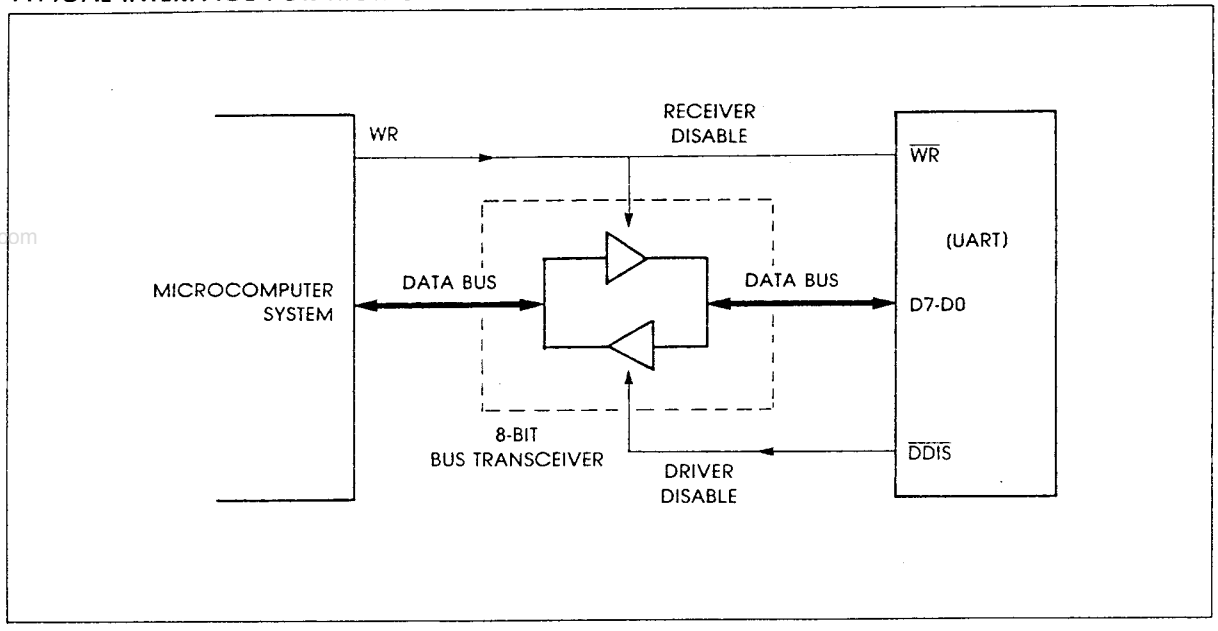
Notes:

1. See Write Cycle Timing
2. See Read Cycle Timine

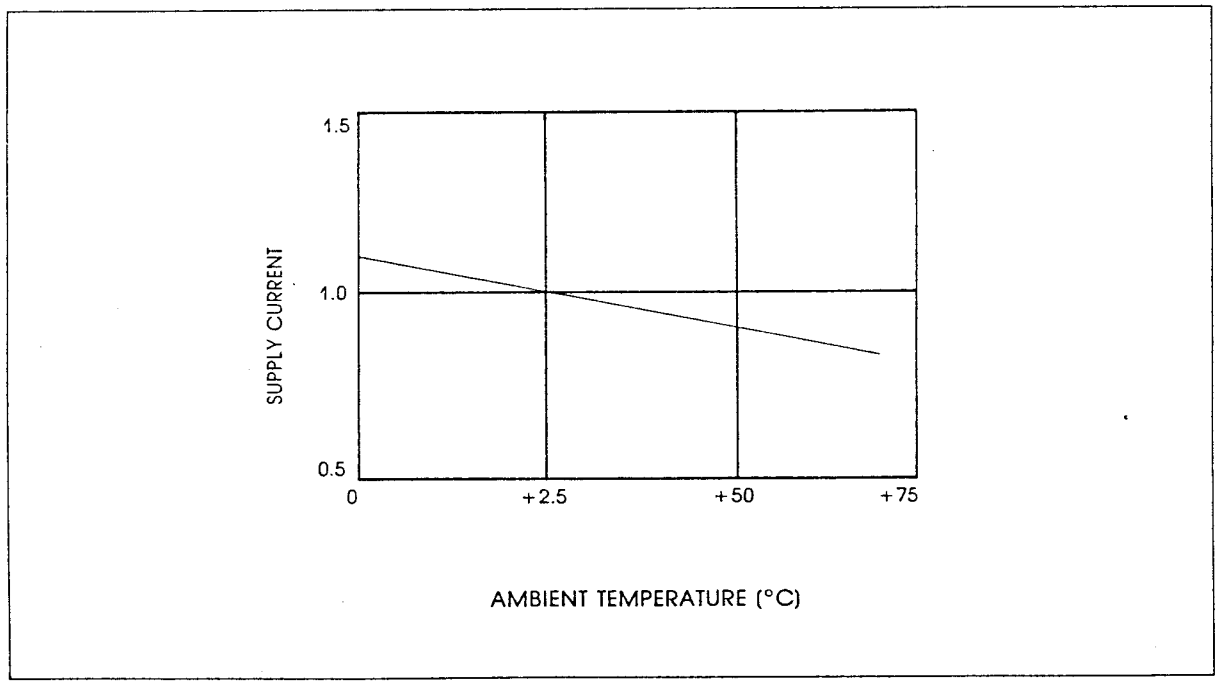
TYPICAL APPLICATION



TYPICAL INTERFACE FOR HIGH-CAPACITY DATA BUS

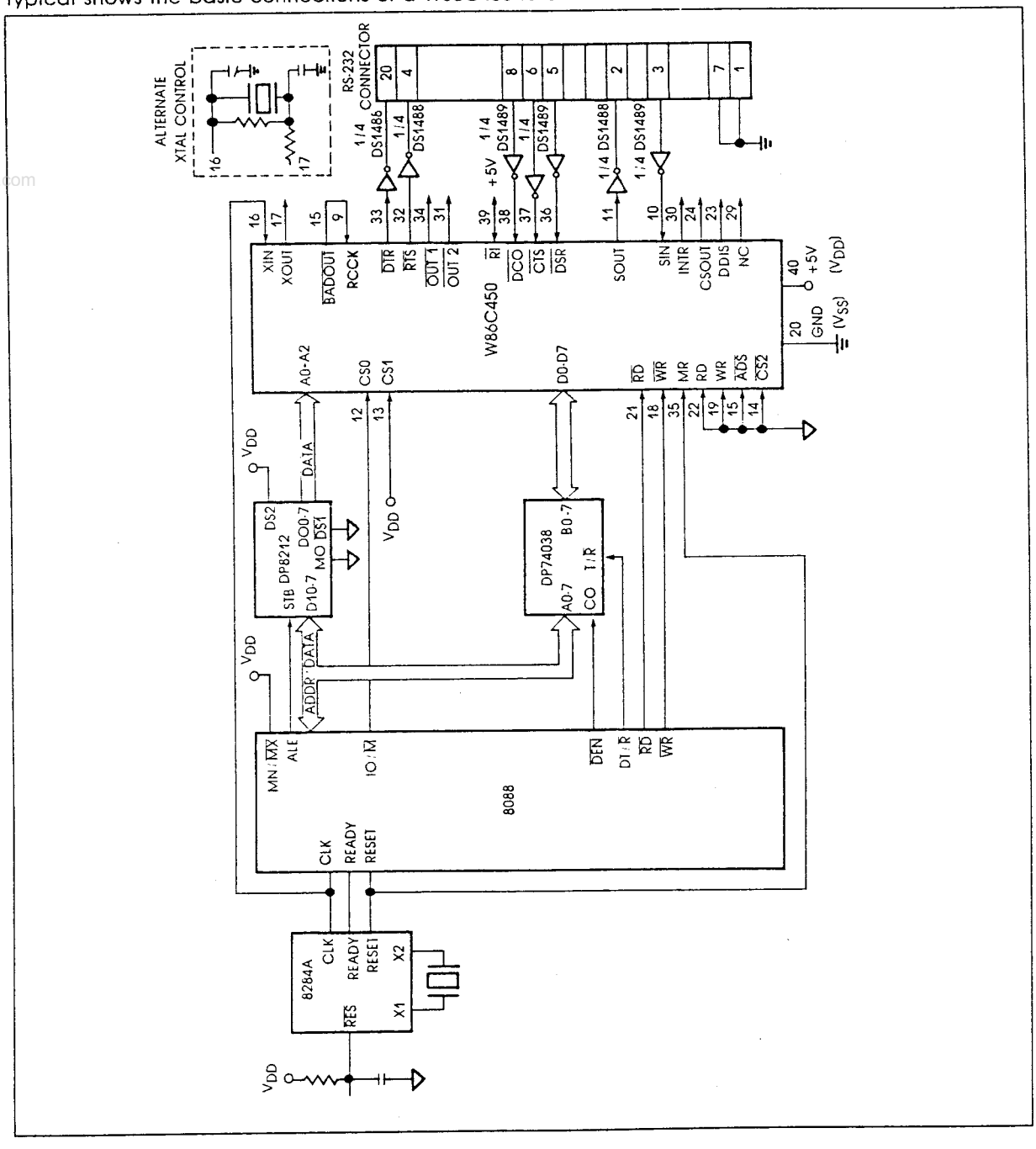


TYPICAL SUPPLY CURRENT VS TEMPERATURE, NORMALIZED



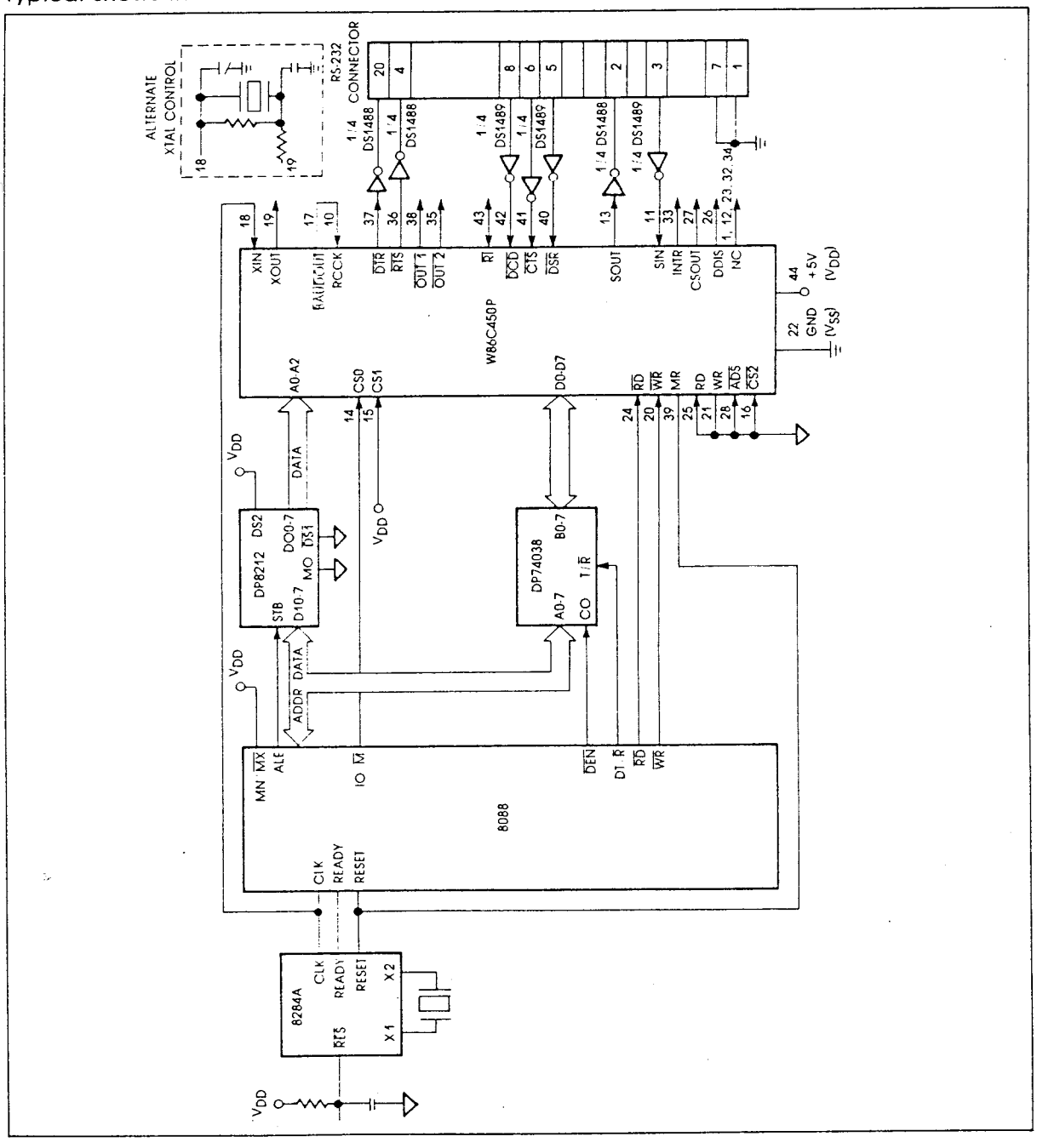
TYPICAL APPLICATION

Typical shows the basic connections of a W86C450 to an 8088 CPU



TYPICAL APPLICATION (Continued)

Typical shows the basic connections of a W86C450P to an 8088 CPU



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Note: All data and specifications are subject to change without notice