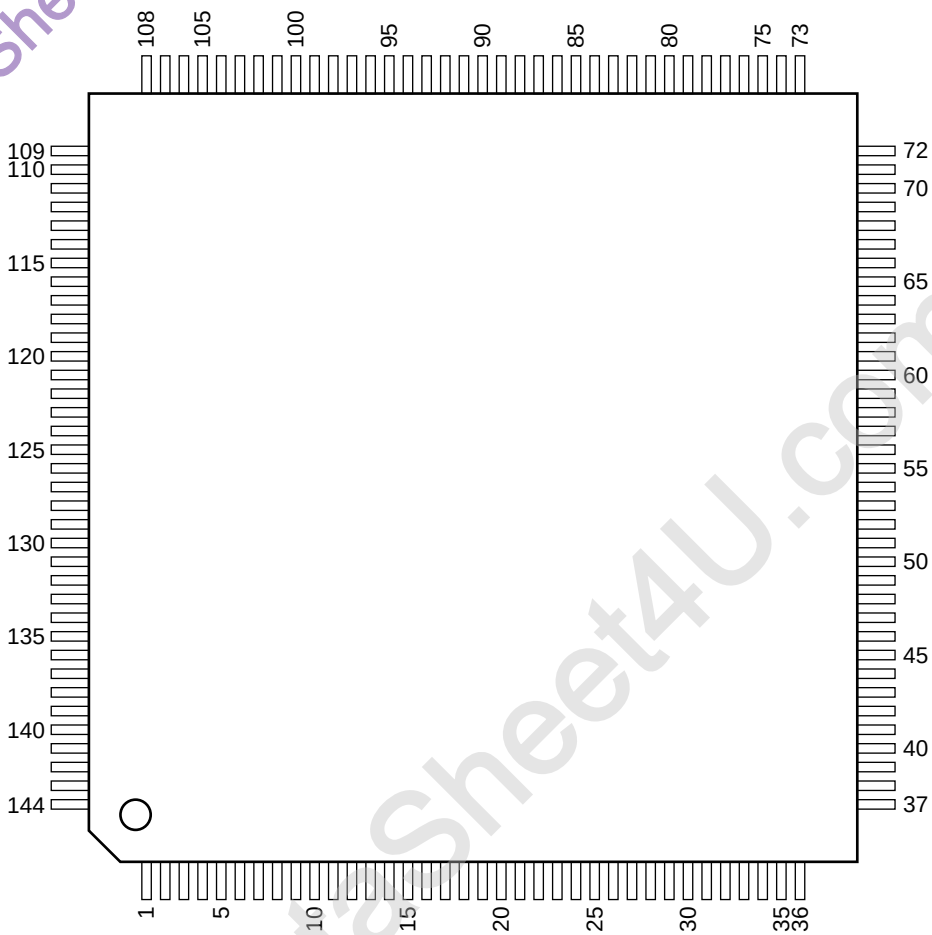
ETHERNET LAN CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VCC	49	I/O	C BE L2	97	I/O	BR AD2
2	—	VCC	50	I/O	FRAME L	98	I/O	BR AD1
3	—	GND	51	I/O	IRDY L	99	I/O	BR AD0
4	O	TP TD−−	52	I/O	TRDY L	100	I/O	GEP0/AUI BNC
5	O	TP TD−	53	—	GND	101	I/O	GEP1/ACTIV
6	O	TP TD+	54	—	VCC	102	I/O	GEP2/RCV MATCH/WAKE
7	O	TP TD++	55	I/O	DEVSEL L	103	I/O	GEP3/LINK
8	—	VCC	56	I/O	STOP L	104	—	GND
9	I	TP RD+	57	I/O	PERR L	105	O	XTAL2
10	I	TP RD−	58	O/D	SERR L	106	I	XTAL1
11	I	TCK	59	I/O	PAR	107	—	VCC
12	I	TMS	60	I/O	C BE L1	108	I	IREF
13	I	TDI	61	I/O	AD15	109	—	ACVCC
14	O	TDO	62	I/O	AD14	110	I	VCAP H
15	I	INT L	63	—	GND	111	—	ACVCC
16	I	RST I	64	I/O	AD13	112	I	SR DO
17	—	GND	65	I/O	AD12	113	O	SR DI
18	—	VCC	66	I/O	AD11	114	O	SR CK
19	I	PCI CLK	67	—	VCC	115	O	SR CS
20	—	VCC CLAMP	68	I/O	AD10	116	—	GND
21	I	GNT L	69	I/O	AD9	117	I	MII CRS/SD
22	O	REQ L	70	I/O	AD8	118	I	MII CLSN/SYM RXD4
23	I/O	AD31	71	—	GND	119	O	MII/SYM TXD3
24	I/O	AD30	72	—	VCC	120	O	MII/SYM TXD2
25	I/O	AD29	73	—	VCC	121	O	MII/SYM TXD1
26	—	VCC	74	—	GND	122	O	MII/SYM TXD0
27	I/O	AD28	75	I/O	C BE L0	123	O	MII TXEN/SYM TXD4
28	I/O	AD27	76	I/O	AD7	124	I	MII/SYM TCLK
29	I/O	AD26	77	I/O	AD6	125	—	VCC
30	—	GND	78	I/O	AD5	126	—	GND
31	I/O	AD25	79	—	VCC	127	I/O	MII RX ERR/SEL10 100
32	I/O	AD24	80	I/O	AD4	128	I	MII/SYM RCLK
33	I/O	C BE L3	81	I/O	AD3	129	I	MII DV
34	I	IDSEL	82	I/O	AD2	130	I	MII/SYM RXD3
35	—	GND	83	—	GND	131	I	MII/SYM RXD2
36	—	VCC	84	I/O	AD1	132	I	MII/SYM RXD1
37	—	VCC	85	I/O	AD0	133	I	MII/SYM RXD0
38	—	GND	86	I/O	CLKRUN L	134	O	MII MDC
39	I/O	AD23	87	O	BR CE L	135	I/O	MII MDIO
40	I/O	AD22	88	O	BR A0/CB PADS L	136	—	VCC
41	I/O	AD21	89	O	BR A1	137	I	AUI CD+
42	—	GND	90	I/O	BR AD7	138	I	AUI CD−
43	I/O	AD20	91	I/O	BR AD6	139	I	AUI RD+
44	I/O	AD19	92	I/O	BR AD5	140	I	AUI RD−
45	I/O	AD18	93	I/O	BR AD4	141	—	VCC
46	—	VCC	94	—	GND	142	O	AUI TD+
47	I/O	AD17	95	—	VCC	143	O	AUI TD−
48	I/O	AD16	96	I/O	BR AD3	144	—	GND

INPUTS

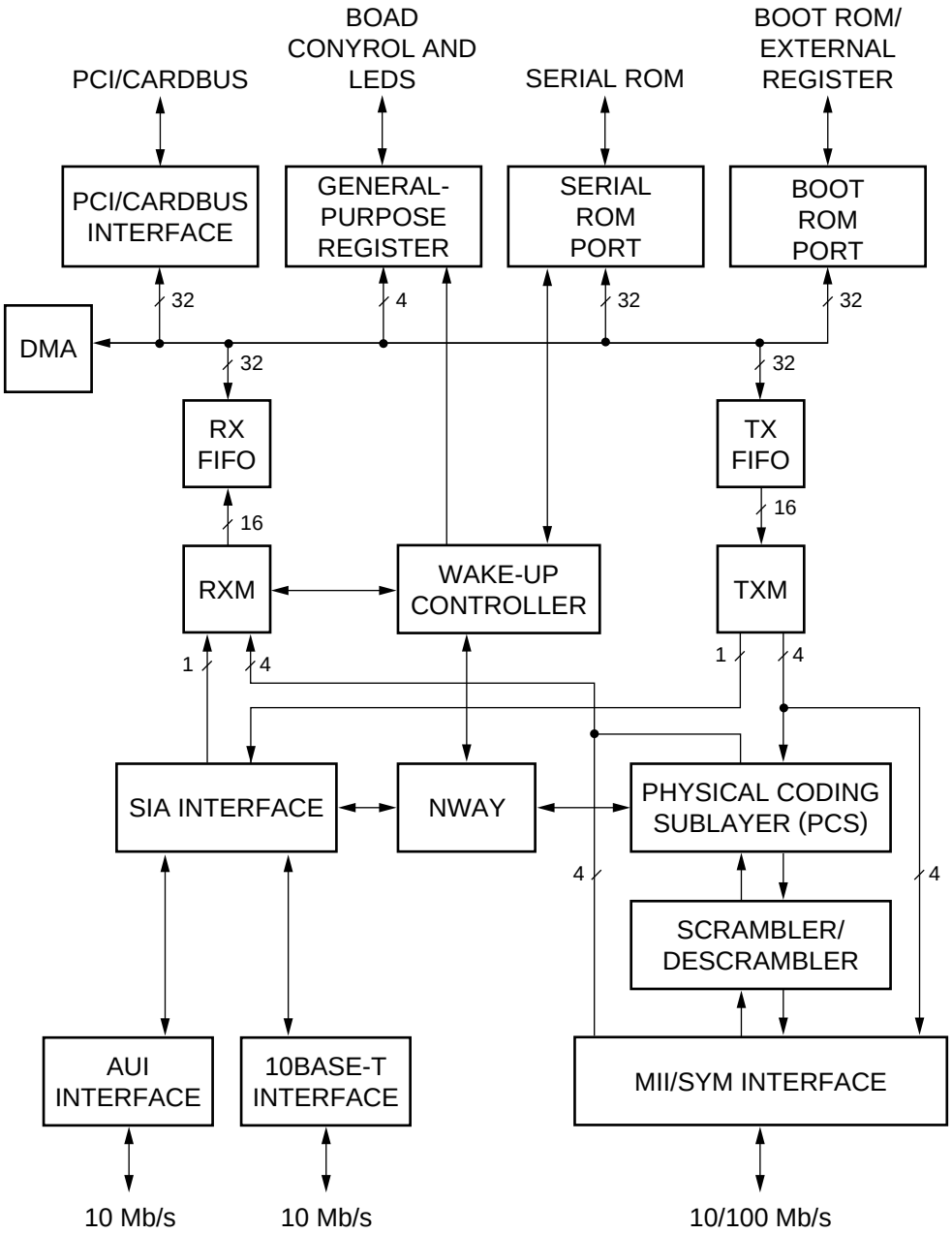
AUI CD–	: ATTACHMENT UNIT INTERFACE RECEIVE COLLISION DIFFERENTIAL NEGATIVE DATA
AUI CD+	: ATTACHMENT UNIT INTERFACE RECEIVE COLLISION DIFFERENTIAL POSITIVE DATA
AUI RD–	: ATTACHMENT UNIT INTERFACE RECEIVE DIFFERENTIAL NEGATIVE DATA
AUI RD+	: ATTACHMENT UNIT INTERFACE RECEIVE DIFFERENTIAL POSITIVE DATA
GNT L	: BUS GRANT
IDSEL	: INITIALIZATION DEVICE SELECT
IREF	: CURRENT REFERENCE
MII CLSN/SYM RXD4	: COLLISION ASSERT/SYMBOL DATA RECEIVE
MII CRS/SD	: CARRIER SENSE/SIGNAL DETECT
MII DV	: DATA VALID
MII/SYM RCLK	: RECEIVE CLOCK
MII/SYM RXD0 - SYM RXD3	: PARALLEL RECEIVE DATA
MII/SYM TCLK	: TRANSMIT CLOCK
PCI CLK	: CLOCK
RST I	: RESET
SR DO	: SERIAL ROM DATA
TCK	: JTAG CLOCK
TDI	: JTAG DATA
TMS	: JTAG TEST MODE SELECT
TP RD–	: TWISTED-PAIR NEGATIVE DIFFERENTIAL RECEIVE DATA
TP RD+	: TWISTED-PAIR POSITIVE DIFFERENTIAL RECEIVE DATA
VCAP H	: CAPACITOR FOR ANALOG PHASE-LOCKED LOOP LOGIC
XTAL1	: CRYSTAL OSCILLATOR

OUTPUTS

AUI TD–	: ATTACHMENT UNIT INTERFACE TRANSMIT DIFFERENTIAL NEGATIVE DATA
AUI TD+	: ATTACHMENT UNIT INTERFACE TRANSMIT DIFFERENTIAL POSITIVE DATA
BR A0, BR A1	: BOOT ROM ADDRESS
BR CE L	: BOOT ROM OR EXTERNAL REGISTER CHIP ENABLE
CB PADS L	: PCI/CARD BUS
MII MDC	: MANAGEMENT DATA CLOCK
MII TXEN/SYM TXD4	: TRANSMIT ENABLE/TRANSMIT DATA
MII/SYM TXD0 - SYM TXD3	: PARALLEL TRANSMIT DATA
REQ L	: BUS REQUEST
SR CK	: SERIAL ROM CLOCK
SR CS	: SERIAL ROM CHIP-SELECT
SR DI	: SERIAL ROM DATA
TDO	: JTAG DATA
TP TD–, TP TD––	: TWISTED-PAIR NEGATIVE DIFFERENTIAL TRANSMIT DATA
TP TD+, TP TD++	: TWISTED-PAIR POSITIVE DIFFERENTIAL TRANSMIT DATA
XTAL2	: CRYSTAL OSCILLATOR

INPUTS/OUTPUTS

ACTIV	: LED ACTIVITY
AD0 - AD31	: PCI ADDRESS AND DATA
AUI BNC	: BNC (10BASE2) SELECT
BR AD0 - BR AD7	: BOOT ROM ADDRESS
C BE L0 - C BE L3	: BUS COMMAND AND BYTE ENABLE
CLKRUN L	: PCI/CARD BUS CLOCK RUN INDICATION
DEVSEL L	: DEVICE SELECT
FRAME L	: FRAME
GEP0 - GEP3	: INTERRUPT
LINK	: NETWORK LINK
INT L	: INTERRUPT REQUEST
IRDY L	: INITIATOR READY
MII MDIO	: MANAGEMENT DATA INPUT/OUTPUT TRANSFERS CONTROL INFORMATION AND STATUS
MII RX ERR/SEL10 100	: RECEIVE ERROR/10BASE-100BASE SELECT
PAR	: PARITY
PERR L	: PARITY ERROR
RCV MATCH	: RECEIVE PACKET HAS PASSED
SERR L	: SYSTEM ERROR
STOP L	: STOP INDICATOR
TRDY L	: TARGET READY
WAKE	: WAKE UP EVENT


PCI/CARDBUS
BOAD CONYROL AND LEDS
SERIAL ROM
BOOT ROM/ EXTERNAL REGISTER
PCI/CARDBUS INTERFACE
GENERAL-PURPOSE REGISTER
SERIAL ROM PORT
BOOT ROM PORT
32
4
32
32
DMA
32
32
RX FIFO
TX FIFO
16
16
RXM
WAKE-UP CONTROLLER
TXM
1
4
1
4
SIA INTERFACE
NWAY
PHYSICAL CODING SUBLAYER (PCS)
4
4
SCRAMBLER/ DESCRAMBLER
AUI INTERFACE
10BASE-T INTERFACE
MII/SYM INTERFACE
10 Mb/s
10 Mb/s
10/100 Mb/s