M5L8288P

T-52-33-55

MITSUBISHI(MICMPTR/MIPRC)

BUS CONTROLLER

DESCRIPTION

The M5L8288P is a semiconductor integrated circuit consisting of a bus controller and bus driver for the MELPS 86, 88, 16-bit microprocessors. By using the status signals from the CPU a Multibus (Intel trademark) control signal is generated.

FEATURES

- High-fanout outputs
  Command output I_{OL}=32mA, I_{OH}=−5mA
  Control output I_{OL}=16mA, I_{OH}=−1mA
- Advanced command outputs ($\overline{AIOWC}$ and $\overline{AMWC}$ outputs)
- Low power dissipation

APPLICATION

Bus controller and bus driver for maximum mode operation of the MELPS 86, 88

FUNCTION

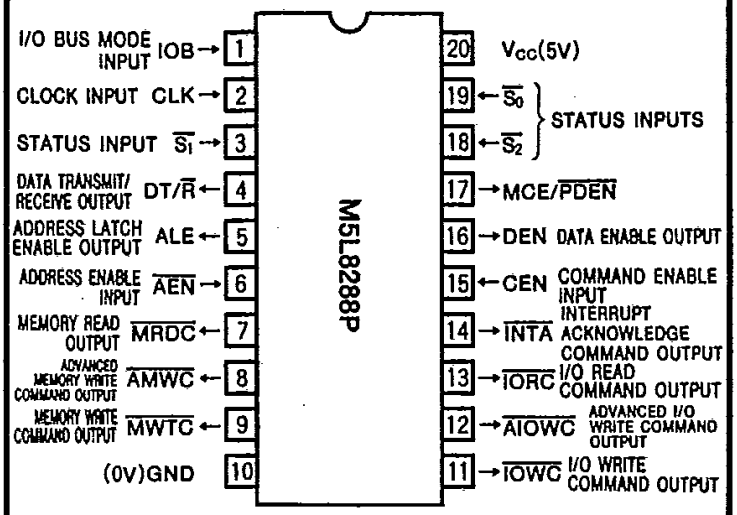
The M5L8288P is a bus controller and driver for maximum mode operation of theMELPS 86, 88 processors.

The command signals and control signals are decoded by means of the $\overline{S_0}$~$\overline{S_2}$ outputs from the CPU and the control signals for I/O devices and memory are output.

The device can be used in the Multimaster mode in which several CPUs acting as masters are connected to one data bus. An input pin for the control signal $\overline{AEN}$ from an 8289 bus arbiter is provided.

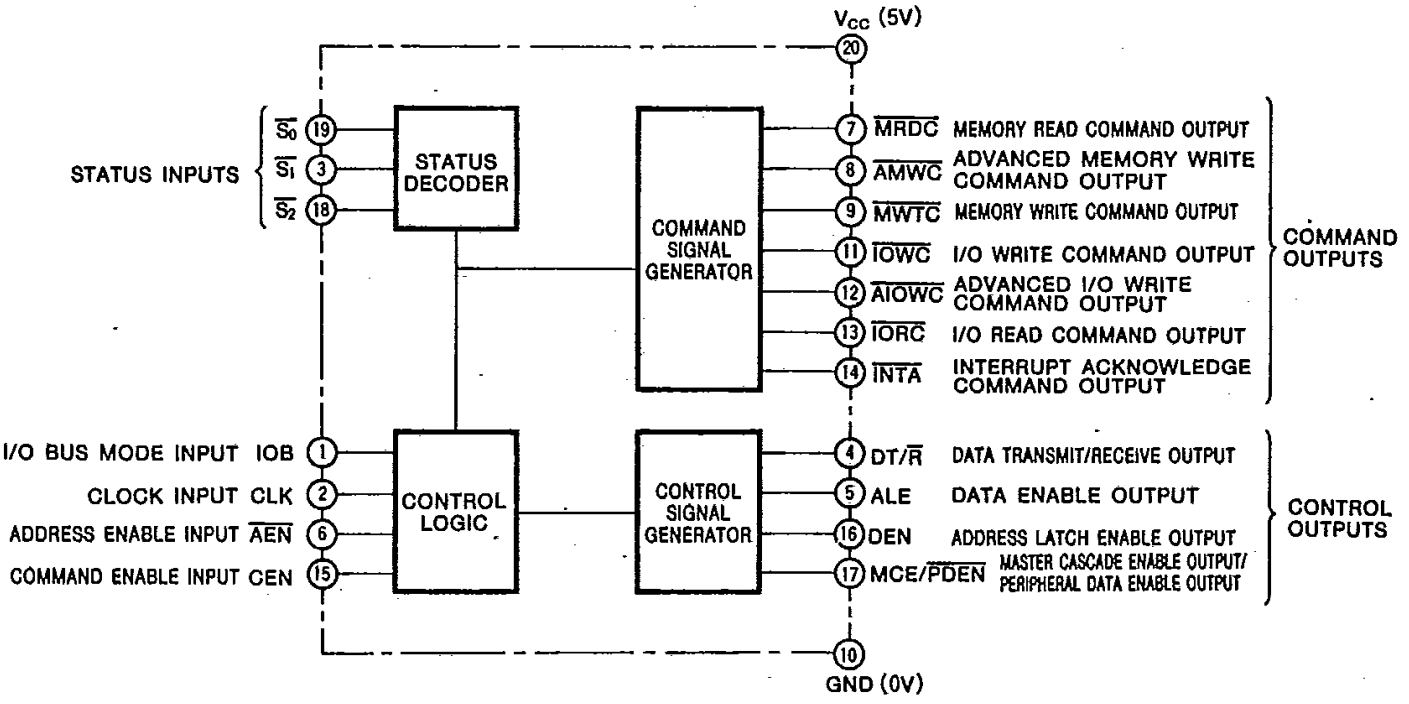
By using the M5L8288P as a bus controller, a highperformance 16-bit microcomputer system can be configured.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Name	Input of output	Functions
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status Input	Input	These are connected to the CPU status output $\overline{S_0}$~$\overline{S_2}$. The M5L8288P uses these signals to generate the proper timing command signals and control signals. All pins are provided with internal pull-up resistors.
CLK	Clock input	Input	Used to connect the clock generator M5L8284AP clock output CLK. All outputs of the M5L8288S change in synchronization with the clock input.
ALE	Address latch enable output	Output	Provides the strobe signal output for the address latches. This pin is connected to the STB pin of the M5L8282P or M5L8283P and used to latch the address from the CPU. When using any other address latch, the following conditions must be satisfied. 1. The enable input must be active high. 2. Data reading is always performed while the enable input is high. 3. The latching operation is performed as the enable input goes from high to low.
DEN	Data enable	Output	Provides the data enable signal for the local bus or a data transceiver on the system bus. Operates in active high mode.
DT/$\overline{R}$	Data transmit/receive control output	Output	Controls the flow of data between CPU and memory or peripheral I/O devices. When this pin is high, the CPU can write data to the peripheral devices. When it is low, it can read data from the peripheral devices. It is connected to the transmit input T of the M5L8286P or M5L8287P bus transceivers.
$\overline{AEN}$	Address enable input	Input	When the IOB input is low and the $\overline{AEN}$ input is set to high, all command outputs are put in the high-impedance state. When the IOB input is high, there is no effect on the $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, and $\overline{INTA}$ outputs, the command output other than these four going into the high-impedance state. None of the command outputs will go low until at least 115ns after $\overline{AEN}$ transits from high to low.
CEN	Command enable input	Input	When this pin is set to low, all command outputs and DEN are prohibited by the $\overline{PDEN}$ control output (not high-impedance state). When set to high, the above outputs are enabled.
IOB	Input/output bus mode input	Input	When this pin is set to high, the M5L8288P functions in the I/O bus mode, and when set to low it functions in the system bus mode. (The I/O bus mode and system bus mode are described in the functional description)
$\overline{AIOWC}$	Advanced I/O write command output	Output	The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction its timing is the same as a read command signal. Active low.
$\overline{IOWC}$	I/O write command output	Output	Instructs an I/O device to read the data on the data bus. Active low.
$\overline{IORC}$	I/O read command output	Output	Instructs an I/O device to drive its data onto the data bus. Active low.
$\overline{AMWC}$	Advanced write command output	Output	The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. Active low.
$\overline{MWTC}$	Memory write command output	Output	Provides a write instruction to memory for the current data on the bus. Active low.
$\overline{MRDC}$	Memory read command output	Output	Provides an output instruction to memory for the present data on the bus. Active low.
$\overline{INTA}$	Interrupt acknowledge command output	Output	This output informs an interrupting device that it has accepted the interrupt, outputting a vector address output instruction to the data bus. $\overline{IORC}$ operates in the same manner for interrupt cycles. Active low.
MCE/ $\overline{PDEN}$	Master cascade Enable output/ Peripheral data Enable output	Output	This output pin has two functions. 1. When the IOB input is set to low: The MCE function is enabled. The signal acts as the enable signal which allows a slave PIC (M5L8259AP) to read the cascade address output to the bus by the master PIC during an interrupt sequence. Active high. 2. When the IOB input is set to high: The $\overline{PDEN}$ function is enabled. This output provides the enable signal to the data bus transceiver connected to the I/O interface bus when an instruction occurs ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$). Operates the same way as DEN with respect to the system bus.

FUNCTIONAL DESCRIPTION

The state of the command outputs and control outputs are determined by the CPU status outputs $\overline{S_0} \sim \overline{S_2}$. The table summarizes the states of the outputs $\overline{S_0} \sim \overline{S_2}$ and their corresponding valid command output names.

Depending upon whether the M5L8288S is in the I/O bus mode or system bus mode, the command output sequence will vary.

STATUS INPUTS AND COMMAND OUTPUTS RELATIONSHIPS

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	8086, 8088 status	Valid command output name
L	L	L	Interrupt acknowledge	$\overline{INTA}$
L	L	H	Data read from an I/O port	$\overline{IORC}$
L	H	L	Data write to an I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
L	H	H	Halt	—
H	L	L	Instruction fetch	$\overline{MRDC}$
H	L	H	Read data from memory	$\overline{MRDC}$
H	H	L	Write data to memory	$\overline{MWTC}$, $\overline{AMWC}$
H	H	H	Passive state	—

1. I/O bus mode operation

When IOB is high, the M5L8288S function in the I/O bus mode.

In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 8288 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

2. System bus mode operation

When IOB is set to low, the M5L8288S enters the system bus mode. In this mode no command is issued until 115 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

3. $\overline{AMWC}$ and $\overline{AIOWC}$ outputs

With respect to the normal write control signals $\overline{MWTC}$ and $\overline{IOWC}$, the advanced-write command signals $\overline{AMWC}$ and $\overline{AIOWC}$ transit low one clock cycle earlier and remain low for two clock cycles.

These signals are used with peripheral devices or static RAM devices which require a long write pulse, so that the CPU does not go into an unnecessarily wait cycle.

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+5.5	V
V_O	Output voltage		−0.5~V_{CC}	V
P_d	Power dissipation		1.5	W
T_{opr}	Operating free-air temperature range		0~75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current	Command outputs			−5	mA
		Control outputs			−1	
I_{OL}	Low-level output current	Command outputs			32	mA
		Control outputs			16	

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage						−1	V
V_{OH}	High-level output voltage	Command outputs	V_{CC}=4.5V, V_I=2V	I_{OH}=−5mA	2.4			V
		Control outputs	V_I=0.8V	I_{OH}=−1mA	2.4			
V_{OL}	Low-level output voltage	Command outputs	V_{CC}=4.5V, V_I=2V	I_{OL}=32mA			0.5	V
		Control outputs	V_I=0.8V	I_{OL}=16mA			0.5	
I_{IH}	High-level input voltage		V_{CC}=5.5V, V_I=5.5V				50	μA
I_{IL}	Low-level input voltage		V_{CC}=5.5V, V_I=0.45V				−0.7	mA
I_{OZH}	Off-state output current with high-level applied to output		V_{CC}=5.5V, V_O=5.25V				100	μA
I_{OZL}	Off-state output current with low-level applied to output		V_{CC}=5.5V, V_O=0.4V				−100	μA
I_{CC}	Supply current		V_{CC}=5.5V				160	mA

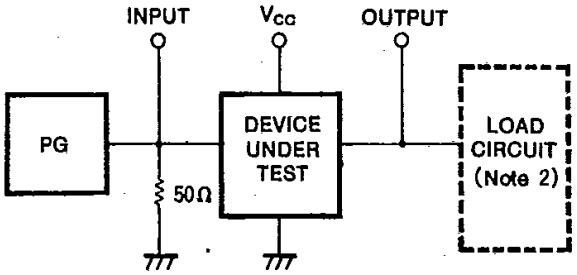
SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75°C, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Output low-level to high-level propagation time From CLK input to DEN output	TCVNV		5		45	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{PDEN}$ output						
t_{PLH}	Output low-level to high-level propagation time From CLK input to DEN output.	TCVNX		10		45	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{PDEN}$ output						
t_{PLH}	Output low-level to high-level propagation time From CLK input to ALE output	TCLLH				20	ns
t_{PLH}	Output low-level to high-level propagaion time From CLK input to MCE output	TCLMCH				20	ns
t_{PLH}	Output low-level to high-level propagation time From $\overline{S_0}$~$\overline{S_1}$ inputs to ALE output	TSVLH				20	ns
t_{PLH}	Output low-level to high-level propagation time From $\overline{S_0}$~$\overline{S_1}$ inputs to MCE output	TSVMCH				20	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to ALE output	TCHLL		4		15	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TCLML		10		35	ns
t_{PLH}	Output low-level to high-level propagation time From CLK input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TCLMH		10		35	ns
t_{PHL}	Output high-level to low-level propagation time From CLK input to DT/$\overline{R}$ output	TCHDTL	(Note 1)			50	ns
t_{PLH}	Output low-level to high-level propagation time From CLK input to DT/$\overline{R}$ output	TCHDTH				30	ns
t_{PZH}	High-level output enable time From $\overline{AEN}$ input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TAELCH				40	ns
t_{PHZ}	High-level output disable time From $\overline{AEN}$ input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TAEHCZ				40	ns
t_{PHL}	Output high-level to low-level propagation time From $\overline{AEN}$ input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$, and $\overline{IOWC}$ outputs	TAELCV		115		200	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time From $\overline{AEN}$ input to DEN output	TAEVNV				20	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time From CEN input to $\overline{DEN}$ and PDEN outputs	TCEVNV				25	ns
t_{PLH} t_{PHL}	Output low-level to high-level and high-level to low-level propagation time. From CEN input to $\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{MWTC}$, $\overline{AIOWC}$ and $\overline{IOWC}$ outputs	TCELRH				35	ns

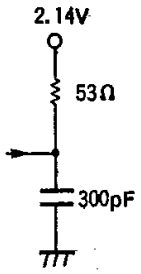
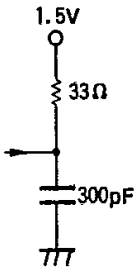
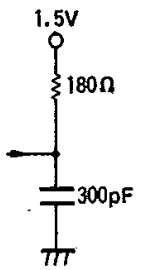
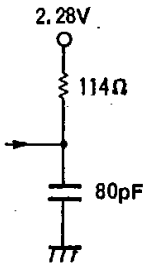
TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75°C, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
t_C	Clock CLK cycle time	TCLCL		100			ns
$t_{W(CLKL)}$	Clock CLK low pulse width	TCLCH		50			ns
$t_{W(CLKH)}$	Clock CLK high pulse width	TCHCL		30			ns
$t_{su(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ setup time with respect to T for the T_1 state	TSVCH		35			ns
$t_{h(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ hold time with respect to T for the T_4 state	TCHSV		10			ns
$t_{su(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ setup time with respect to T for the T_3 state	TSHCL		35			ns
$t_{h(\overline{S_0}\sim\overline{S_2})}$	$\overline{S_0}$~$\overline{S_2}$ hold time with respect to T for the T_3 state	TCLSH		10			ns

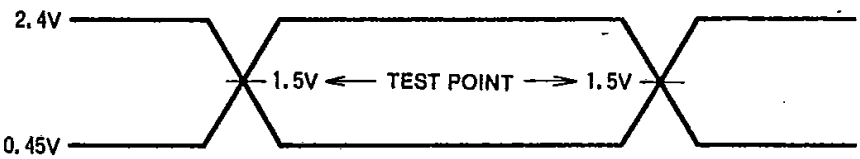
Note 1 : Test Circuit



Note 2

Load circuit	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
Command output load circuit			
Control output load circuit		—	—

Note 3 : AC TEST WAVE FORM

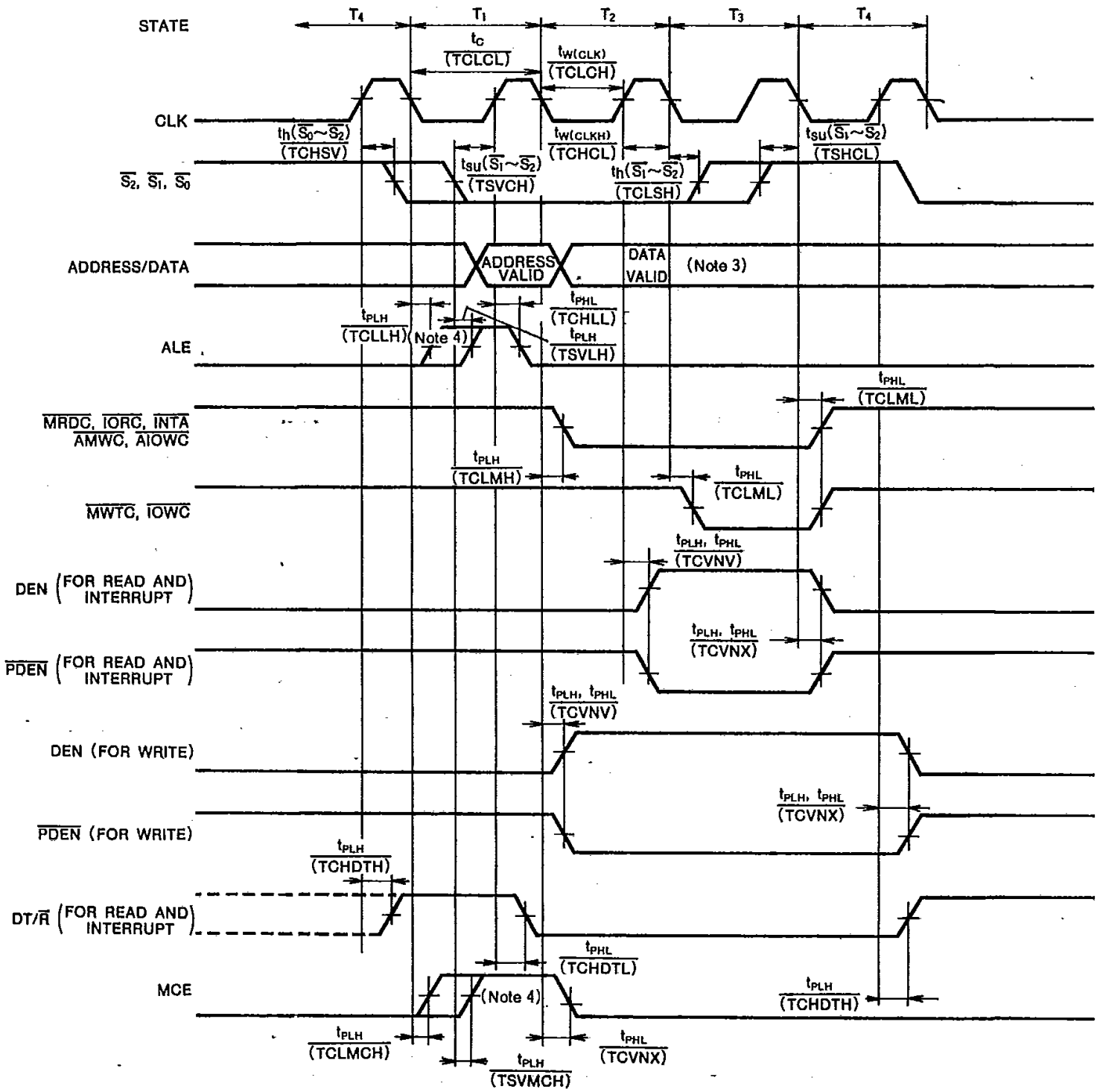


INPUT PULSE LEVEL : 0.45~2.4V

TIMING MEASUREMENT POINT : 1.5V

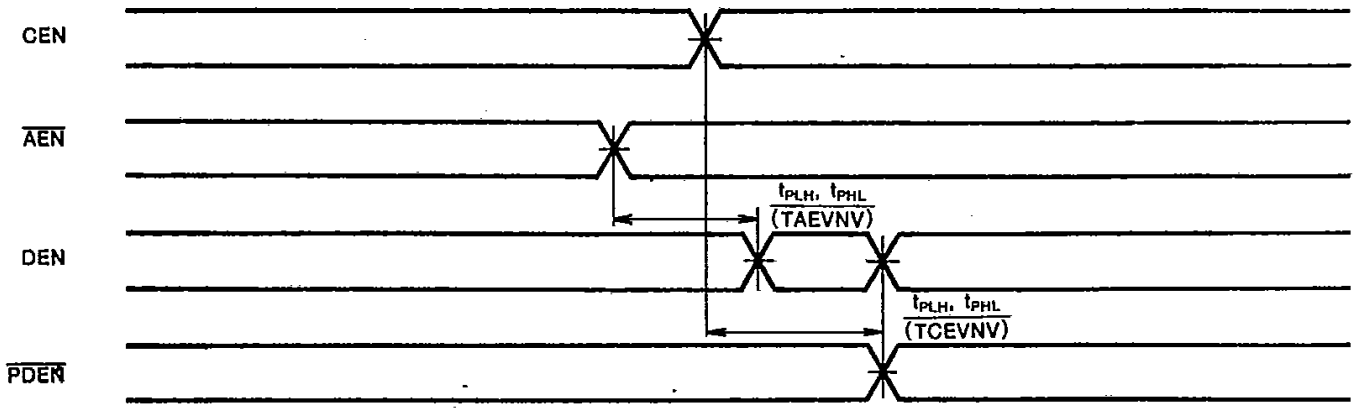
TIMING DIAGRAM

1. Command output timing

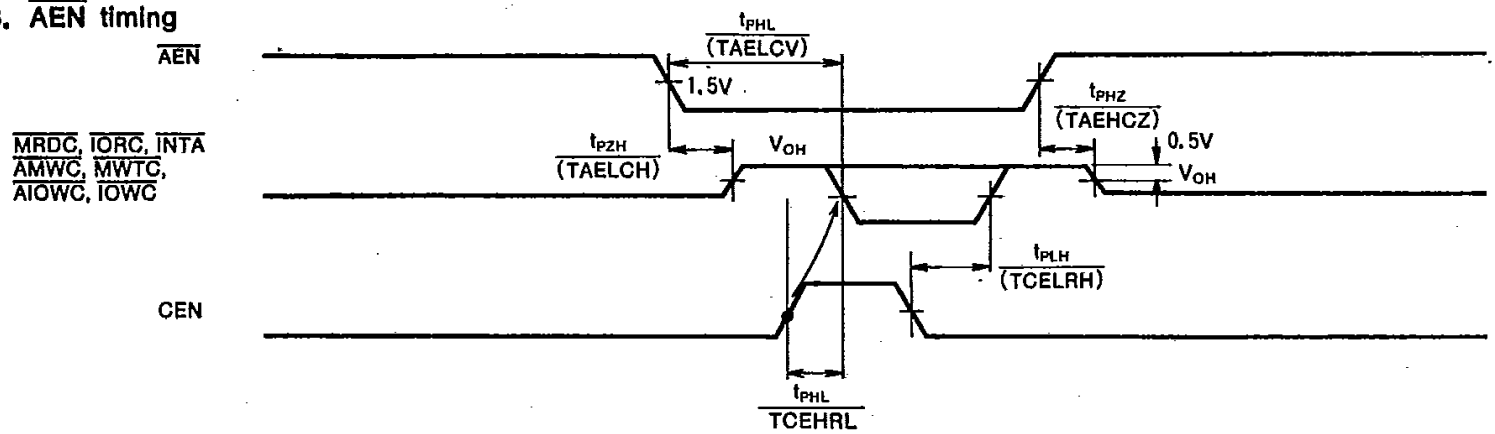


Note 3 : The address/data bus signals are shown only for reference.
4 : The ALE and MCE leading edge occurs in synchronization with the falling edge of CLK or $\overline{S_0}$~$\overline{S_2}$, whichever is later.
5 : Unless otherwise noted, the timing of all signals is respect to 1.5V

2. DEN and $\overline{PDEN}$ timing



3. $\overline{AEN}$ timing



Note 6 : CEN must be low or valid prior to T_2 to prevent the command from being generated.

APPLICATION EXAMPLE