NEC

NEC Electronics Inc.

μPD7519/19H 4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH FIP® CONTROLLER/DRIVER

Description

The μPD7519, 7519H, 75CG19, and 75CG19H are CMOS 4-bit, single-chip microcomputers with the μPD7500 series architecture and a FIP controller/driver. On-board peripheral functions include and 8-bit timer/event counter, an 8-bit serial interface, a 14-bit programmable pulse generator, and a display controller/driver that supervises all of the timing requirements of the 24 port S segment drivers either for a 16-character, 7-segment FIP, or an 8-character, 14-segment FIP.

Twenty-eight I/O lines are organized into seven 4-bit ports: the input serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, and 6.

The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values.

The μPD7519 has a 7.63 μs instruction cycle time at f_{xx} = 4.19 MHz. The μPD7519H/75CG19H has a 2.44 μs instruction cycle time at f_{xx} = 6.55 MHz.

Current consumption for the μPD7519 is less than 2 mA in normal operation (V_{DD} = 5 V ± 10%, f_{xx} = 4.19 MHz, high speed mode) and is further reduced in the halt and stop power-down modes. For the μPD7519H, current consumption is less than 6 mA for normal operation (V_{DD} = 5 V ± 10%, f_{xx} = 6.55 MHz, high speed mode).

The μPD75CG19/75CG19H piggyback EPROM version, is available for prototyping and program development. It is pin-compatible and functionally equivalent to the masked version.

Note: FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Features

- ☐ 4096 × 8-bit program memory (ROM)
- ☐ 256 × 4-bit data memory (RAM)
- ☐ 28 I/O lines
- ☐ Programmable FIP controller/driver
  - — 24 high-voltage output lines
- ☐ 8-bit serial interface
- ☐ 8-bit timer/event counter
- ☐ Programmable pulse generator (PPG)
  - — Variable duty port (D/A converter)
  - — Signal generator port
  - — 1-bit output port
- ☐ Vectored, prioritized interrupts
  - — Two external: INT0, INT1
  - — Two internal: timer (INTT) and serial (INTS)
- ☐ Four 4-bit general purpose registers
- ☐ 106 instructions; subset of μPD7500 series instructions set A
  - — Look-up-table capability
  - — Indirect indexed addressing
- ☐ Instruction cycle
  - — μPD7519 low speed mode: 15.26 μs/4.19 MHz
  - — μPD7519 high speed mode: 7.63 μs/4.19 MHz
  - — μPD7519H low speed mode: 15.26 μs/4.19 MHz
  - — μPD7519H low speed mode: 9.77 μs/6.55 MHz
  - — μPD7519H high speed mode: 3.81 μs/4.19 MHz
  - — μPD7519H high speed mode: 2.44 μs/6.55 MHz
- ☐ Two power-down modes
- ☐ Single power supply (2.5 V to 6.0 V)

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7519G-12	64-pin plastic miniflat	4.19 MHz
μPD7519G-36	64-pin plastic QUIP	4.19 MHz
μPD7519CW	64-pin plastic shrink DIP	4.19 MHz
μPD75CG19E	64-pin ceramic piggyback QUIP	4.19 MHz
μPD7519HG-12	64-pin plastic miniflat	6.55 MHz
μPD7519HG-36	64-pin plastic QUIP	6.55 MHz
μPD7519HCW	64-pin plastic shrink DIP	6.55 MHz
μPD75CG19HE	64-pin ceramic piggyback QUIP	6.55 MHz

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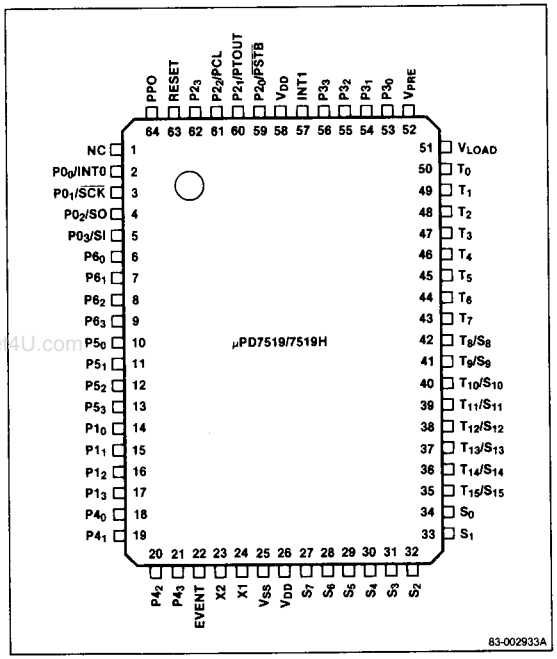
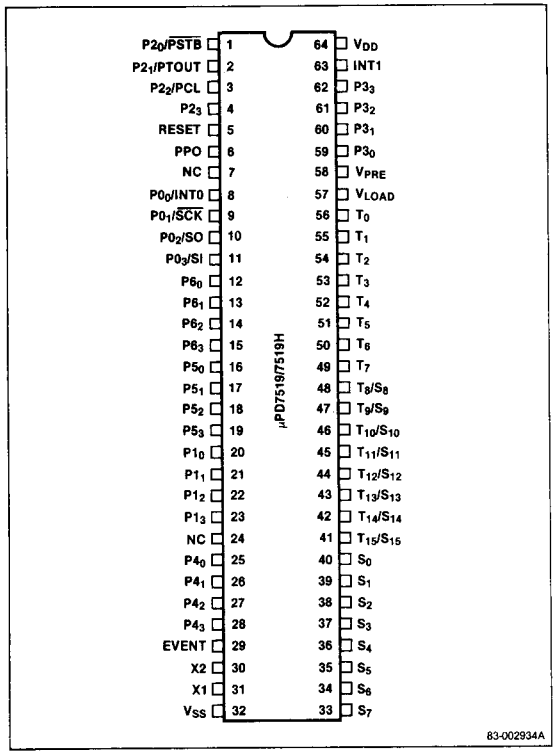
Pin Configurations

64-Pin Plastic Miniflat

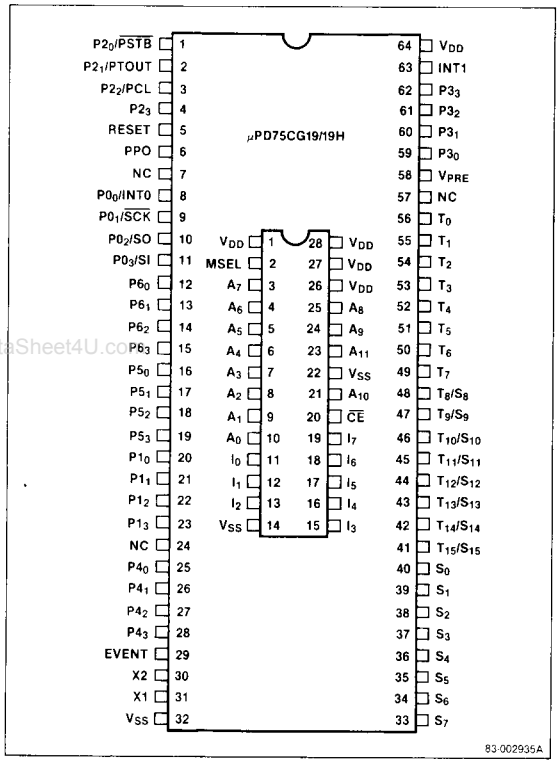


64-Pin Plastic QUIP and Shrink DIP



Pin Configurations (cont)

64-Pin Ceramic Piggyback QUIP



Pin Identification

Flatpack, Shrink DIP, and QUIP Packages

Flat	QUIP(1)	Name	Function
1	7, 24	NC	No connection
2	8	$P0_0$/INT0	Port 0 or external interrupt INT0 and the serial I/O interface
3	9	$P0_1$/$\overline{SCK}$	
4	10	$P0_2$/SO	
5	11	$P0_3$/SI	
6-9	12-15	$P6_0$-$P6_3$	Port 6
10-13	16-19	$P5_0$-$P5_3$	Port 5
14-17	20-23	$P1_0$-$P1_3$	Port 1
18-21	25-28	$P4_0$-$P4_3$	Port 4
22	29	EVENT	Timer/event counter input
23-24	30-31	X2, X1	Crystal clock input
25	32	V_{SS}	Ground
26, 58	64	V_{DD}	Power supply positive
27-34	33-40	S_0-S_7	Segment outputs
35-42	41-48	T_8/S_8-T_{15}/S_{15}	Timing/segment outputs
43-50	49-56	T_0-T_7	Timing outputs
51	57	V_{LOAD}	High voltage option resistor supply negative. This pin is not used (NC) in the μPD75CG19/75CG19H.
52	58	V_{PRE}	High voltage predriver supply negative
53-56	59-62	$P3_0$-$P3_3$	Port 3
57	63	INT1	External interrupt
59	1	$P2_0$/$\overline{PSTB}$	Port 2, or port 1 STB signal, timer F/F output, internal CL output, and general purpose output
60	2	$P2_1$/PTOUT	
61	3	$P2_2$/PCL	
62	4	$P2_3$	
63	5	RESET	RESET input
64	6	PPO	PPG output

Note:

(1) This QUIP pin identification is also true for the shrink DIP and piggyback packages.

Pin Identification (cont)

EPROM Socket on Piggyback QUIP

No.	Symbol	Function
1	V_{DD}	Unused
2	MSEL	Unused
3-10, 21, 23-25	A_0-A_{11}	Program counter output
11-13, 15-19	I_0-I_7	Data input from the 2732
14	V_{SS}	Same as bottom pin 32; connected to 2732 GND pin
20	$\overline{CE}$	Chip enable output
22	V_{SS}	Same as bottom pin 32; supplies $\overline{OE}$ signal to the 2732
26	V_{DD}	Same as bottom pin 64; supplies V_{CC} to the 2732
27, 28	V_{DD}	Unused

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI (Port 0)

This port can be configured as the 4-bit, parallel input port 0, or as the 8-bit serial I/O interface under control of the serial mode select register. The serial interface consists of the serial input (SI), serial output (SO), and serial clock ($\overline{SCK}$) used for synchronizing data transfer. Line $P0_0$ is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

$P1_0$-$P1_3$ (Port 1)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 1 mode select register.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$/PCL, $P2_3$ (Port 2)

$P2_0$-$P2_3$ are the 4-bit latched output port 2. $\overline{PSTB}$ is the port 1 output strobe pulse. PTOUT is the timer-out F/F signal. PCL is the internal system clock output. $P2_3$ is a general purpose output.

$P3_0$-$P3_3$ (Port 3)

4-bit, latched three-state output port 3.

$P4_0$-$P4_3$ (Port 4)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 5.

$P5_0$-$P5_3$ (Port 5)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 4.

$P6_0$-$P6_3$ (Port 6)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 6 mode select register.

EVENT

1-bit external event input for the timer/event counter.

S_0-S_7, T_8/S_8-T_{15}/S_{15}, T_0-T_7

High voltage outputs. S_0-S_7 are segment driver outputs, and T_0-T_7 are digit driver outputs. T_8/S_8-T_{15}/S_{15} can be configured as either segment or digit driver outputs under control of the display mode select register.

INT1

External, rising edge triggered interrupt.

PPO

1-bit programmable pulse generator output. PPO can operate as the pulse width modulation output, the signal generator port, or as a 1-bit output port, as dictated by the PPG mode select register.

RESET

RESET input. R/C circuit or pulse initializes μPD7519/7519H and also releases stop or halt mode.

X2, X1

Crystal clock connection. A crystal oscillator circuit is connected to X1 and X2 for system clock operation. Or, an external clock may be connected to X1 and an inverted clock to X2.

V_{PRE}

High voltage predriver supply. Apply single voltage from V_{DD}-12 V to V_{DD} for proper display operation.

V_{LOAD}

High voltage option resistor supply negative. Apply single voltage from V_{DD}-40 V to V_{DD} for proper display operation. This pin is not used (NC) in the μPD75CG19/75CG19H.

V_{DD}

Power supply positive. Apply single voltage ranging from 2.5 V to 6.0 V for proper operation.

V_{SS}

Ground.

Pin Functions, EPROM Socket

A_0-A_{11} (Address)

Output the 12 bits of the program counter (PC_0-PC_{11}), which are the address signals of EPROM 2732.

I_0-I_7 (Data Input)

Input data from the 2732.

$\overline{CE}$ (Chip Enable)

Outputs the chip enable signal to the 2732.

V_{DD} (Pin 1)

Electrically equivalent to V_{DD} of the bottom pins. Provided for future devices. Use in the open condition.

V_{DD} (Pin 26)

Electrically equivalent to V_{DD} of the bottom pins. Supplies V_{CC} to the 2732.

V_{DD} (Pins 27, 28)

Electrically equivalent to V_{DD} of the bottom pins. Do not use these pins.

V_{SS} (Pin 22)

Electrically equivalent to V_{SS} of the bottom pins. Supplies $\overline{OE}$ signal to the 2732.

V_{SS} (Pin 14)

Electrically equivalent to V_{SS} of the bottom pins. Connected to 2732 GND pin.

MSEL

Provided for future devices. Use in the open condition.

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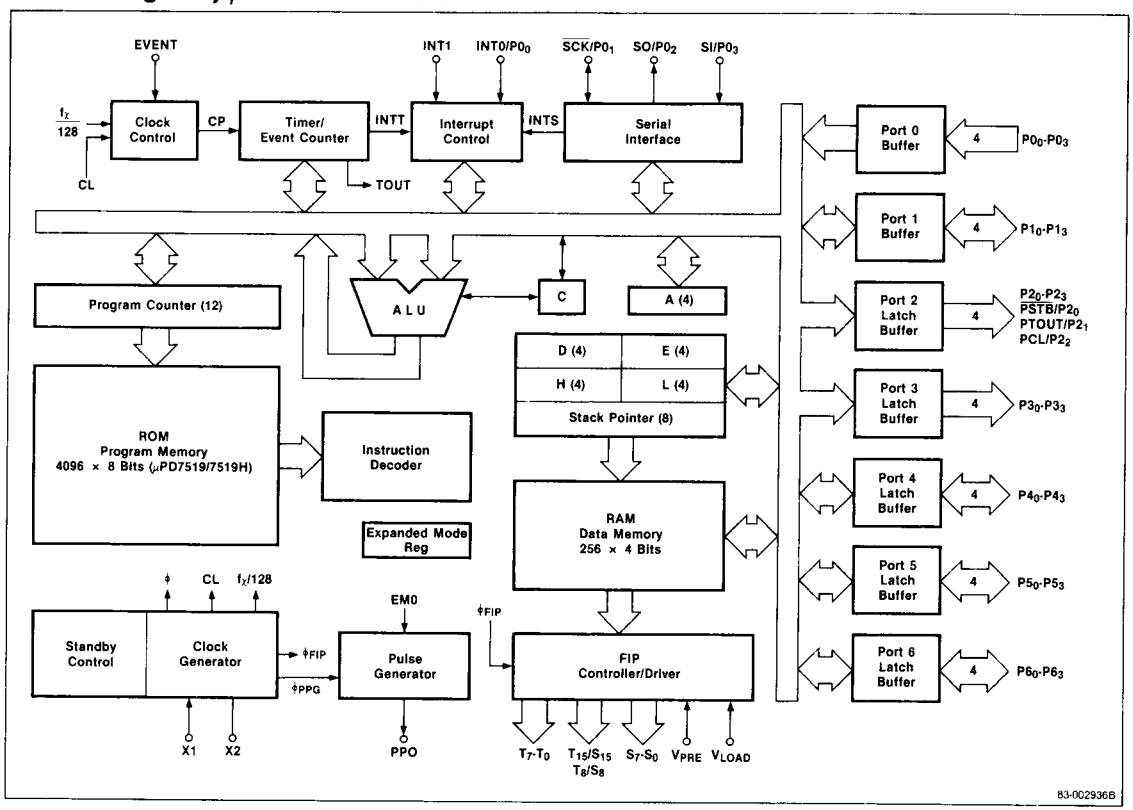
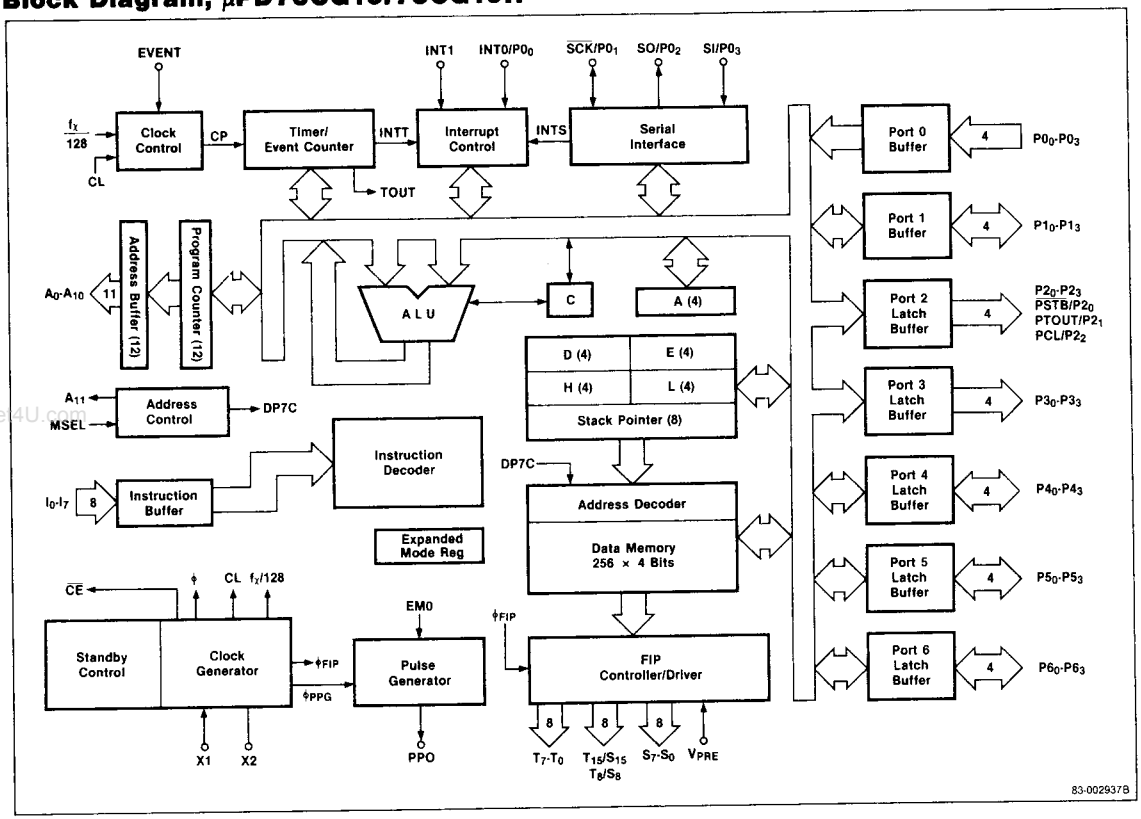
Block Diagram, μPD7519/7519H



Block Diagram, μPD75CG19/75CG19H



Functional Description

Program Memory (ROM), 4096 Words × 8 Bits

This mask programmable memory is addressed by the program counter (PC), and is used to store programs and table data. See figure 1.

General Purpose Registers

Four 4-bit general purpose registers (D, E, H, L) may be paired as follows for 8-bit operations: DE, HL, and DL. These 8-bit register pairs are commonly used as pointers to memory locations. When using the HL register pair as a data pointer, auto-increment and -decrement of the L register may be specified.

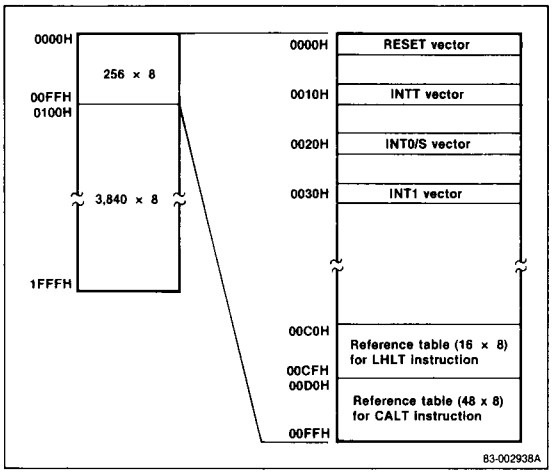
Data Memory (RAM), 256 Words × 4 Bits

This static RAM is used to store display and operation data. It may also function with the accumulator (A) for 8-bit data processing.

There are three types of data memory addressing:

- Direct. Address designation is made on the second byte of the instruction.
- Register indirect. Address designation is made by the contents of a register pair designated by the instruction.
- Stack. Indirect address designation is made by the contents of the stack pointer (SP).

Figure 1. Program Memory Map



Data memory addresses are from 00H to 0FFH. The first 64 locations are pre-assigned as display data for the FIP display (00H to 03BH) and the programmable pulse generator (PPG) modulo section (03CH to 03FH). When display data is written in 00H-03BH, the FIP controller/driver automatically reads it and generates drive signals for the FIP. See figure 2.

Addresses 00H-03FH cannot be accessed by stack operations. RAM locations 40H-0FFH can be used as a stack area addressed by the SP. This data memory area is used when executing call or return instructions (CALL, CALT, RT, RTS, RTSPW), push/pop instructions (PSHDE, PSHHL, POPDE, POPHL), and when answering an interrupt.

When executing a call instruction or interrupt occurrence with interrupts enabled, the contents of the PC and program status word (PSW) are stored in the stack area. A push instruction stores the contents of DE or HL in the stack area. See figure 3.

Figure 2. Data Memory Map

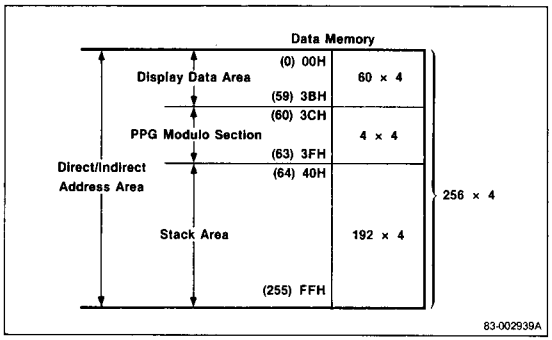
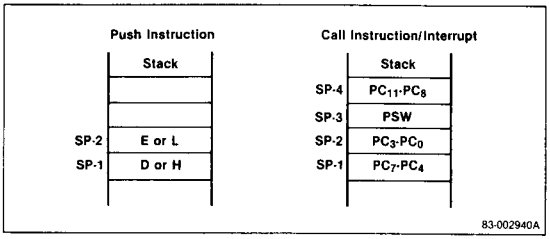


Figure 3. Push, Call, Interrupt



Clock Generator

The system clock generator consists of a crystal oscillator, a frequency divider, and a standby (stop/halt) mode control circuit, as shown in figure 4. When an external crystal is connected to X1 and X2, the crystal oscillator generates the f_{XX}. (The notation 'f_{XX}' is used when referring to crystal oscillation; 'f_X' is used when an external clock is input.) It is also possible to obtain a clock by inputting an external clock into X1 and an inverted clock to X2.

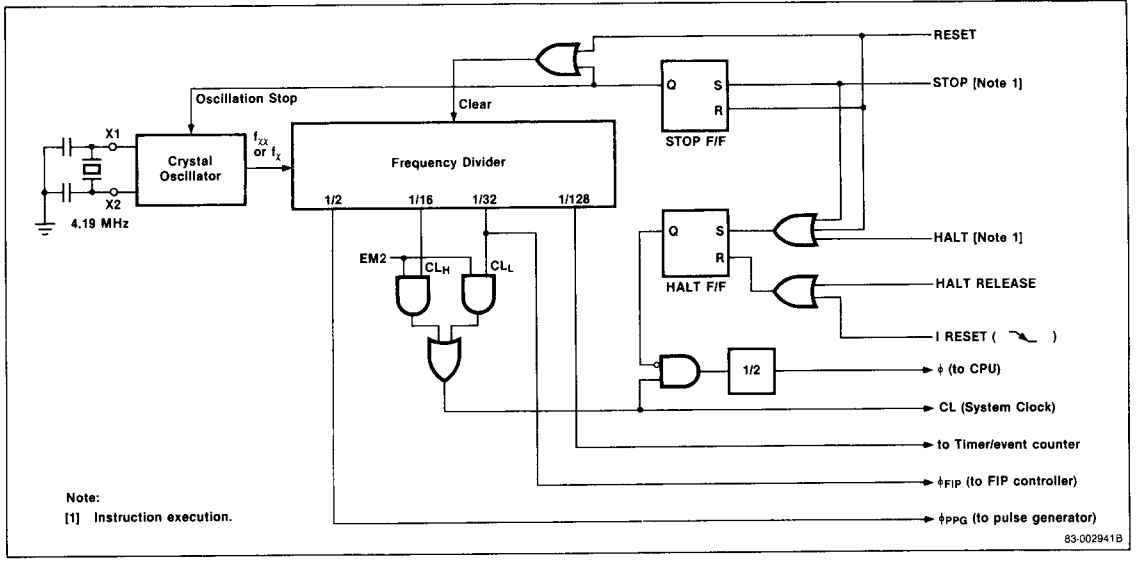
The frequency divider divides the output of the crystal oscillator into four frequencies, as follows:

- 1/2 (pulse generator clock, PPG)
- 1/8 (system clock, CLH) μPD7519H only
- 1/16 (system clock, CLH) μPD7519 only
- 1/32 (system clock, CLL; and FIP controller clock, FIP)
- 1/128 (timer/event counter clock)

The system clock (CL) may be 1/8 (μPD7519H), 1/16 (μPD7519) or 1/32 frequency-divided, depending on the state of expansion mode register bit 2 (EM_2). EM_2 = 1 selects 1/8 (μPD7519H) and 1/16 (μPD7519), and EM_2 = 0 selects 1/32. CL is supplied to all circuits except the FIP controller and PPG, which use the f_{XX} × 1/32 and f_{XX} × 1/2, respectively. CL is 1/2 frequency divided to supply the CPU (ϕ) clock. CL is an input to the clock control circuitry used to generate the clock pulse (CP) used by the timer/event counter.

The standby mode control circuit consists mainly of the stop and halt flip-flops. The stop flip-flop, when set, stops the crystal oscillator. There is no input to the frequency divider, so no clocks are output to the μPD7519/7519H circuitry. The STOP instruction sets the stop flip-flop, and RESET clears it. The halt flip-flop, when set, inhibits the input to the 1/2 frequency divider that generates ϕ, thereby stopping ϕ, A HALT or STOP sets this flip-flop; it is reset by the RELEASE signal (generated when an interrupt flag is set) or at the falling edge of the internal reset (IRESET) signal. (IRESET is released after a waiting time following the release of the external RESET input.)

Figure 4. Clock Generator Circuit



Clock Control Circuit

This circuit consists of a 4-bit clock mode register (CM_0-CM_3), three prescalers, and a multiplexer, as shown in figure 5. The circuit generates the clock pulse (CP) input to the timer/event counter from the following inputs:

- System clock (CL)
- 1/128 divided clock from the crystal oscillator ($f_{XX}/128$)
- External EVENT pulse

Bits CM_0-CM_2 determine the clock input selection and divide ratio. CM_3 gates the output of a timer out signal from the PTOUT ($P2_1$) pin. When CM_3 = 1, output from the timer out flip-flop (TOUT) is output to $P2_1$. Executing an OP or OPL instruction loads the clock mode register.

The format of the clock mode register is shown in figure 6.

Figure 6. Clock Mode Register

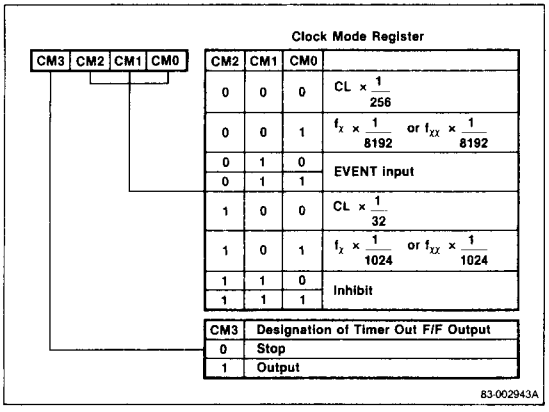
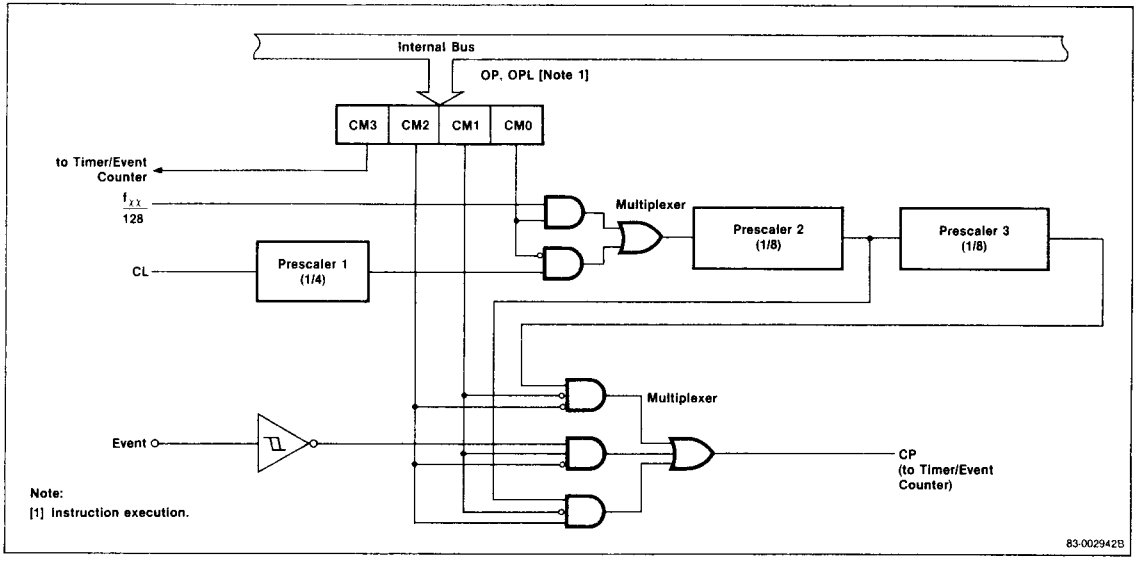


Figure 5. Clock Control Circuit



Timer/Event Counter

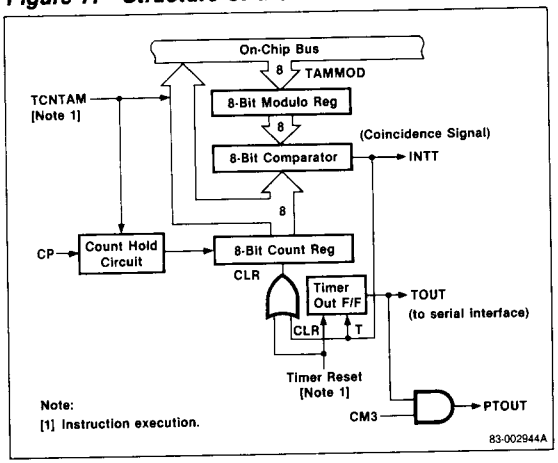
This counter consists of an 8-bit count register, an 8-bit modulo register, an 8-bit comparator, and a timer-out flip-flop, as shown in figure 7.

The 8-bit count increments at every rising edge of the clock pulse (CP). Executing the TIMER instruction, a RESET input, or a coincidence signal from the comparator clears it to 0.

The modulo register determines the INTT signal interval. The contents of this register are set via the TAMMOD instruction. RESET sets the contents to OFFH.

The timer-out flip-flop inverts with every INTT signal output from the comparator. Its output, TOUT, can be sent to the PTOUT pin when bit 3 (CM_3) of the clock mode register is set. TOUT may also be used as a serial clock source to the serial interface.

Figure 7. Structure of the Timer/Event Counter



Serial Interface

The serial interface, used for serial data I/O, consists of an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter, as shown in figure 8. Figure 9 shows the serial shift timing.

The serial clock ($\overline{SCK}$) controls the serial data communication rate. An 8-bit byte clocks into the serial input (SI) port or out of the serial output (SO) port starting with the MSB. Data transmission occurs synchronously with the falling edge of $\overline{SCK}$. Data reception occurs synchronously with the rising edge of $\overline{SCK}$.

The 3-bit counter counts the number of serial clock pulses. When a byte of serial data is transferred, an internal interrupt signal (INTS) is generated. Selecting INTS (setting SM_3 of the shift mode register to 0) sets the interrupt request flag, INT0/S RQF.

The end of transfer of each byte can also be verified by testing INTS RQF with the SKI instruction instead of interrupt processing.

Figure 8. Serial Interface Block Diagram

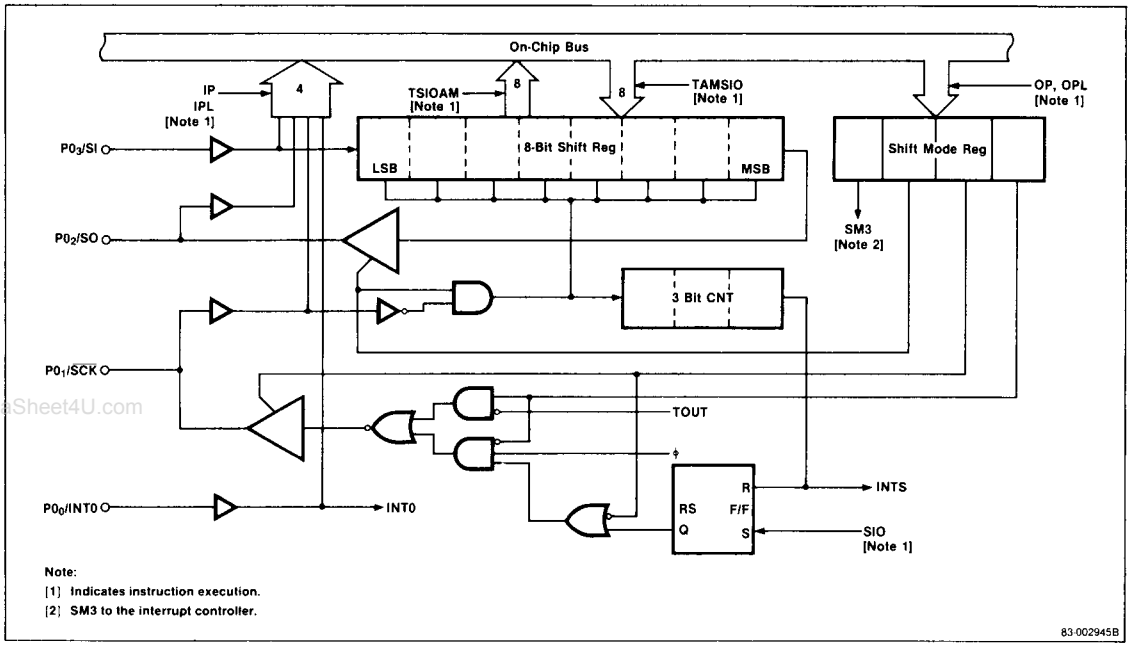
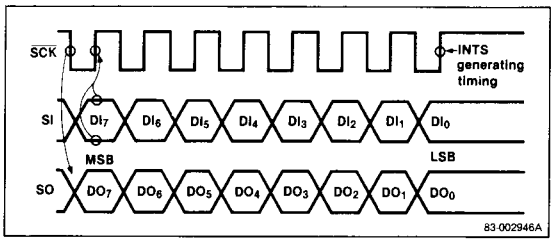


Figure 9. Serial Shift Timing



CPU Clock (ϕ)

When the SIO instruction executes, eight CPU clock pulses (ϕ) are supplied to the serial interface for the serial clock and output from $\overline{SCK}$. After the eighth clock, $\overline{SCK}$ is fixed high level, automatically stopping serial data I/O after one byte has transferred.

$\overline{SCK}$ does not have to be software controlled. Its transfer rate is determined by the frequency of ϕ. See table 1.

Interrupt Function

There are two external and two internal interrupts, with the specifications listed in table 2. The external interrupt INT0 uses the $P0_0$ port pin as the interrupt signal input, and has the same interrupt process as the internal serial interrupt INTS. Selection of the interrupt is programmable and depends on the application.

Table 1. SCK Frequencies

f_{XX}	Low Speed Mode	High Speed Mode
6.55 MHz	102.4 kHz	409.6 kHz (μPD7519H)
4.19 MHz	65.5 kHz	262 kHz (μPD7519H)
4.19 MHz	65.6 kHz	131 kHz (μPD7519)

Table 2. Interrupt Specifications

Source	Int/Ext	Priority	Vector Address
INTT (coincidence signal from timer/event counter)	int	1	10H(16)
INT0 (interrupt signal from $P0_0$ terminal)	ext	2	20H(32)
INTS (end of transfer signal from serial interface)	int	2	20H(32)
INT1 (interrupt signal from INT1 terminal)	ext	3	30H(48)

Interrupt Sequence

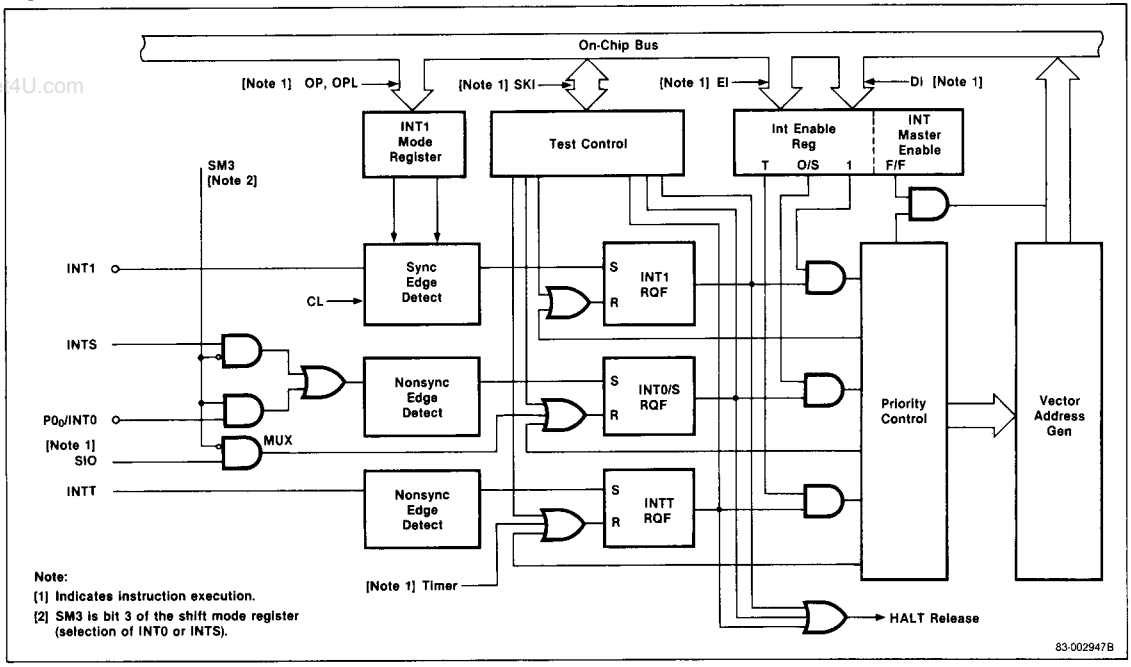
When an interrupt goes active, the following occur:

- A corresponding interrupt request flag is set.
- The interrupt master enable flip-flop is reset.
- The contents of the PC and PSW are saved in the stack.
- An interrupt start address is generated and jumped to.
- The interrupt request flag set by the interrupt is reset.

Two machine cycles are required for interrupt execution, one for saving the return address and one for jumping to the interrupt start address. If several interrupts occur simultaneously, all respective request flags are set, and the interrupt with the highest priority is processed. The remaining interrupts are pending until serviced by reenabling the master interrupt flip-flop or until their interrupt request flags are reset by executing a SKI instruction.

Figure 10 is a block diagram of the interrupt control circuit.

Figure 10. Interrupt Control Circuit Block Diagram



FIP Controller/Driver

The FIP controller/driver consists of 60 4-bit nibbles of display memory (000-03BH of data RAM), a 4-bit display mode register (DM_3-DM_0), a 4-bit timing mode register (TM_3-TM_0), a 4-bit blanking mode register (BM_3-BM_0), an output selector, and a high voltage output driver. See figure 11.

The FIP controller/driver has 24 outputs for directly driving a high voltage vacuum fluorescent display:

- 8 segment signal outputs (S_0-S_7)
- 8 timing signal (grid) outputs (T_0-T_7)
- 8 timing or segment outputs (T_8/S_8-T_{15}/S_{15}

The content of the display mode register determines which of five display modes is available to the user. The modes are as follows:

- Static mode
  - — 24 static output
- Dynamic mode
  - — 8 segment mode
  - — 12 segment mode I
  - — 12 segment mode II
  - — 16 segment mode

The content of the timing mode register determines the number of display digits (1-16), and controls the number of timing signals (T_0-T_{15}) output. Timing signals drive the grids of vacuum fluorescent display tubes. The voltage on the grid will determine the brightness of a digit (made up of one or more segments) or if the digit will be turned on or off.

The width of the timing signal pulse can be adjusted at eight independent steps by the value loaded into the blanking mode register. This function is useful for dimming control and for preventing display cross-talk of adjacent digits.

The active level of the timing signal can be designated high or low by bit DM_3.

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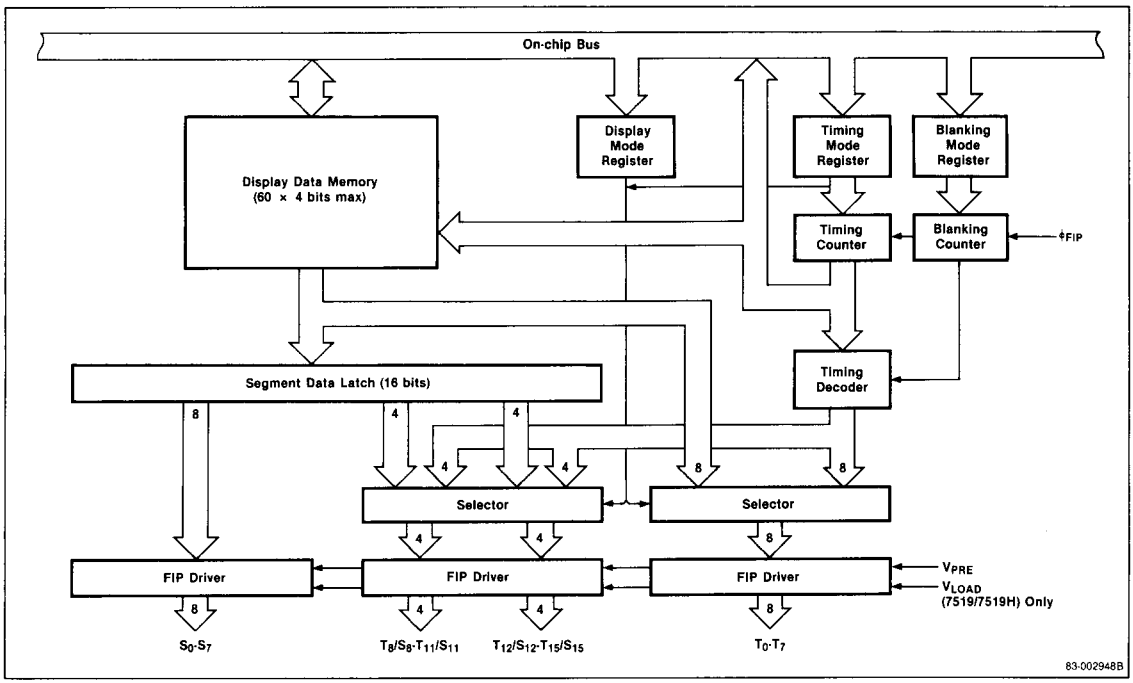
Figure 11. FIP Controller/Driver Block Diagram



Display Mode Register (DM)

This 4-bit write-only register (DM_3-DM_0) determines the display mode (dynamic, static, and off) of the FIP controller/driver. It also determines the active level of the display timing signals. This is shown in figure 12.

The DM register has an output address of 0BH and is accessed by the output instructions OP and OPL when bit EM_3 of the expansion mode register is set. The DM register is cleared by a RESET.

Figure 13 shows a display example in 12 segment mode I.

Figure 12. Display Mode Register Format

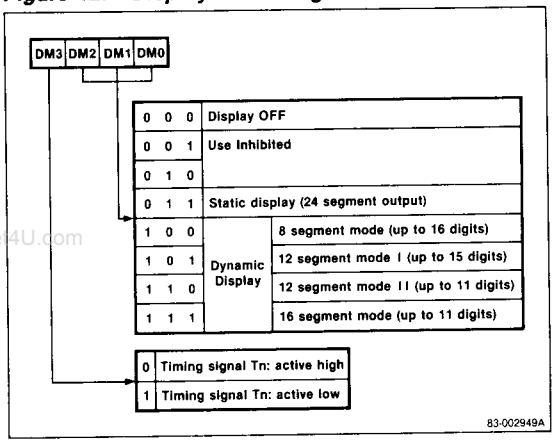
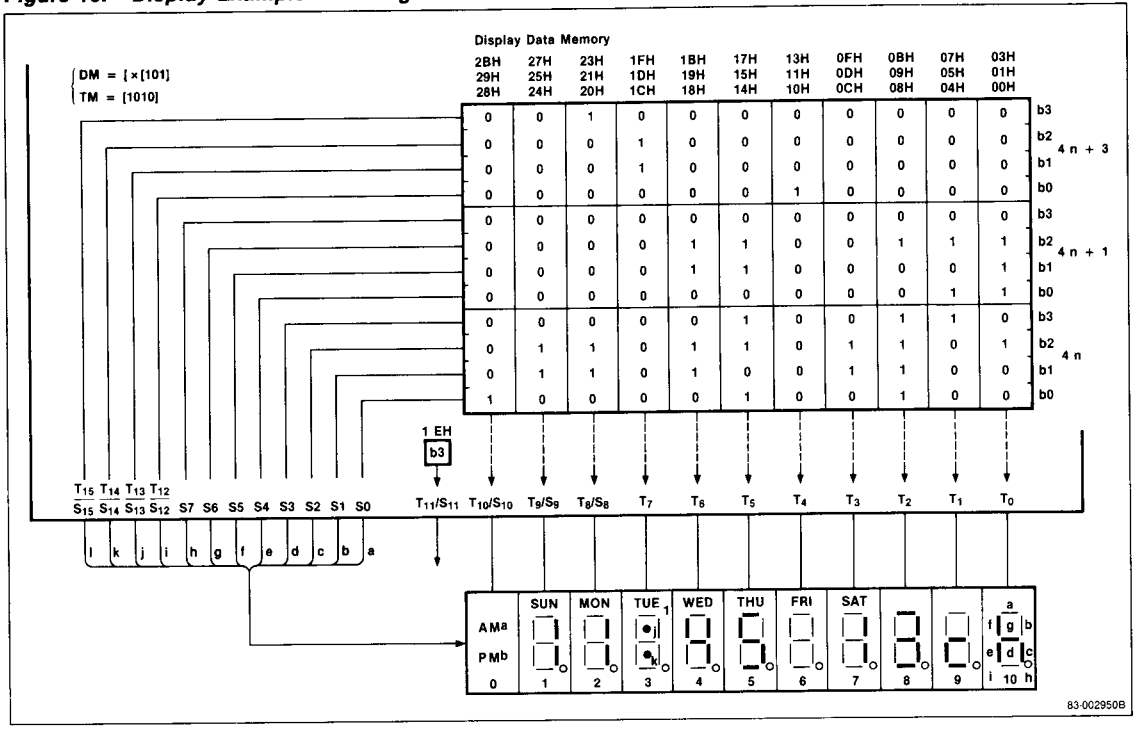


Figure 13. Display Example in 12 Segment Mode I



Standby Function

Two standby modes, stop and halt, hold device power consumption to a minimum. Stop mode is entered via the STOP instruction, and halt mode is entered via the HALT instruction. In stop mode, all clocks are stopped. In halt mode, only the CPU clock (ϕ) is stopped.

Stop mode can only be released by a RESET. Halt mode may be released either by a RESET or by the setting of an interrupt request flag.

Stop Mode

In stop mode, the contents of memory are retained, and all other functions are stopped. RESET releases stop mode.

In stop mode, the X1 input is internally shorted to V_{SS} in order to hold the crystal oscillator leakage to a minimum. A system using stop mode cannot use an external clock.

Halt Mode

When no interrupt flags are set, the HALT instruction causes the device to enter halt mode. In this mode, only ϕ stops; all other clocks continue to operate. The following functions continue to operate:

- Clock oscillation
- Frequency division and output of clocks other than ϕ
- Event input
- Timer/event counter
- Serial interface (except when ϕ is used as SCK)
- FIP controller/driver
- PPG
- Interrupts (INT0, INTS, INTT, INT1)
- RESET

Since a set interrupt flag releases the device from halt mode, this mode cannot be entered if an interrupt request flag is set. It is therefore necessary to reset the request flag(s) either by answering the interrupt(s) (setting the interrupt master enable F/F and process interrupt) or by executing the SKI instruction.

In halt mode, CPU power consumption is eliminated. To hold power consumption to a minimum, all unnecessary circuits should be inactive and the steps below should be taken:

- Set the system clock (CL) to low speed
- Set the FIP controller/driver to the off mode
- Set the PPG for static operation
- Stop $\overline{SCK}$ input

Low Supply Voltage Data Retention (μPD7519/7519H only)

Data retention is possible with V_{DD} as low as 2 V. V_{DD} should be lowered after the device is put in stop mode, and while RESET is inactive. Stop mode cannot be released in low voltage data retention mode; V_{DD} should first be raised to normal operation.

Release of Stop Mode

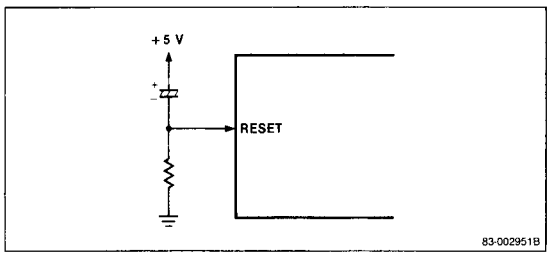
RESET releases stop mode. On RESET's rising edge, the device mode changes to halt mode, starting clock oscillation. At the falling edge of RESET, a waiting time (about 62.5 ms/4.19 MHz, 40 ms/6.55 MHz) elapses, allowing for stabilization of crystal operation, following which halt mode is released. After normal RESET operation, the CPU begins program execution from address 0000H.

In the release operation, the contents of data memory are retained while the contents of other registers become undefined.

Power-on Reset Circuit

An example of the simplest power-on reset circuit using a resistor and capacitor is show in figure 14.

Figure 14. Power-on Reset Circuit



Application

The μPD7519/7519H has a variety of flexible powerful functions and is best suited for the following applications:

- Video tape recorders
- Plain paper copiers
- Electronic cash registers
- Telephone sets
- Electronic scales
- Automobiles

Figures 15-18 show how to apply the device to a digital tuning system, a telephone, an ECR, and automotive equipment.

Figure 15. Digital Tuning System Application

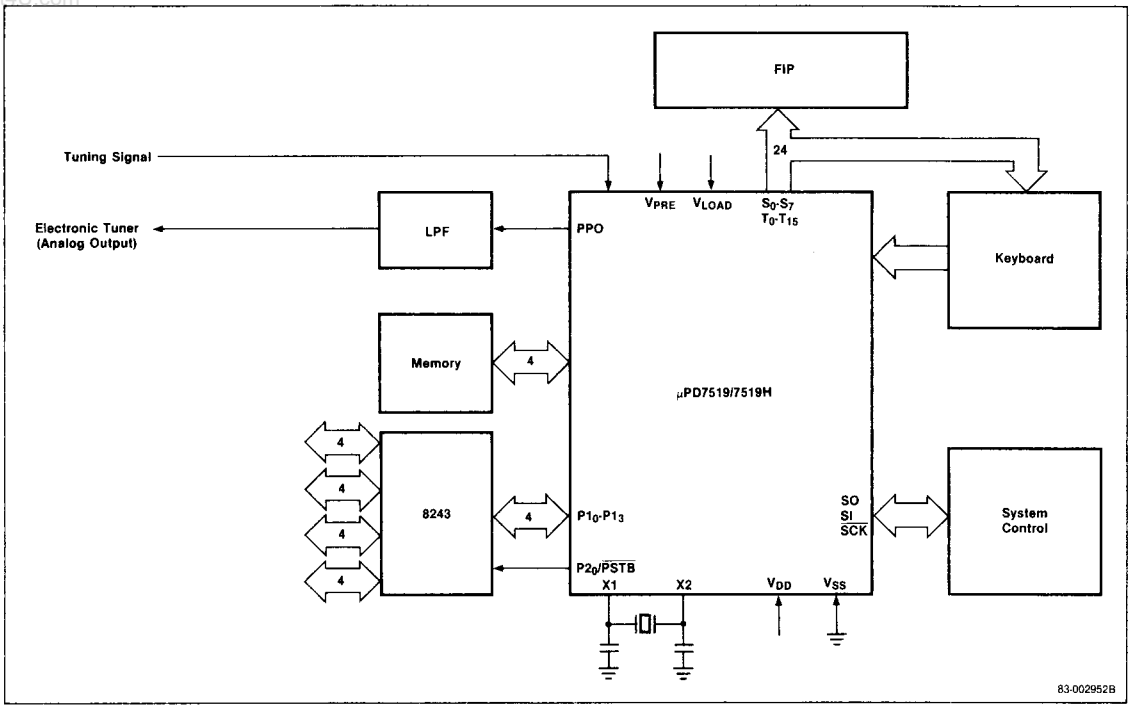


Figure 16. Telephone Application

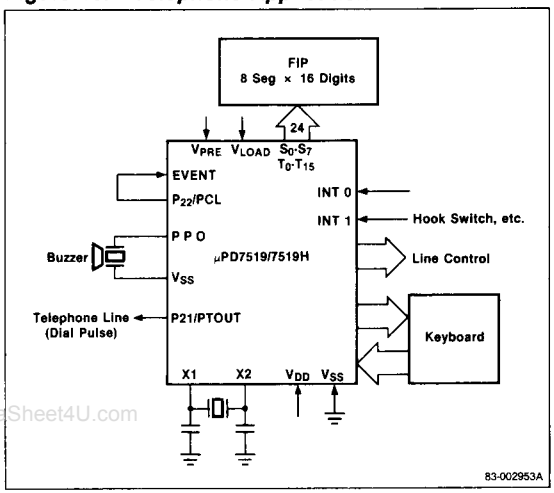


Figure 17. ECR Application

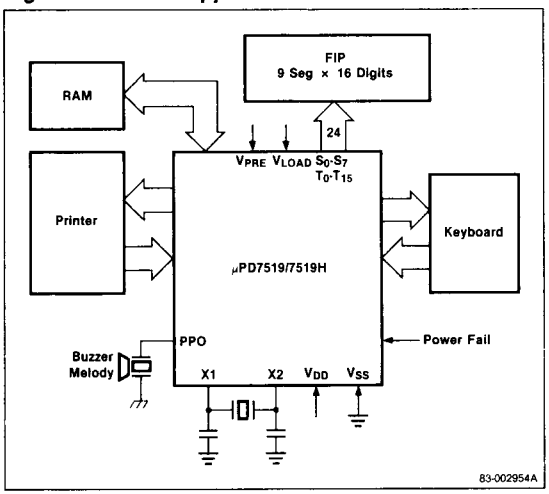
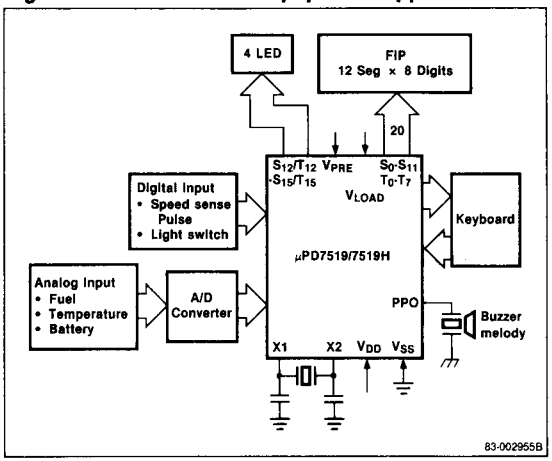


Figure 18. Automotive Equipment Application



3

Absolute Maximum Ratings

T_A = 25°C

Supply voltages, V_{DD}	−0.3 V to +7 V
V_{LOAD} (μPD7519/7519H)	(V_{DD} − 40) to (V_{DD} + 0.3)
V_{PRE}	(V_{DD} − 12) to (V_{DD} + 0.3)
Input voltage, V_I	−0.3 V to (V_{DD} + 0.3)
Output voltage, Display outputs, V_O	(V_{DD} − 40) to (V_{DD} + 0.3)
Other outputs, V_{OD}	−0.3 V to (V_{DD} + 0.3)
Output current high, I_{OH}	
Per pin, other than display outputs	−15 mA
Per pin, S_0-S_7	−15 mA
Per pin, T_0-T_7, T_8/S_8-T_{15}/S_{15}	−30 mA
Total, display outputs, μPD7519/7519H	−120 mA
Display outputs, μPD75CG19/75CG19H	−90 mA
Total, other than display outputs	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, all output ports	60 mA
Total power consumption (1), PT Plastic flat package (μPD7519/7519H)	400 mW
Plastic QUIP, (μPD7519/7519H)	600 mW
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

(1) Calculation of PT: There are three kinds of power consumption, the total of which should be less than the total power consumption (PT) in this specification. Use of less than 80% of PT is recommended. The three different power consumptions are as follows:

1. CPU power consumption. V_{DD}(max) × I_{DD1}(max)
2. Power consumption of output pins. This includes both normal output and display output. Calculate the total consumption of each output pin to which the maximum current flows.
3. Power consumption of on-chip pull-down resistors (mask option).

Example

Configuration:

9 segments × 11 digits, 4 LED outputs
V_{DD} = 5 V ± 10%, 4.19 MHz oscillation
Segment pin = 5 mA (max)
Timing pin = 15 mA (max)
LED output pin = 10 mA (max)
Vacuum fluorescent display (V_{LOAD}) = −30 V

Consumption:

(1) CPU
5.5 V × 2.0 mA = 11 mW
(2) Output pins
Segment pins: (5/7 × 2 V) × 5 mA × 9 = 64 mW
Timing pins: 2 V × 15 mA = 30 mW
LED output pins: (10/15 × 2 V) × 10 mA × 4 = 53 mW
(3) Pull-down resistors
$(30 + 5.5\ V)^2/80\ k\Omega \times 10 = 158$ mW

Therefore, PT = (1) + (2) + (3) = 316 mW

Capacitance

T_A = 25°C; V_{DD} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	f_C = 1 MHz Unmeasured pins are connected to 0 V
Output capacitance, Display outputs	C_O			35	pF	
Other outputs				15	pf	
I/O capacitance	C_{IO}			15	pF	

Operating Supply Voltages

T_A = −10°C to +70°C

Parameter	Limits Min	Max	Unit	Test Conditions	
CPU (1) μPD7519/75CG19	4.0	6.0	V	f_x = 0.4 MHz to 4.2 MHz f_{xx} = 3.5 MHz to 4.2 MHz	High speed mode, EM2=1
	2.5	6.0	V		Low speed mode, EM2=0
CPU (1) μPD7519H/75CG19H	4.5	6.0	V	f_x, f_{xx} = 4.2 MHz to 6.6 MHz	High speed mode, EM2=1
	4.0	6.0	V	f_x = 0.1 MHz to 4.2 MHz f_{xx} = 3.5 MHz to 4.2 MHz	
	4.5	6.0	V	f_x, f_{xx} = 4.2 MHz to 6.6 MHz	Low speed mode, EM2=0
	2.5	6.0	V	f_x = 0.1 MHz to 4.2 MHz f_{xx} = 3.5 MHz to 4.2 MHz	
Crystal oscillation circuit (2) μPD7519/75CG19	2.7	6.0	V	C_1 = 10 pF $C_2 \leq$ 10 pF	Crystal Oscillator
	2.85	6.0	V	C_1 = 10 pF $C_2 \leq$ 22 pF	
	2.5	6.0	V		External clock
Crystal oscillation circuit (2) μPD7519H/75CG19H	4.5	6.0	V	f_{xx} = 4.2 MHz to 6.6 MHz C_1 = 10 pF, $C_2 \leq$ 10 pF	Crystal Oscillator
	2.7	6.0	V	C_1 = 10 pF, $C_2 \leq$ 10 pF f_{xx} = 3.5 MHz to 4.2 MHz	
	2.85	6.0	V	C_1 = 10 pF, $C_2 \leq$ 22 pF f_{xx} = 3.5 MHz to 4.2 MHz	
	2.6	6.0	V		External clock
Display controller	4.0	6.0	V		
PPG	4.0	6.0	V		
Port 1	2.5	6.0	V	Port output mode	
	4.0	6.0	V	I/O expander mode	

Note:

(1) Except the crystal oscillation circuit, display controller, PPG, and port 1.

(2) The circuits in figures 19 and 20 are recommended.

3

DC Characteristics

T_A = −10°C to +70°C
μPD7519/7519H: V_{DD} = 2.5 V to 6 V; μPD75CG19/75CG19H: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than X1, X2
	V_{IH2}	V_{DD} −0.4		V_{DD}	V	X1, X2 (1)
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Other than X1, X2
	V_{IL2}	0		0.4	V	X1, X2 (1)
Output voltage high	V_{OH}	V_{DD} −1.0			V	V_{DD} = 5 V ± 10%, I_{OH} = −1 mA
		V_{DD} −0.5			V	μPD7519/19H only, I_{OH} = −100 μA
Output voltage low	V_{OL}			0.4	V	V_{DD} = 5 V ± 10%, I_{OL} = 1.6 mA;
				0.5	V	μPD7519/19H only, I_{OL} = 400 μA
Input leakage current high	I_{LIH1}			3	μA	V_I = V_{DD}; other than X1, X2
	I_{LIH2}			20	μA	V_I = V_{DD}; X1, X2
Input leakage current low	I_{LIL1}			−3	μA	V_I = 0 V; other than X1, X2
	I_{LIL2}			−20	μA	V_I = 0 V; X1, X2
Input leakage current	I_{IL}			−200	μA	μPD75CG19H only V_I = 0 V, I_0 − I_7
Output leakage current high	I_{LOH}			3	μA	V_O = V_{DD}
Output leakage current low	I_{LOL1}			−3	μA	V_O = 0 V; other than display outputs
	I_{LOL2}			−10	μA	V_O = V_{LOAD} = V_{DD}−35 V; display outputs
Display output current	I_{OD}	−7			mA	S_0-S_7 V_{PRE} = V_{DD}−9 V ± 1 V(2)
		−4			mA	μPD75CG19/75CG19H V_{OD} = V_{DD}−2 V V_{DD} = 4 V to 6 V
		−15			mA	T_0-T_{15}
		−10			mA	μPD75CG19/75CG19H
		−3			mA	S_0-S_7 V_{PRE} = 0 V
		−2			mA	μPD75CG19/75CG19H V_{OD} = V_{DD} −2 V V_{DD} = 4 V to 6 V
		−7			mA	T_0-T_{15}
		−5			mA	μPD75CG19/75CG19H
On-chip pull-down resistance, μPD7519	R_L	80	140	220	kΩ	V_{OD} − V_{LOAD} = 35 V
On-chip pull-down resistance, μPD7519H	R_L	40	70	120	kΩ	V_{OD} − V_{LOAD} = 35 V

DC Characteristics (cont)

T_A = −10°C to +70°C
μPD7519/7519H: V_{DD} = 2.5 V to 6 V; μPD75CG19/75CG19H: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply current, μPD7519 (3)	I_{DD1}		600	2000	μA	High speed V_{DD} = 5 V ± 10% 4.19 MHz crystal C1 = C2 = 10 pF
			200	700	μA	Low speed V_{DD} = 3 V ± 10%
	I_{DD2}		260	800	μA	Low speed halt mode V_{DD} = 5 V ± 10%
			120	400	μA	Low speed halt mode V_{DD} = 3 V ± 10%
	I_{DD3}		0.1	10	μA	Stop mode
Supply current, μPD75CG19 (3)	I_{DD1}		700	2000	μA	High speed 4.19 MHz crystal C1 = C2 = 10 pF
	I_{DD2}		350	800	μA	Low speed halt mode V_{DD} = 5 V ± 10%
Supply current, μPD7519H (3)	I_{DD1}		2.0	6.0	mA	High speed 6.55 MHz crystal
	I_{DD2}		0.6	1.9	mA	Halt mode C1 = C2 = 10 pF V_{DD} = 5 V ± 10
	I_{DD1}		1.3	4.0	mA	High speed 4.19 MHz crystal V_{DD} = 5 V ± 10% C1 = C2 = 10 pF
			250	800	μA	Low speed V_{DD} = 3 V ± 10%
	I_{DD2}		450	1500	μA	Low speed halt mode V_{DD} = 5 V ± 10%
			150	400	μA	Low speed halt mode V_{DD} = 3 V ± 10%
	I_{DD3}		0.1	20	μA	V_{DD} = 5 V ± 10% Stop mode
			0.1	10	μA	V_{DD} = 3 V ± 10%
Supply current, μPD75CG19H (3)	I_{DD1}		1.2	3.6	mA	High speed V_{DD} = 5 V ± 10% 6.55 MHz crystal C1 = C2 = 10 pF
			1.0	3.0	mA	High speed halt mode V_{DD} = 4.75 to 5.5 V 4.19 MHz crystal C1 = C2 = 10 pF
	I_{DD2}		350	1000	μA	Low speed halt mode V_{DD} = 5 V ± 10% 4.19 MHz crystal C1 = C2 = 10 pF
	I_{DD3}			20	μA	V_{DD} = 5 V ± 10% Stop mode

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) The external circuit in figure 21 is recommended.

(3) The display controller and PPG are not operated.

Figure 19. Crystal

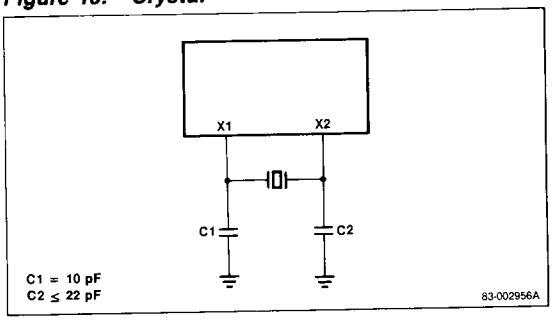


Figure 20. External Clock

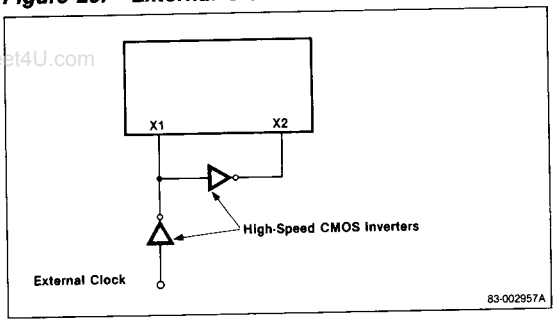
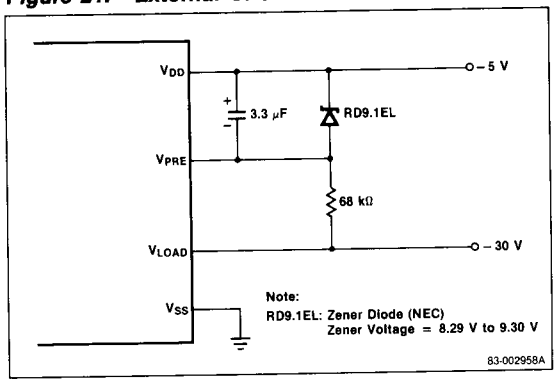


Figure 21. External Circuit



AC Characteristics

T_A = −10°C to +70°C

Clock Operation, μPD7519/75CG19

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency	f_{XX}	3.5	4.19	4.2	MHz	Crystal oscillation (1), (2)
System clock input frequency	f_X	0.1		5	MHz	External clock (1)
X1, X2 input pulse width high and low	t_{XH}	100			ns	External clock (1)
	t_{XL}	100			ns	
EVENT input frequency	f_E			410	kHz	V_{DD} = 4.0 V to 6.0 V
				80	kHz	μPD7519 only
EVENT input pulse width high, low	t_{EL}	1.2			μs	V_{DD} = 4.0 V to 6.0 V
	t_{EH}	6.25			μs	μPD7519 only

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) Refer to the Operating Supply Voltages tables.

Clock Operation, μPD7519H/75CG19H

μPD7519H: V_{DD} = 2.5 V to 6 V
μPD75CG19H: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency	f_{XX}	3.5	4.19	4.2	MHz	Crystal oscillation (1), (2)
		4.2	6.55	6.6	MHz	V_{DD} = 4.5 V to 6.0 V
System clock input frequency	f_X	0.1		4.2	MHz	External clock (1)
		4.2		6.6	MHz	V_{DD} = 4.5 V to 6.0 V
X1, X2 input pulse width high, low	t_{XH}	100			ns	External clock (1)
	t_{XL}	75			ns	V_{DD} = 4.5 V to 6.0 V
EVENT input frequency	f_E			410	kHz	V_{DD} = 4.0 V to 6.0 V
				80	kHz	μPD7519H only
EVENT Input pulse width high, low	t_{EL}	6.25			μs	V_{DD} = 4.0 V to 6.0 V μPD7519H only

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) Refer to the Operating Supply Voltages table.

AC Characteristics (cont)

T_A = −10°C to +70°C

Port 1 I/O Operation, μPD7519/75CG19

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%
0.1 MHz ≤ f_x, f_{xx} ≤ 4.2 MHz

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Port 1 output setup time (to $\overline{PSTB}$↑)	t_{PST}	400		ns	Port output mode
Port 1 output hold time (after $\overline{PSTB}$↑)	t_{STP}	100		ns	
$\overline{PSTB}$ pulse width low	t_{STL1}	600		ns	
Output data set-up time (to $\overline{PSTB}$↑)	t_{DST}	400		ns	I/O expander mode V_{DD} = 4 V to 6 V
Output data hold time (after $\overline{PSTB}$↑)	t_{STD}	100		ns	
Input data valid time (after $\overline{PSTB}$↓)	t_{STDV}		850	ns	
Input data floating time (after $\overline{PSTB}$↑)	t_{STDF}	0		ns	
Control set-up time (to $\overline{PSTB}$↓)	t_{CST}	400		ns	
Control hold time	t_{STC}				
Output command		100		ns	
Input command		0	80	ns	
$\overline{PSTB}$ pulse width low	t_{STL2}	1200		ns	

Port 1 I/O Operation, μPD7519H/75CG19H

μPD7519H: V_{DD} = 2.5 V to 6 V
μPD75CG19H: V_{DD} = 5 V ± 10%
0.1 MHz ≤ f_x, f_{xx} ≤ 4.2 MHz

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Port 1 output setup time (to $\overline{PSTB}$↑)	t_{PST}	250		ns	Port output mode
Port 1 output hold time (after $\overline{PSTB}$↑)	t_{STP}	100		ns	
$\overline{PSTB}$ pulse width low	t_{STL1}	450		ns	
Output data set-up time (to $\overline{PSTB}$↑)	t_{DST}	200		ns	I/O expander mode V_{DD} = 4 V to 6 V
Output data hold time (after $\overline{PSTB}$↑)	t_{STD}	100		ns	
Input data valid time (after $\overline{PSTB}$↓)	t_{STDV}		700	ns	
Input data floating time (after $\overline{PSTB}$↑)	t_{STDF}	0		ns	
Control set-up time (to $\overline{PSTB}$↓)	t_{CST}	100		ns	
Control hold time	t_{STC}				
Output command		100		ns	
Input command		0	80	ns	
$\overline{PSTB}$ pulse width low	t_{STL2}	750		ns	

AC Characteristics (cont)

T_A = −10°C to +70°C

Port 1 I/O Operation, μPD7519H/75CG19H

μPD7519H: V_{DD} = 4.5 V to 6 V
μPD75CG19H: V_{DD} = 4.75 V to 5.5 V
4.2 MHz ≤ f_x, f_{xx} ≤ 6.6 MHz, Low Speed Mode(1) (EM_2 = 0)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Port 1 output setup time (to $\overline{PSTB}$↑)	t_{PST}	400		ns	Port output mode
Port 1 output hold time (after $\overline{PSTB}$↑)	t_{STP}	100		ns	
$\overline{PSTB}$ pulse width low	t_{STL1}	600		ns	
Output data set-up time (to $\overline{PSTB}$↑)	t_{DST}	400		ns	I/O expander mode V_{DD} = 4 V to 6 V
Output data hold time (after $\overline{PSTB}$↑)	t_{STD}	100		ns	
Input data valid time (after $\overline{PSTB}$↓)	t_{STDV}		850	ns	
Input data floating time (after $\overline{PSTB}$↑)	t_{STDF}	0		ns	
Control set-up time (to $\overline{PSTB}$↓)	t_{CST}	400		ns	
Control hold time	t_{STC}				
Output command		100		ns	
Input command		0	80	ns	
$\overline{PSTB}$ pulse width low	t_{STL2}	1200		ns	

Note:

(1) The μPD82C43/8243H, etc, cannot interface with the μPD7519H in high speed mode (EM_2 = 1).

3

AC Characteristics (cont)

T_A = −10°C to +70°C

Serial Interface Operation, μPD7519/75CG19

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{KCY}	3.0		μs	Input V_{DD} = 4 V to 6 V
		12.5		μs	μPD7519 only
		4.9		μs	Output V_{DD} = 4 V to 6 V
		10		μs	μPD7519 only
$\overline{SCK}$ pulse width high, low	t_{KH}	1.3		μs	Input V_{DD} = 4 V to 6 V
	t_{KL}	65		μs	μPD7519 only
		2.2		μs	Output V_{DD} = 4 V to 6 V
		4.5		μs	μPD7519 only
SI set-up time (to $\overline{SCK}$↑)	t_{SIK}	300		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519 only
SI hold time (after $\overline{SCK}$↑)	t_{KSI}	450		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519 only
SO output delay time (after $\overline{SCK}$↓)	t_{KSO}		850	ns	V_{DD} = 4 V to 6 V
			2000	ns	μPD7519 only

AC Characteristics (cont)

T_A = −10°C to +70°C

Serial Interface Operation, μPD7519H/75CG19H

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{KCY}	2.1		μs	Input V_{DD} = 4 V to 6 V
		12.5		μs	μPD7519H only
		(1)		μs	Output V_{DD} = 4 V to 6 V
		(2)		μ	μPD7519H only
$\overline{SCK}$ pulse width high, low	t_{KH}	0.7		μs	Input V_{DD} = 4 V to 6 V
	t_{KL}	6.5		μs	μPD7519H only
		(3)		μs	Output V_{DD} = 4 V to 6 V
		(4)		μs	μPD7519H only
SI set-up time (to $\overline{SCK}$↑)	t_{SIK}	300		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519H only
SI hold time (after $\overline{SCK}$↑)	t_{KSI}	450		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519H only
SO output delay time (after $\overline{SCK}$↓)	t_{KSO}		500	ns	V_{DD} = 4 V to 6 V
			2000	ns	μPD7519H only

Note:

(1) High speed mode: $16/f_X$ or $16/f_{XX}$
Low speed mode: $64/f_X$ or $64/f_{XX}$

(2) $64/f_X$ or $64/f_{XX}$

(3) High speed mode: $8/f_X$ − 0.8 μs, or $8/f_{XX}$ − 0.8 μs
Low speed mode: $32/f_X$ − 0.8 μs, or $32/f_{XX}$ − 0.8 μs

(4) $32/f_X$ − 2.0 μs, or $32/f_{XX}$ − 2.0 μs

AC Characteristics (cont)

T_A = −10°C to +70°C

Other Operations

μPD7519/7519H: V_{DD} = 4.5 V to 6.0 V
μPD75CG19/75CG19H: V_{DD} = 4.75 V to 5.5 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
INT0 pulse width high, low	t_{I0H}, t_{I0L}	10		μs	
INT1 pulse width high, low	t_{I1H}, t_{I1L}	(1)		μs	
RESET pulse width high, low	t_{RSH}, t_{RSL}	10		μs	

Note:

(1) $26/f_X$ or $26/f_{XX}$

μPD75CG19/75CG19H EPROM Characteristics

T_A = −10°C to +70°C; V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Access time	t_{ACC}			700	ns	
$\overline{CE}$ low set-up time to data valid	t_{CE}			700	ns	
Data valid hold time to $\overline{CE}$ rising edge	t_{IH}	0			ns	

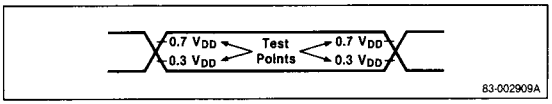
Stop Mode Low Voltage Data Retention Characteristics, μPD7519/7519H

T_A = −10°C to +70°C

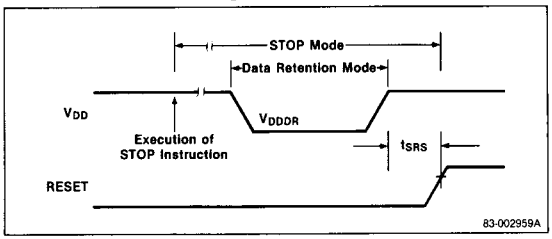
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2 V
RESET set-up time	t_{SRS}	0			μs	

Timing Waveforms

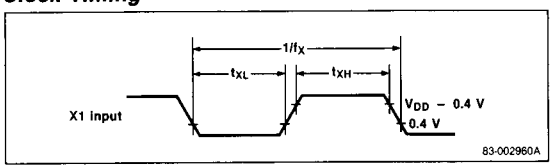
AC Waveform Measurement Points (Except X1, X2)



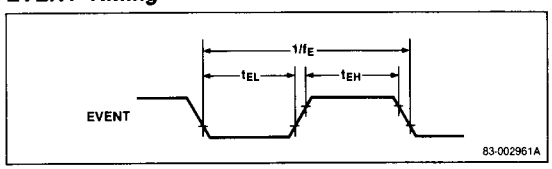
Data Retention Timing



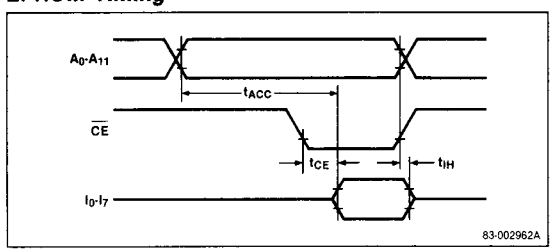
Clock Timing



EVENT Timing



EPROM Timing



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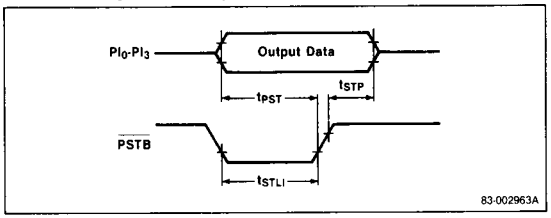
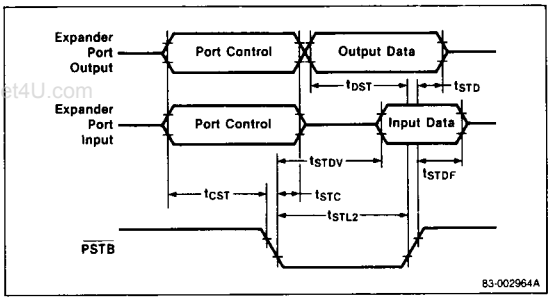
Timing Waveforms (cont)

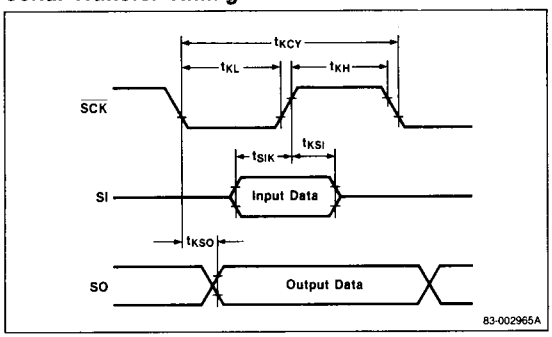
Strobe Output Timing



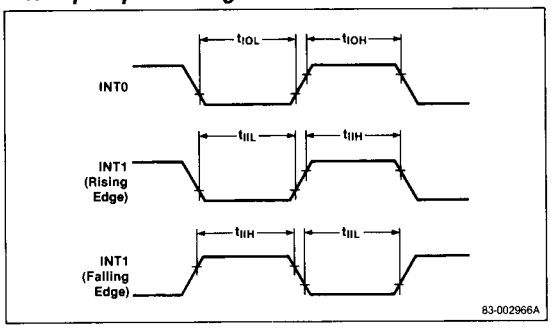
Port 1 I/O Expander I/O Timing



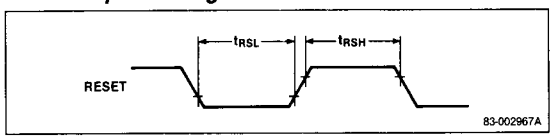
Serial Transfer Timing



Interrupt Input Timing



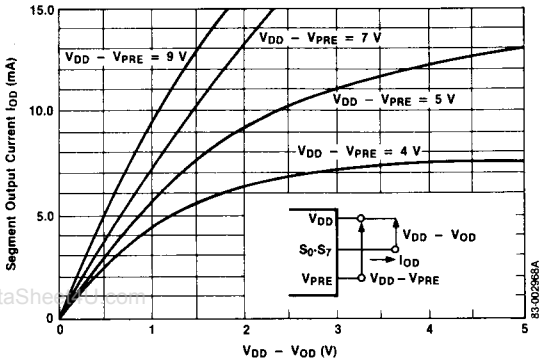
RESET Input Timing



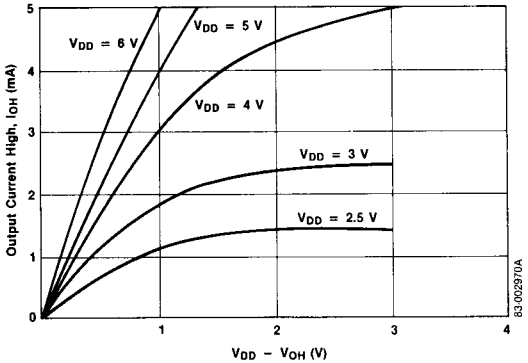
Operating Characteristics, μPD7519/7519H

T_A = 25°C

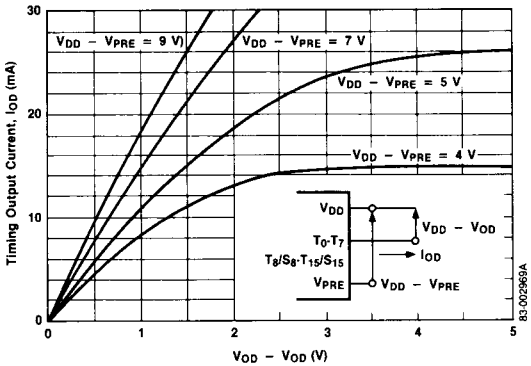
I_{OD} vs (V_{DD} – V_{OD}) (V_{DD} = 4 V to 6 V)



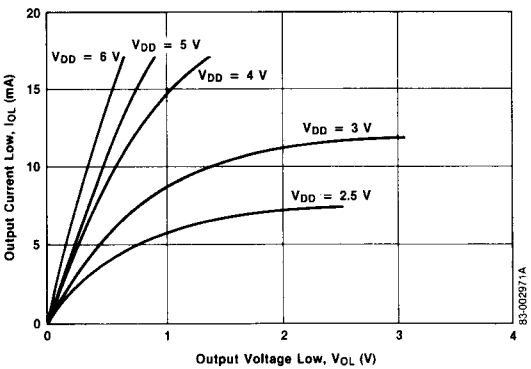
I_{OH} vs (V_{DD} – V_{OH})



I_{OD} vs (V_{DD} – V_{OD}) (V_{DD} = 4 to 6 V)



I_{OL} vs V_{OL}



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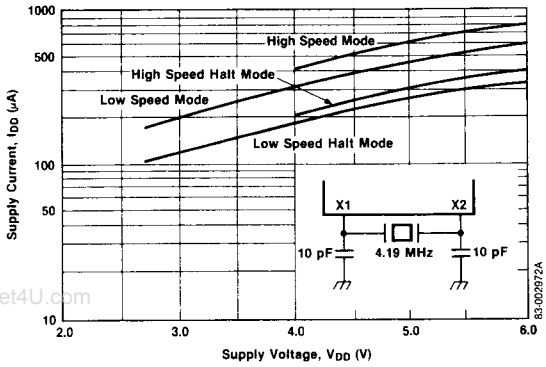
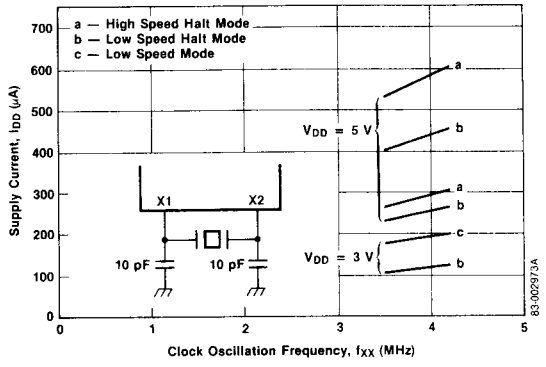
Operating Characteristics, μPD7519H only

T_A = 25°C

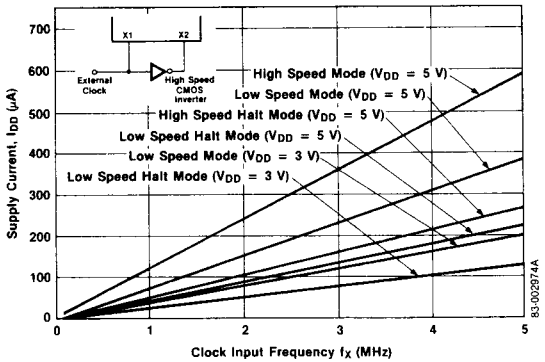
I_{DD} vs V_{DD} (f_{XX} = 4.19 MHz)



I_{DD} vs f_{XX}



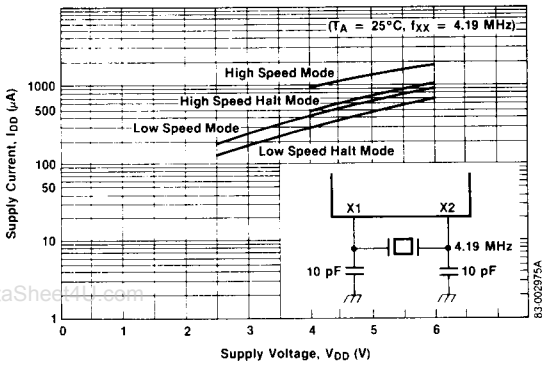
I_{DD} vs f_X



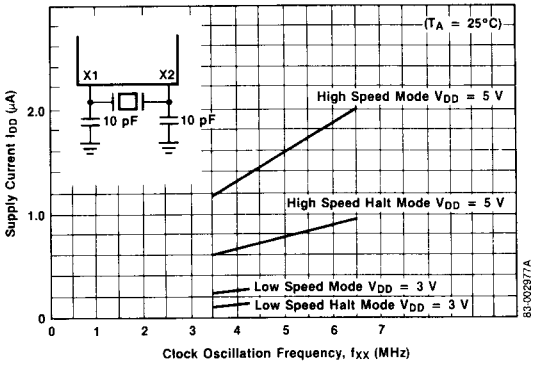
Operating Characteristics, μPD7519 only

T_A = 25°C

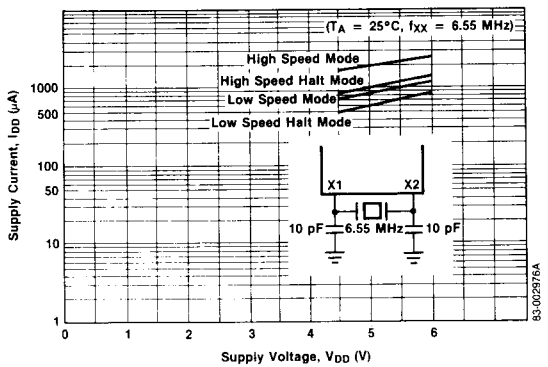
I_{DD} vs V_{DD}



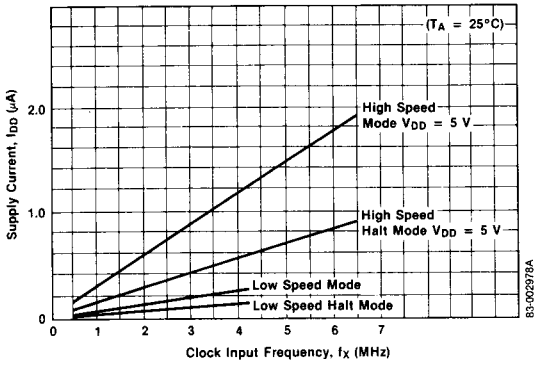
I_{DD} vs f_{XX}



I_{DD} vs V_{DD}



I_{DD} vs f_X



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