

Silicon PNP Power Transistors

2N6029 2N6030

DESCRIPTION

- With TO-3 package
- Complement to type 2N5629 2N5630
- High power dissipations

APPLICATIONS

- For high voltage and high power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

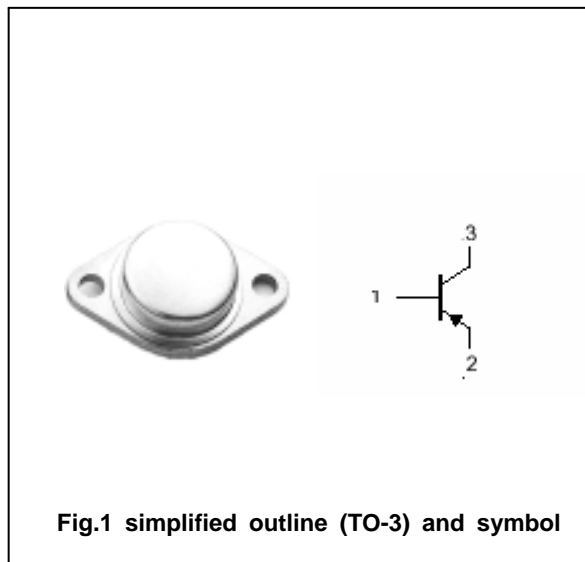


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CB0}	Collector-base voltage	2N6029	-100	V
		2N6030	-120	
V _{CEO}	Collector-emitter voltage	2N6029	-100	V
		2N6030	-120	
V _{EBO}	Emitter-base voltage	Open collector	-7	V
I _C	Collector current		-16	A
I _{CM}	Collector current-peak		-20	A
I _B	Base current		-5.0	A
P _D	Total Power Dissipation	T _C =25	200	W
T _j	Junction temperature		150	
T _{stg}	Storage temperature		-65~200	

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-c}	Thermal resistance junction to case	0.875	/W

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	2N6029	I _C =-0.2A ; I _B =0	-100			V
		2N6030		-120			
V _{CEsat-1}	Collector-emitter saturation voltage		I _C =-10A; I _B =-1A			-1.0	V
V _{CEsat-2}	Collector-emitter saturation voltage		I _C =-16A ; I _B =-4A			-2.0	V
V _{BEsat}	Base-emitter saturation voltage		I _C =-10A; I _B =-1A			-1.8	V
V _{BE}	Base-emitter on voltage		I _C =-8A ; V _{CE} =-2V			-1.5	V
I _{CBO}	Collector cut-off current		V _{CB} =ratedV _{CB0} ; I _E =0			-1.0	mA
I _{CEO}	Collector cut-off current	2N6029	V _{CE} =-50V; I _B =0			-1.0	mA
		2N6030	V _{CE} =-60V; I _B =0				
I _{CEV}	Collector cut-off current (V _{BE(off)} =1.5V)	V _{CE} =ratedV _{CB}				-1.0	mA
		V _{CE} =ratedV _{CB} ; T _C =150				-5.0	
I _{EBO}	Emitter cut-off current		V _{EB} =-7V; I _C =0			-1.0	mA
h _{FE-1}	DC current gain	2N6029	I _C =-8A ; V _{CE} =-2V	25		100	
		2N6030		20		80	
h _{FE-2}	DC current gain		I _C =-16A ; V _{CE} =-2V	4			
C _{OB}	Output capacitance		I _E =0 ; V _{CB} =-10V ; f=0.1MHz			1000	pF
f _T	Transition frequency		I _C =-1A ; V _{CE} =-20V	1.0			MHz

PACKAGE OUTLINE

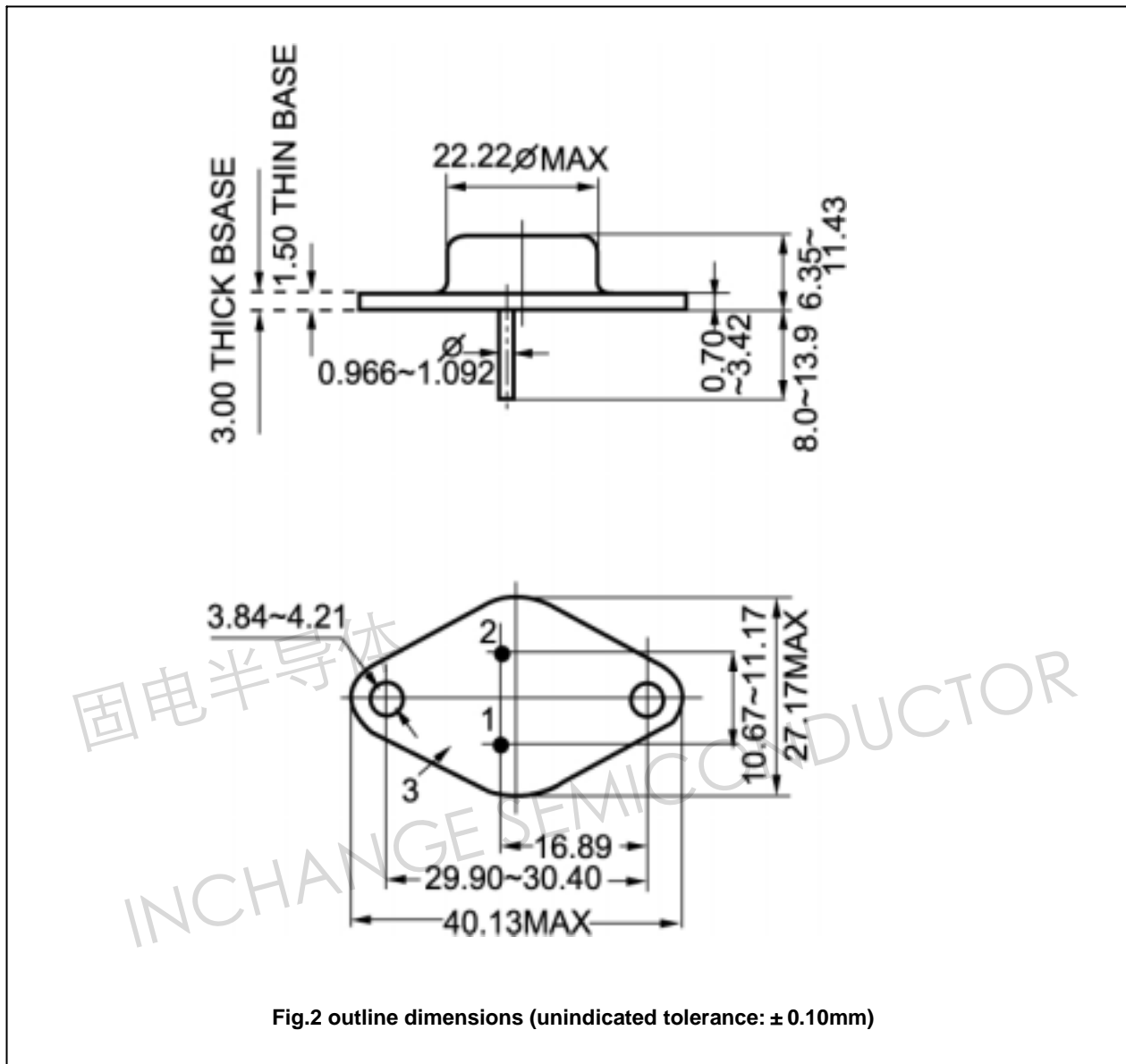


Fig.2 outline dimensions (unindicated tolerance: $\pm 0.10\text{mm}$)