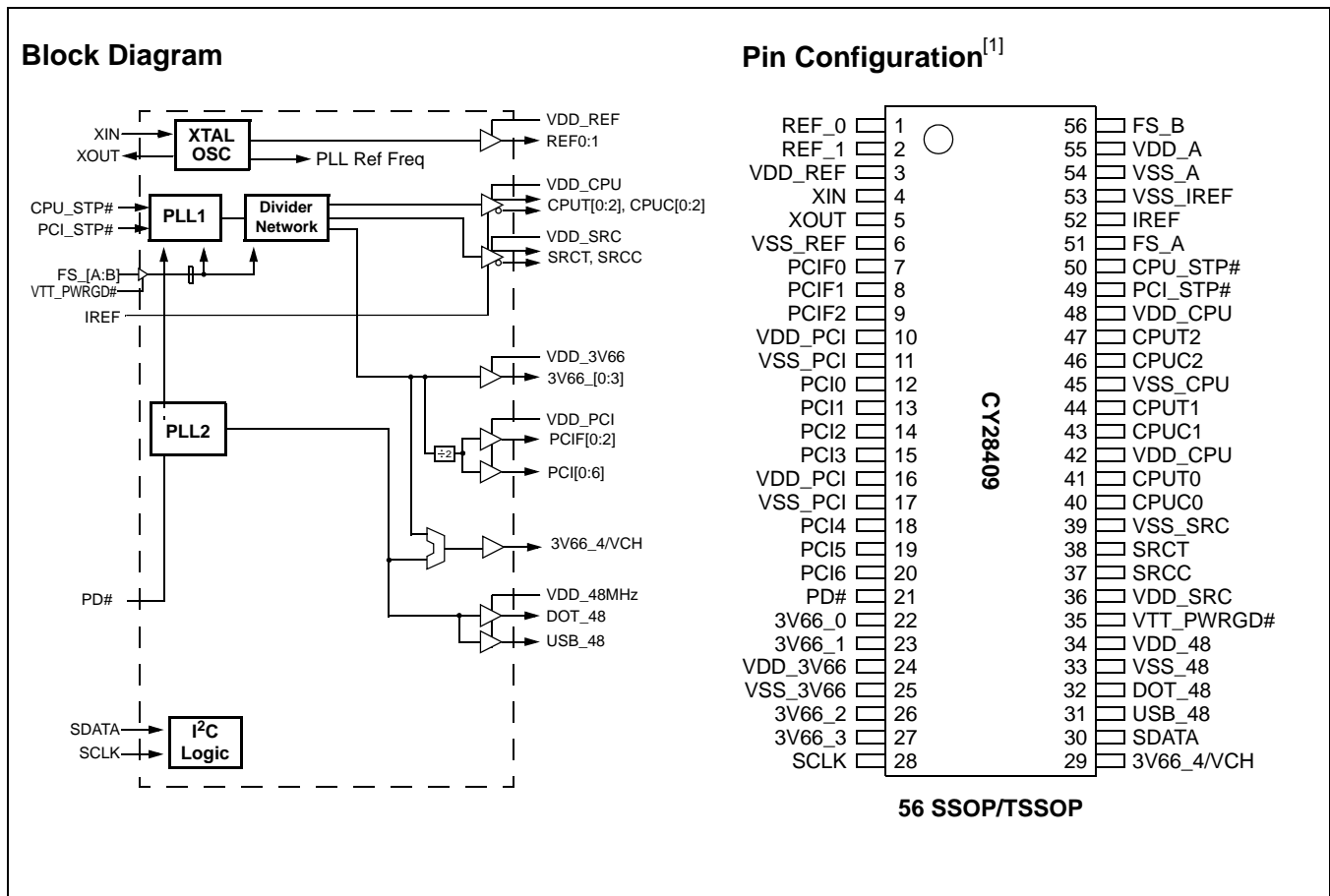


Clock Synthesizer with Differential SRC and CPU Outputs

Features

- Supports Intel® Pentium® 4-type CPUs
- Selectable CPU frequencies
- 3.3V power supply
- Ten copies of PCI clocks
- Five copies of 3V66 with one optional VCH
- Two copies 48-MHz USB clocks
- Three differential CPU clock pairs
- One differential SRC clock
- I²C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum EMI reduction
- 56-pin SSOP and TSSOP packages

| CPU | SRC | 3V66 | PCI | REF | 48M |
|-----|-----|------|------|-----|-----|
| x 3 | x 1 | x 5 | x 10 | x 2 | x 2 |



Note:

1. Signals marked with [*] and [**] have internal pull-up and pull-down resistors, respectively.

Pin Description

| Pin No. | Name | Type | Description |
|--------------------------|------------|--------|--|
| 1, 2 | REF(0:1) | O, SE | Reference Clock. 3.3V 14.318-MHz clock output. |
| 4 | XIN | I | Crystal Connection or External Reference Frequency Input. This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| 5 | XOUT | O, SE | Crystal Connection. Connection for an external 14.318-MHz crystal output. |
| 41,44,47 | CPUT(0:2) | O, DIF | CPU Clock Output. Differential CPU clock outputs. See <i>Table 1</i> for frequency configuration. |
| 40,43,46 | CPUC(0:2) | O, DIF | CPU Clock Output. Differential CPU clock outputs. See <i>Table 1</i> for frequency configuration. |
| 38, 37 | SRCT, SRCC | O, DIF | Differential serial reference clock. |
| 22,23,26,27 | 3V66(0:3) | O, SE | 66-MHz Clock Output. 3.3V 66-MHz clock from internal VCO. |
| 29 | 3V66_4VCH | O, SE | 48-/66-MHz Clock Output. 3.3V selectable through SMBus to be 66 or 48 MHz. |
| 7,8,9 | PCIF(0:2) | O, SE | Free-running PCI Output. 33-MHz clocks divided down from 3V66. |
| 12,13,14, 15,18,19,20 | PCI(0:6) | O, SE | PCI Clock Output. 33-MHz clocks divided down from 3V66. |
| 31, | USB_48 | O, SE | Fixed 48-MHz clock output. |
| 32 | DOT_48 | O, SE | Fixed 48-MHz clock output. |
| 51,56 | FS_A, FS_B | I | 3.3V LVTTTL input for CPU frequency selection. |
| 52 | IREF | I | Current Reference. A precision resistor is attached to this pin which is connected to the internal current reference. |
| 21 | PD# | I, PU | 3.3V LVTTTL input for Power-Down# active LOW. |
| 50 | CPU_STP# | I, PU | 3.3V LVTTTL input for CPU_STP# active LOW. |
| 49 | PCI_STP# | I, PU | 3.3V LVTTTL input for PCI_STP# active LOW. |
| 35 | VTT_PWRGD# | I | 3.3V LVTTTL input is a level sensitive strobe used to latch the FS_A and FS_B inputs (active LOW). |
| 30 | SDATA | I/O | SMBus-compatible SDATA. |
| 28 | SCLK | I | SMBus-compatible SCLOCK. |
| 53 | VSS_IREF | GND | Ground for current reference. |
| 55 | VDD_A | PWR | 3.3V power supply for PLL. |
| 54 | VSS_A | GND | Ground for PLL. |
| 42,48 | VDD_CPU | PWR | 3.3V power supply for outputs. |
| 45 | VSS_CPU | GND | Ground for outputs. |
| 36 | VDD_SRC | PWR | 3.3V power supply for outputs. |
| 39 | VSS_SRC | GND | Ground for outputs. |
| 34 | VDD_48 | PWR | 3.3V power supply for outputs. |
| 33 | VSS_48 | GND | Ground for outputs. |
| 10,16 | VDD_PCI | PWR | 3.3V power supply for outputs. |
| 11,17 | VSS_PCI | GND | Ground for outputs. |
| 24 | VDD_3V66 | PWR | 3.3V power supply for outputs. |
| 25 | VSS_3V66 | GND | Ground for outputs. |
| 3 | VDD_REF | PWR | 3.3V power supply for outputs. |
| 6 | VSS_REF | GND | Ground for outputs. |

Table 1. Frequency Select Table (FS_A, FS_B)

| FS_A | FS_B | CPU | SRC | 3V66 | PCIF/PCI | REF0 | REF1 | USB/DOT |
|------|------|---------|-------------|--------|----------|----------|-----------|---------|
| 0 | 0 | 100 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 0 | MID | REF/N | REF/N | REF/N | REF/N | REF/N | REF/N | REF/N |
| 0 | 1 | 200 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 0 | 133 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | MID | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

Table 2. Frequency Select Table (FS_A, FS_B) SMBus Bit 5 of Byte 6 = 1

| FS_A | FS_B | CPU | SRC | 3V66 | PCIF/PCI | REF0 | REF1 | USB/DOT |
|------|------|---------|-------------|--------|----------|----------|-----------|---------|
| 0 | 0 | 200 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 0 | 1 | 400 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 0 | 266 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |

Frequency Select Pins (FS_A, FS_B)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A and FS_B inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A and FS_B input values. For all logic levels of FS_A and FS_B except MID, VTT_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT_PWRGD# has been sampled LOW, all further VTT_PWRGD#, FS_A and FS_B transitions will be ignored. In the case where FS_B is at mid level when VTT_PWRGD# is sampled LOW, the clock chip will assume “Test Clock Mode.” Once “Test Clock Mode” has been invoked, all further FS_B transitions will be ignored and FS_A will asynchronously select between the Hi-Z and REF/N mode. Exiting test mode is accomplished by cycling power with FS_B in a HIGH or LOW state.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial

Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 3.

The block write and block read protocol is outlined in Table 4 while Table 5 outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3. Command Code Definition

| Bit | Description |
|-------|---|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

Table 4. Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|--|---------------------|--|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '00000000' stands for block operation | 11:18 | Command Code – 8 bits '00000000' stands for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |

Table 4. Block Read and Block Write Protocol (continued)

| Block Write Protocol | | Block Read Protocol | |
|----------------------|--------------------------|---------------------|---------------------------------|
| Bit | Description | Bit | Description |
| 20:27 | Byte Count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29:36 | Data byte 1 – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 2 – 8 bits | 30:37 | Byte count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge from master |
| | | 39:46 | Data byte from slave – 8 bits |
| | Data Byte (N-1) – 8 bits | 47 | Acknowledge from master |
| | Acknowledge from slave | 48:55 | Data byte from slave – 8 bits |
| | Data Byte N – 8 bits | 56 | Acknowledge from master |
| | Acknowledge from slave | | Data byte N from slave – 8 bits |
| | Stop | | Acknowledge from master |
| | | | Stop |

Table 5. Byte Read and Byte Write protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|---|--------------------|---|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[4:0] of the command code represents the offset of the byte to be accessed | 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[4:0] of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte from master – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29 | Stop | 28 | Read = 1 |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave – 8 bits |
| | | 38 | Acknowledge from master |
| | | 39 | Stop |

Control Registers

Byte 0:Control Register 0

| Bit | @Pup | Name | Description |
|-----|------|-------------|--|
| 7 | 0 | Reserved | Reserved, Set = 0 |
| 6 | 1 | PCIF PCI | PCI Drive Strength Override 0 = Force All PCI and PCIF Outputs to Low Drive Strength 1 = Force All PCI and PCIF Outputs to High Drive Strength |
| 5 | 0 | Reserved | Reserved, Set = 0 |
| 4 | 0 | Reserved | Reserved, Set = 0 |

Byte 0: Control Register 0 (continued)

| Bit | @Pup | Name | Description |
|-----|---------------------|----------|---|
| 3 | Externally Selected | PCI_STP# | PCI_STP# reflects the current value of the external PCI_STP# pin. 0 = PCI_STP# pin is LOW. |
| 2 | Externally Selected | CPU_STP# | CPU_STP# reflects the current value of the external CPU_STP# pin. 0 = CPU_STP# pin is LOW. |
| 1 | Externally Selected | FS_B | FS_B reflects the value of the FS_B pin sampled on power-up. |
| 0 | Externally Selected | FS_A | FS_A reflects the value of the FS_A pin sampled on power-up. |

Byte 1: Control Register 1

| Bit | @Pup | Name | Description |
|-----|------|--------------|--|
| 7 | 0 | SRCT, SRCC | Allows control of SRCT/C with assertion of PCI_STP# or SW PCI_STP 0 = Free Running, 1 = Stopped with PCI_STP# |
| 6 | 1 | SRCT, SRCC | SRCT/C Output Enable; 0 = Disabled (Hi-z), 1 = Enabled |
| 5 | 1 | Reserved | Reserved, Set = 1 |
| 4 | 1 | Reserved | Reserved, Set = 1 |
| 3 | 1 | Reserved | Reserved, Set = 1 |
| 2 | 1 | CPUT2, CPUC2 | CPUT/C2 Output Enable; 0 = Disabled (Hi-z), 1 = Enabled |
| 1 | 1 | CPUT1, CPUC1 | CPUT/C1 Output Enable; 0 = Disabled (Hi-z), 1 = Enabled |
| 0 | 1 | CPUT0, CPUC0 | CPUT/C0 Output Enable; 0 = Disabled (Hi-z), 1 = Enabled |

Byte 2: Control Register 2

| Bit | @Pup | Name | Description |
|-----|------|--------------|---|
| 7 | 0 | SRCT, SRCC | SRCT/C Pwrdown Drive Mode 0 = Driven during power-down, 1 = Three-state during power-down |
| 6 | 0 | SRCT, SRCC | SRCT/C Stop Drive Mode 0 = Driven during PCI_STP, 1 = Three-state during PCI_STP |
| 5 | 0 | CPUT2, CPUC2 | CPUT/C2 Pwrdown Drive Mode 0 = Driven during power-down, 1 = Three-state during power-down |
| 4 | 0 | CPUT1, CPUC1 | CPUT/C1 Pwrdown Drive Mode 0 = Driven during power-down, 1 = Three-state during power-down |
| 3 | 0 | CPUT0, CPUC0 | CPUT/C0 Pwrdown Drive Mode 0 = Driven during power-down, 1 = Three-state during power-down |
| 2 | 0 | CPUT2, CPUC2 | CPUT/C2 stop Drive Mode 0 = Driven when stopped, 1 = Three-state when stopped |
| 1 | 0 | CPUT1, CPUC1 | CPUT/C1 stop Drive Mode 0 = Driven when stopped, 1 = Three-state when stopped |
| 0 | 0 | CPUT0, CPUC0 | CPUT/C0 stop Drive Mode 0 = Driven when stopped, 1 = Three-state when stopped |

Byte 3: Control Register 3

| Bit | @Pup | Name | Description |
|-----|------|-------------|---|
| 7 | 1 | SW PCI STOP | SW PCI_STP Function 0= PCI_STP assert, 1= PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses. |
| 6 | 1 | PCI6 | PCI6 Output Enable 0 = Disabled, 1 = Enabled |

Byte 3: Control Register 3 (continued)

| Bit | @Pup | Name | Description |
|-----|------|------|---|
| 5 | 1 | PCI5 | PCI5 Output Enable 0 = Disabled, 1 = Enabled |
| 4 | 1 | PCI4 | PCI4 Output Enable 0 = Disabled, 1 = Enabled |
| 3 | 1 | PCI3 | PCI3 Output Enable 0 = Disabled, 1 = Enabled |
| 2 | 1 | PCI2 | PCI2 Output Enable 0 = Disabled, 1 = Enabled |
| 1 | 1 | PCI1 | PCI1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | PCI0 | PCI0 Output Enable 0 = Disabled, 1 = Enabled |

Byte 4: Control Register 4

| Bit | @Pup | Name | Description |
|-----|------|--------|--|
| 7 | 0 | USB_48 | USB_48 Drive Strength 0 = High drive strength, 1 = Low drive strength |
| 6 | 1 | USB_48 | USB_48 Output Enable 0 = Disabled, 1 = Enabled |
| 5 | 0 | PCIF2 | Allow control of PCIF2 with assertion of PCI_STP# or SW PCI_STP 0 = Free Running, 1 = Stopped with PCI_STP# |
| 4 | 0 | PCIF1 | Allow control of PCIF1 with assertion of PCI_STP# or SW PCI_STP 0 = Free Running, 1 = Stopped with PCI_STP# |
| 3 | 0 | PCIF0 | Allow control of PCIF0 with assertion of PCI_STP# or SW PCI_STP 0 = Free Running, 1 = Stopped with PCI_STP# |
| 2 | 1 | PCIF2 | PCIF2 Output Enable 0 = Disabled, 1 = Enabled |
| 1 | 1 | PCIF1 | PCIF1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | PCIF0 | PCIF0 Output Enable 0 = Disabled, 1 = Enabled |

Byte 5: Control Register 5

| Bit | @Pup | Name | Description |
|-----|------|------------|--|
| 7 | 1 | DOT_48 | DOT_48 Output Enable 0 = Disabled, 1 = Enabled |
| 6 | 1 | Reserved | Reserved, Set = 1 |
| 5 | 0 | 3V66_4/VCH | VCH Select 66-MHz/48-MHz 0 = 3V66 mode, 1 = VCH (48-MHz) mode |
| 4 | 1 | 3V66_4/VCH | 3V66_4/VCH Output Enable 0 = Disabled, 1 = Enabled |
| 3 | 1 | 3V66_3 | 3V66_3 Output Enable 0 = Disabled, 1 = Enabled |
| 2 | 1 | 3V66_2 | 3V66_2 Output Enable 0 = Disabled, 1 = Enabled |
| 1 | 1 | 3V66_1 | 3V66_1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | 3V66_0 | 3V66_0 Output Enable 0 = Disabled, 1 = Enabled |

Byte 6: Control Register 6

| Bit | @Pup | Name | Description |
|-----|------|---|---|
| 7 | 0 | Reserved | Reserved, Set = 0 |
| 6 | 0 | Reserved | Reserved, Set = 0 |
| 5 | 0 | CPUC0, CPUT0 CPUC1, CPUT1 CPUC2, CPUT2 | FS_A & FS_B Operation 0 = Normal, 1 = Test mode |
| 4 | 0 | SRCT, SRCC | SRC Frequency Select 0 = 100 MHz, 1 = 200 MHz |
| 3 | 0 | Reserved | Reserved, Set = 0 |
| 2 | 0 | PCIF PCI 3V66 SRCT,SRCC CPUT_ITP,CPUC_ITP | Spread Spectrum Enable 0 = Spread Off, 1 = Spread On |
| 1 | 1 | REF_1 | REF_1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | REF_0 | REF_0 Output Enable 0 = Disabled, 1 = Enabled |

Byte 7: Vendor ID

| Bit | @Pup | Name | Description |
|-----|------|-------------------|-------------------|
| 7 | 0 | Revision ID Bit 3 | Revision ID Bit 3 |
| 6 | 1 | Revision ID Bit 2 | Revision ID Bit 2 |
| 5 | 0 | Revision ID Bit 1 | Revision ID Bit 1 |
| 4 | 0 | Revision ID Bit 0 | Revision ID Bit 0 |
| 3 | 1 | Vendor ID Bit 3 | Vendor ID Bit 3 |
| 2 | 0 | Vendor ID Bit 2 | Vendor ID Bit 2 |
| 1 | 0 | Vendor ID Bit 1 | Vendor ID Bit 1 |
| 0 | 0 | Vendor ID Bit 0 | Vendor ID Bit 0 |

Table 6. Crystal Recommendations

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|------------------|-----|----------|----------|--------------|------------------|-----------------|------------------|------------------|--------------|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 50 ppm | 50 ppm | 5 ppm |

Crystal Recommendations

The CY28409 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28409 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is **not true**.

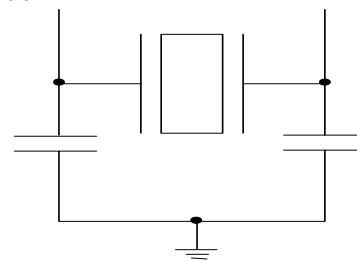


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

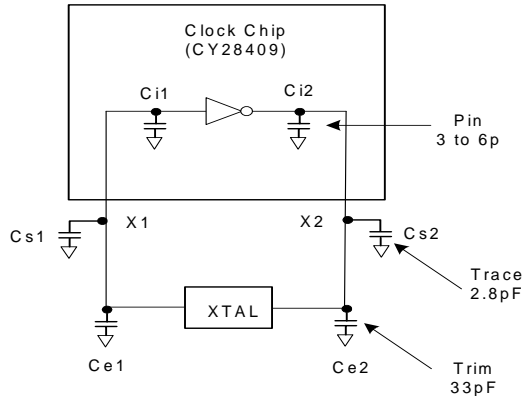


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

$$\begin{aligned}
 &\text{Load Capacitance (each side)} \\
 &Ce = 2 * CL - (Cs + Ci) \\
 &\text{Total Capacitance (as seen by the crystal)} \\
 &CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}
 \end{aligned}$$

- CL.....Crystal load capacitance
- CLe..... Actual loading seen by crystal using standard value trim capacitors
- Ce..... External trim capacitors
- Cs..... Stray capacitance (terraced)
- Ci..... Internal capacitance (lead frame, bond wires etc.)

PD# (Power-down) Clarification

The PD# (Power-down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is LOW, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so as not to cause glitches while changing to the low 'stopped' state.

PD# Assertion

When PD# is sampled LOW by two consecutive rising edges of the CPUC clock then all clock outputs (except CPU) clocks must be held LOW on their next HIGH-to-LOW transition. CPU clocks must be held with CPU clock pin driven HIGH with a value of 2 x Iref and CPUC undriven. Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete

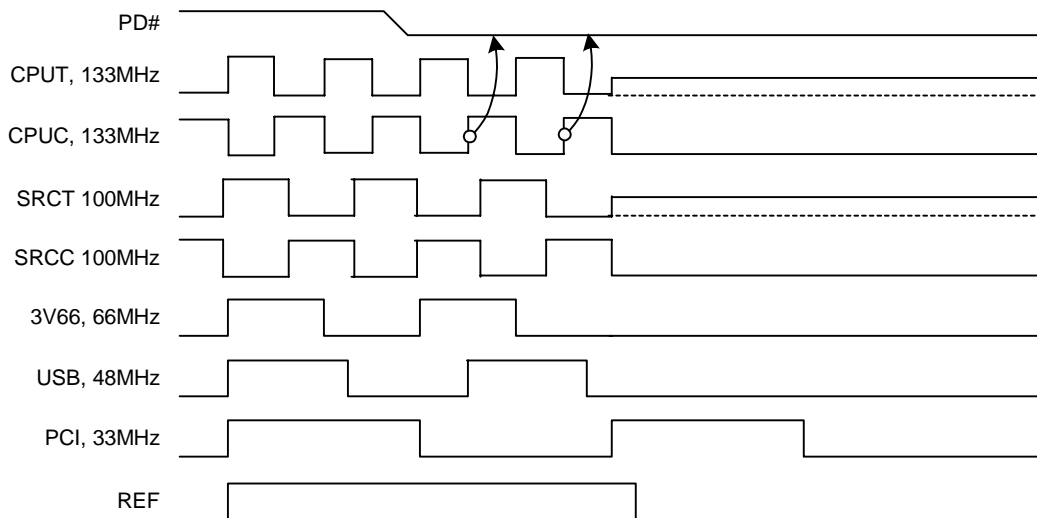


Figure 3. Power-down Assertion Timing Waveform

PD# Deassertion

The power-up latency between PD# rising to a valid logic '1' level and the starting of all clocks is less than 1.8 ms.

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped after being sampled by two rising edges of the internal CPUT clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to (Mult 0 'select') x (Iref), and the CPUC signal will not be driven. Due to the external pull-down circuitry, CPUC will be LOW during this stopped state.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

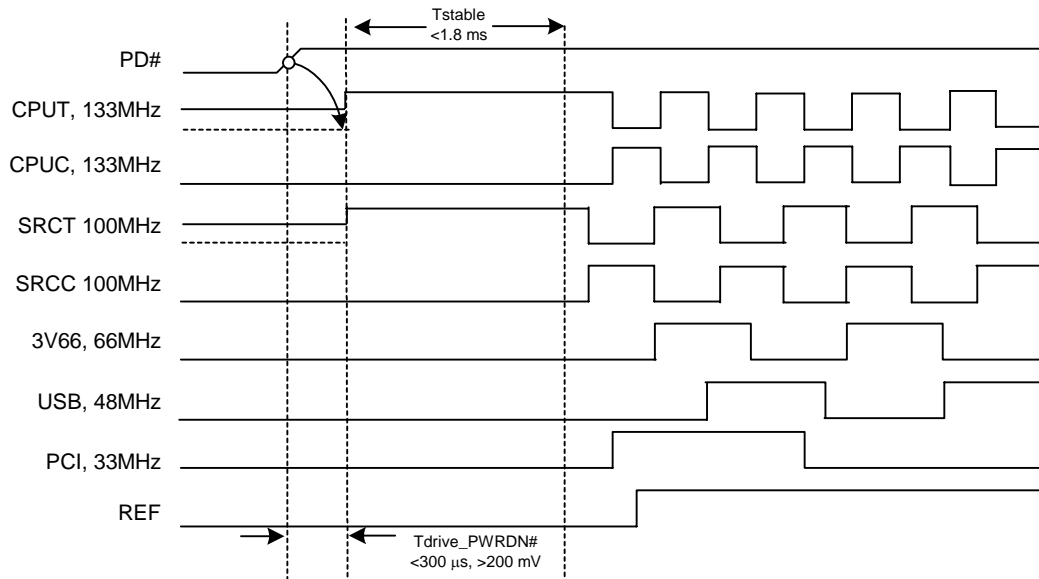


Figure 4. Power-down Deassertion Timing Waveform

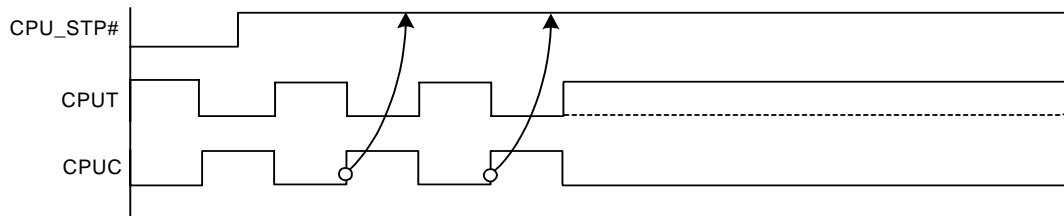


Figure 5. CPU_STP# Assertion Waveform

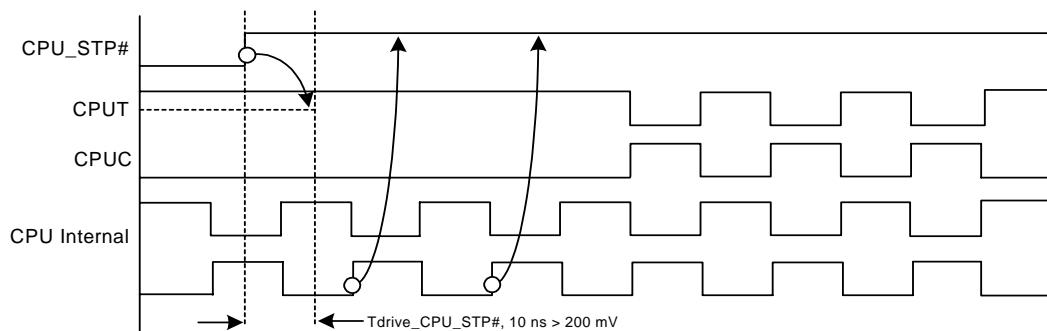


Figure 6. CPU_STP# Deassertion Waveform

PCI_STP# Assertion^[2]

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See Figure 7.) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free-running.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a high level.

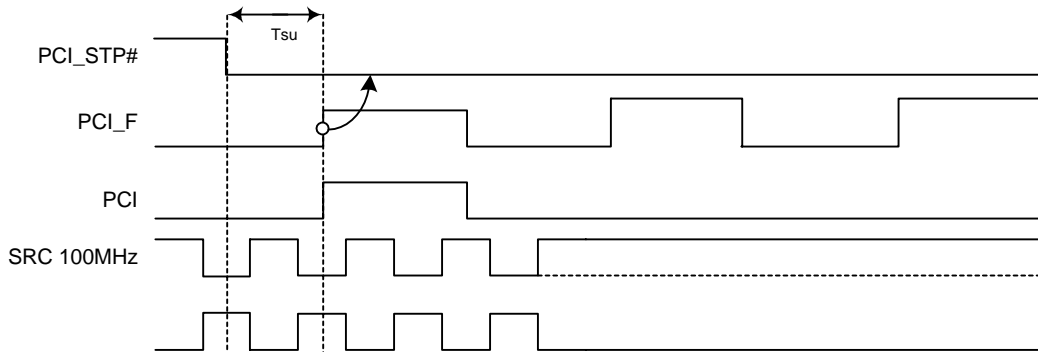


Figure 7. PCI_STP# Assertion Waveform

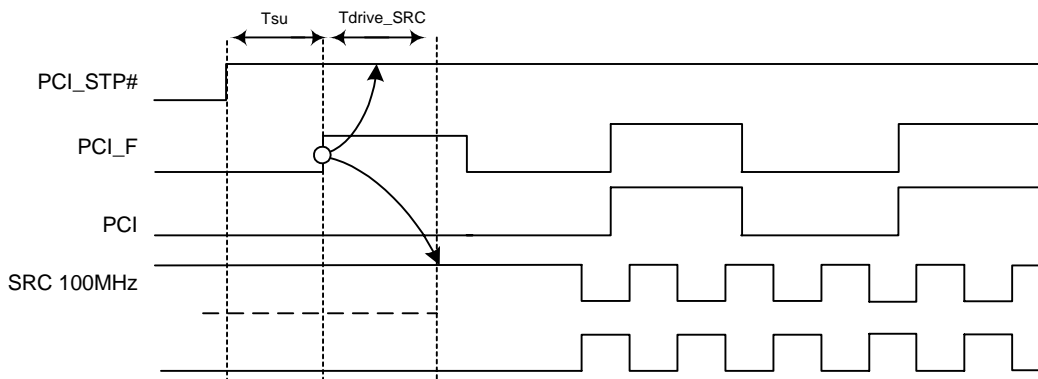


Figure 8. PCI_STP# Deassertion Waveform

Note:

2. The PCI STOP function is controlled by two inputs. One is the device PCI_STP# pin number 34 and the other is SMBus byte 0 bit 3. These two inputs are logically ANDed. If either the external pin or the internal SMBus register bit is set low then the stoppable PCI clocks will be stopped in a logic low state. Reading SMBus Byte 0 Bit 3 will return a 0 value if either of these control bits are set LOW thereby indicating the device's stoppable PCI clocks are not running.

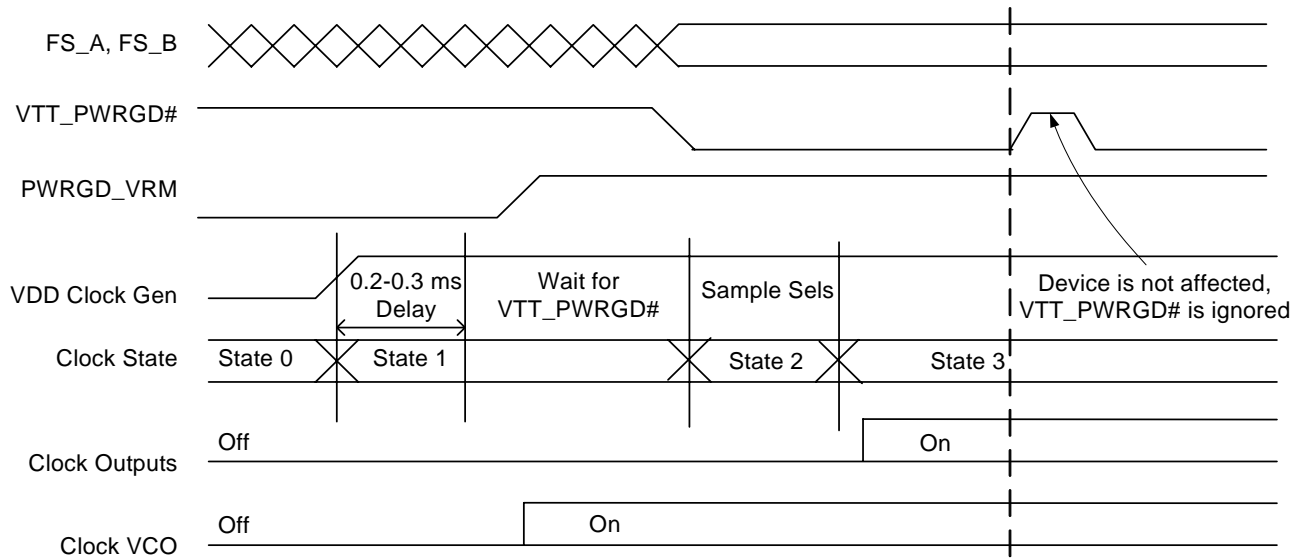


Figure 9. VTT_PWRGD# Timing Diagram

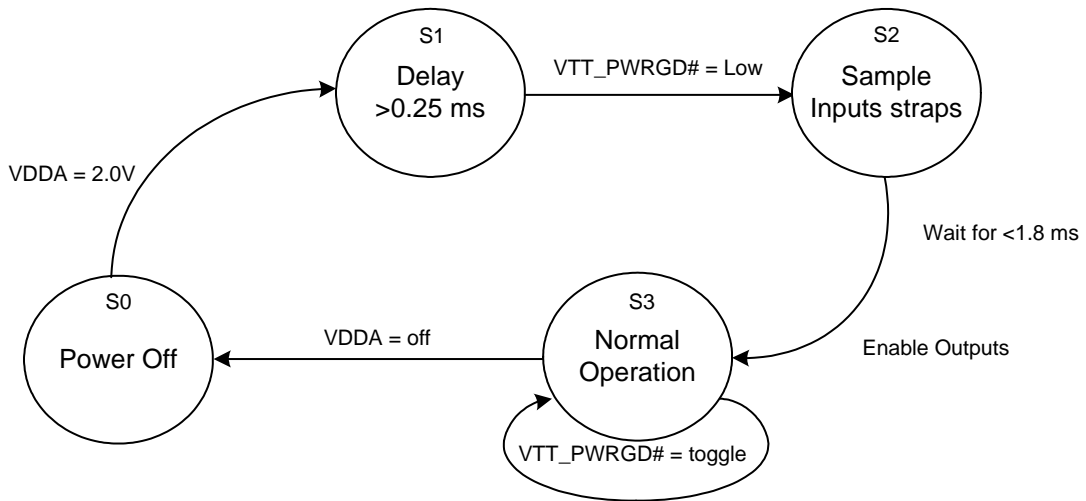


Figure 10. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V _{DD} | Core Supply Voltage | | -0.5 | 4.6 | V |
| V _{DD_A} | Analog Supply Voltage | | -0.5 | 4.6 | V |
| V _{IN} | Input Voltage | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | VDC |
| T _S | Temperature, Storage | Non-functional | -65 | 150 | °C |
| T _A | Temperature, Operating Ambient | Functional | 0 | 70 | °C |
| T _J | Temperature, Junction | Functional | - | 150 | °C |
| ∅ _{JC} | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | - | 15 | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | JEDEC (JESD 51) | - | 45 | °C/W |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |
| UL-94 | Flammability Rating | @ 1/8 in. | | V-0 | |
| MSL | Moisture Sensitivity Level | | | 1 | |

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|--|-------------------------------|--|-----------------------|-----------------------|------|
| V _{DD_A} , V _{DD_REF} , V _{DD_PCI} , V _{DD_3V66} , V _{DD_48} , V _{DD_CPU} | 3.3V Operating Voltage | 3.3 ± 5% | 3.135 | 3.465 | V |
| V _{IL2C} | Input Low Voltage | SDATA, SCLK | - | 1.0 | V |
| V _{IH2C} | Input High Voltage | SDATA, SCLK | 2.2 | - | V |
| V _{IL} | Input Low Voltage | | V _{SS} - 0.5 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | V _{DD} + 0.5 | V |
| I _{IL} | Input Low Leakage Current | except internal pull-ups resistors, 0 < V _{IN} < V _{DD} | -5 | | μA |
| I _{IH} | Input High Leakage Current | except internal pull-down resistors, 0 < V _{IN} < V _{DD} | | 5 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 1 mA | - | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -1 mA | 2.4 | - | V |
| I _{OZ} | High-impedance Output Current | | -10 | 10 | μA |
| I _{DD} | Dynamic Supply Current | All outputs loaded per Table 9 and Figure 11 | - | 350 | mA |
| C _{IN} | Input Pin Capacitance | | 2 | 5 | pF |
| C _{OUT} | Output Pin Capacitance | | 3 | 6 | pF |
| L _{IN} | Pin Inductance | | - | 7 | nH |
| V _{XIH} | Xin High Voltage | | 0.7V _{DD} | V _{DD} | V |
| V _{XIL} | Xin Low Voltage | | 0 | 0.3V _{DD} | V |
| I _{PD3.3V} | Power-down Supply Current | PD# Asserted | - | 1 | mA |

AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|---------------------------|---|--------|------|------|
| Crystal | | | | | |
| T _{DC} | XIN Duty Cycle | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| T _{PERIOD} | XIN Period | When XIN is driven from an external clock source | 69.841 | 71.0 | ns |
| T _R / T _F | XIN Rise and Fall Times | Measured between 0.3V _{DD} and 0.7V _{DD} | - | 10.0 | ns |
| T _{CCJ} | XIN Cycle to Cycle Jitter | As an average over 1-μs duration | - | 500 | ps |
| L _{ACC} | Long-term Accuracy | Over 150 ms | | 300 | ppm |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|--------------------------------------|---|---------|-------------------------|------|
| CPU at 0.7V | | | | | |
| T _{DC} | CPUT and CPUC Duty Cycle | Measured at crossing point V _{OX} | 45 | 55 | % |
| T _{PERIOD} | 100-MHz CPUT and CPUC Period | Measured at crossing point V _{OX} | 9.9970 | 10.003 | ns |
| T _{PERIOD} | 133-MHz CPUT and CPUC Period | Measured at crossing point V _{OX} | 7.4978 | 7.5023 | ns |
| T _{PERIOD} | 200-MHz CPUT and CPUC Period | Measured at crossing point V _{OX} | 4.9985 | 5.0015 | ns |
| T _{SKEW} | Any CPUT/C to CPUT/C Clock Skew | Measured at crossing point V _{OX} | – | 100 | ps |
| T _{CCJ} | CPUT/C Cycle to Cycle Jitter | Measured at crossing point V _{OX} | – | 125 | ps |
| T _R / T _F | CPUT and CPUC Rise and Fall Times | Measured from V _{OL} = 0.175 to V _{OH} = 0.525V | 175 | 700 | ps |
| T _{RFM} | Rise/Fall Matching | Determined as a fraction of 2*(T _R – T _F)/(T _R + T _F) | – | 20 | % |
| ΔT _R | Rise Time Variation | | – | 125 | ps |
| ΔT _F | Fall Time Variation | | – | 125 | ps |
| V _{HIGH} | Voltage High | Math averages <i>Figure 11</i> | 660 | 850 | mV |
| V _{LOW} | Voltage Low | Math averages <i>Figure 11</i> | –150 | – | mV |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| V _{OVS} | Maximum Overshoot Voltage | | – | V _{HIGH} + 0.3 | V |
| V _{UDS} | Minimum Undershoot Voltage | | –0.3 | – | V |
| V _{RB} | Ring Back Voltage | See <i>Figure 11</i> . Measure SE | – | 0.2 | V |
| SRC | | | | | |
| T _{DC} | SRCT and SRCC Duty Cycle | Measured at crossing point V _{OX} | 45 | 55 | % |
| T _{PERIOD} | 100 MHz SRCT and SRCC Period | Measured at crossing point V _{OX} | 9.9970 | 10.003 | ns |
| T _{PERIOD} | 200 MHz SRCT and SRCC Period | Measured at crossing point V _{OX} | 4.9985 | 5.0015 | ns |
| T _{CCJ} | SRCT/C Cycle to Cycle Jitter | Measured at crossing point V _{OX} | – | 125 | ps |
| L _{ACC} | SRCT/C Long Term Accuracy | Measured at crossing point V _{OX} | – | 300 | ppm |
| T _R / T _F | SRCT and SRCC Rise and Fall Times | Measured from V _{OL} = 0.175 to V _{OH} = 0.525V | 175 | 700 | ps |
| T _{RFM} | Rise/Fall Matching | Determined as a fraction of 2*(T _R – T _F)/(T _R + T _F) | – | 20 | % |
| ΔT _R | Rise Time Variation | | – | 125 | ps |
| ΔT _F | Fall Time Variation | | – | 125 | ps |
| V _{HIGH} | Voltage High | Math averages <i>Figure 11</i> | 660 | 850 | mV |
| V _{LOW} | Voltage Low | Math averages <i>Figure 11</i> | –150 | – | mV |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| V _{OVS} | Maximum Overshoot Voltage | | – | V _{HIGH} + 0.3 | V |
| V _{UDS} | Minimum Undershoot Voltage | | –0.3 | – | V |
| V _{RB} | Ring Back Voltage | See <i>Figure 11</i> . Measure SE | – | 0.2 | V |
| 3V66 | | | | | |
| T _{DC} | 3V66 Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Spread Disabled 3V66 Period | Measurement at 1.5V | 14.9955 | 15.0045 | ns |
| T _{PERIOD} | Spread Enabled 3V66 Period | Measurement at 1.5V | 14.9955 | 15.0799 | ns |
| T _{HIGH} | 3V66 High Time | Measurement at 2.0V | 4.9500 | – | ns |
| T _{LOW} | 3V66 Low Time | Measurement at 0.8V | 4.5500 | – | ns |
| T _R / T _F | 3V66 Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| T _{SKEW} | Any 3V66 to Any 3V66 Clock Skew | Measurement at 1.5V | – | 250 | ps |
| T _{CCJ} | 3V66 Cycle to Cycle Jitter | Measurement at 1.5V | – | 250 | ps |
| PCI/PCIF | | | | | |
| T _{DC} | PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.9910 | 30.0009 | ns |
| T _{PERIOD} | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 29.9910 | 30.1598 | ns |
| T _{HIGH} | PCIF and PCI high time | Measurement at 2.0V | 12.0 | – | ns |
| T _{LOW} | PCIF and PCI low time | Measurement at 0.8V | 12.0 | – | ns |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------------------|-------------------------------------|--|---------|---------|------|
| T _R / T _F | PCIF and PCI rise and fall times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| T _{SKREW} | Any PCI clock to Any PCI clock Skew | Measurement at 1.5V | – | 500 | ps |
| T _{CCJ} | PCIF and PCI Cycle to Cycle Jitter | Measurement at 1.5V | – | 250 | ps |
| DOT | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Period | Measurement at 1.5V | 20.8271 | 20.8396 | ns |
| T _{SKREW} | Any 48-MHz to 48-MHz Clock Skew | Measured at crossing point V _{OX} | – | 500 | ps |
| T _{HIGH} | USB high time | Measurement at 2.0V | 8.994 | 10.486 | ns |
| T _{LOW} | USB low time | Measurement at 0.8V | 8.794 | 10.386 | ns |
| T _R / T _F | Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 1.0 | ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| USB | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Period | Measurement at 1.5V | 20.8271 | 20.8396 | ns |
| T _{SKREW} | Any 48-MHz to 48-MHz Clock Skew | Measured at crossing point V _{OX} | – | 500 | ps |
| T _{HIGH} | USB high time | Measurement at 2.0V | 8.094 | 10.036 | ns |
| T _{LOW} | USB low time | Measurement at 0.8V | 7.694 | 9.836 | ns |
| T _R / T _F | Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 2.0 | ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| REF | | | | | |
| T _{DC} | REF Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | REF Period | Measurement at 1.5V | 69.827 | 69.855 | ns |
| T _{SKREW} | Any REF to REF Clock Skew | Measured at crossing point V _{OX} | – | 500 | ps |
| T _R / T _F | REF Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| T _{CCJ} | REF Cycle to Cycle Jitter | Measurement at 1.5V | – | 1000 | ps |
| ENABLE/DISABLE and SET-UP | | | | | |
| T _{STABLE} | Clock Stabilization from Power-up | | – | 1.8 | ms |
| T _{SS} | Stopclock Set-up Time | | 10.0 | – | ns |
| T _{SH} | Stopclock Hold Time | | 0 | – | ns |

Table 7. Group Timing Relationship and Tolerances

| Group | Conditions | Offset | |
|-------------|----------------|--------|--------|
| | | Min. | Max. |
| 3V66 to PCI | 3V66 Leads PCI | 1.5 ns | 3.5 ns |

Table 8. USB to DOT Phase Offset

| Parameter | Typical | Value | Tolerance |
|-----------|---------|--------|-----------|
| DOT Skew | 0° | 0.0 ns | 1000 ps |
| USB Skew | 180° | 0.0 ns | 1000 ps |
| VCH Skew | 0° | 0.0 ns | 1000 ps |

Table 9. Maximum Lumped Capacitive Output Loads

| Clock | Max Load | Unit |
|-------------|----------|------|
| PCI Clocks | 30 | pF |
| 3V66 Clocks | 30 | pF |
| USB Clock | 20 | pF |
| DOT Clock | 10 | pF |
| REF Clock | 30 | pF |

Test and Measurement Set-up

For Differential CPU and SRC Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

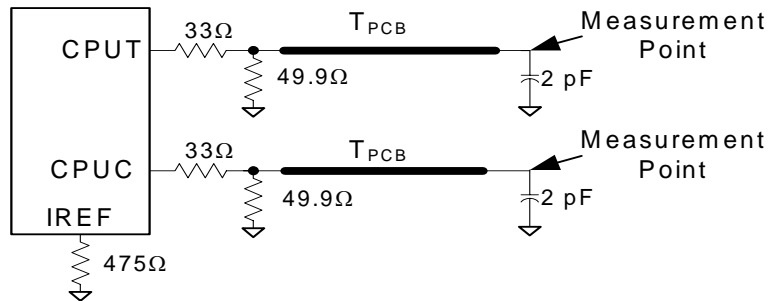


Figure 11. 0.7V Load Configuration

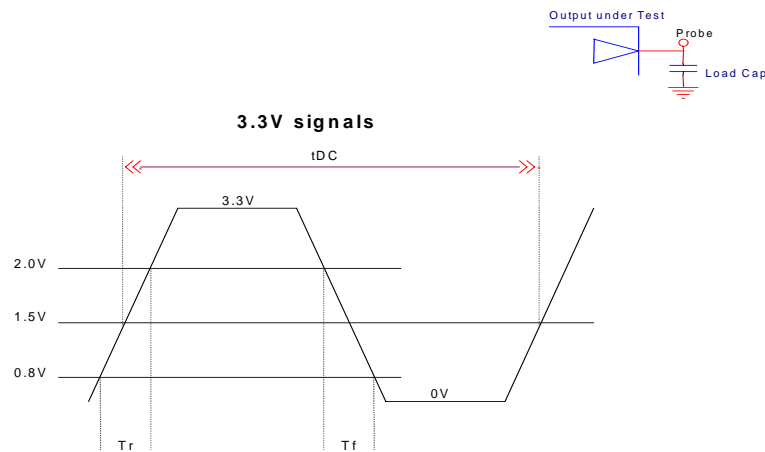


Figure 12. Lumped Load For Single-ended Output Signals (for AC Parameters Measurement)

Table 10.CPU Clock Current Select Function

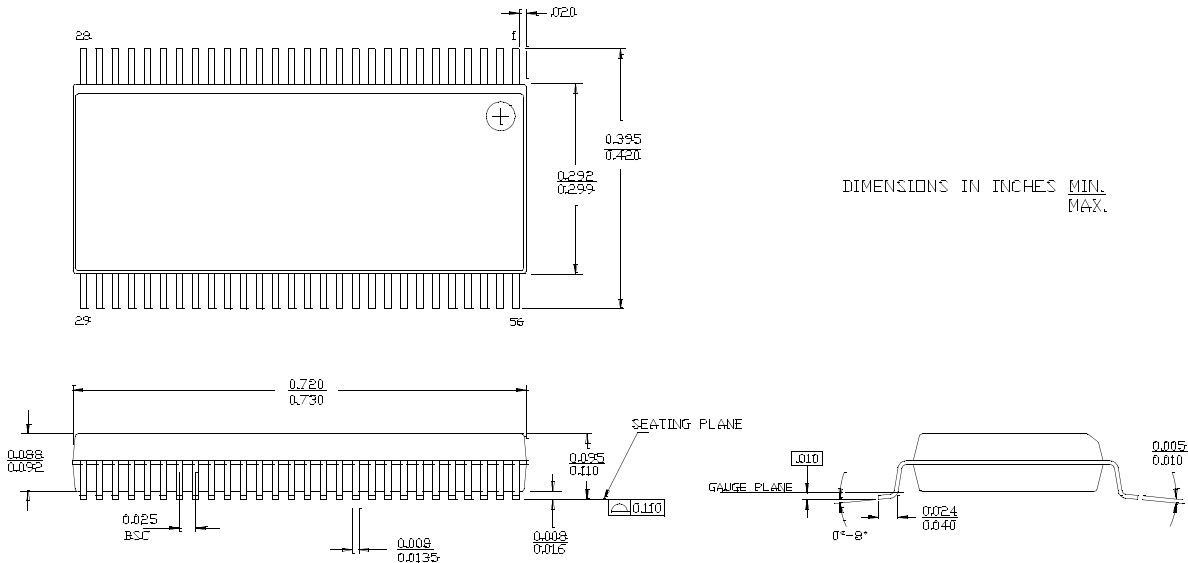
| Board Target Trace/Term Z | Reference R, I _{REF} – V _{DD} (3*R _{REF}) | Output Current | V _{oh} @ Z |
|---------------------------|---|--------------------------------------|---------------------|
| 50 Ohms | R _{REF} = 475 1%, I _{REF} = 2.32 mA | I _{OH} = 6*I _{REF} | 0.7V @ 50 |

Ordering Information

| Part Number | Package Type | Product Flow |
|----------------|------------------------------|------------------------|
| CY28409OC | 56-pin SSOP | Commercial, 0° to 70°C |
| CY28409OCT | 56-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |
| CY28409ZC | 56-pin TSSOP | Commercial, 0° to 70°C |
| CY28409ZCT | 56-pin TSSOP – Tape and Reel | Commercial, 0° to 70°C |
| PB-Free | | |
| CY28409OXC | 56-pin SSOP | Commercial, 0° to 70°C |
| CY28409OCXT | 56-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |
| CY28409ZXC | 56-pin TSSOP | Commercial, 0° to 70°C |
| CY28409ZXCT | 56-pin TSSOP – Tape and Reel | Commercial, 0° to 70°C |

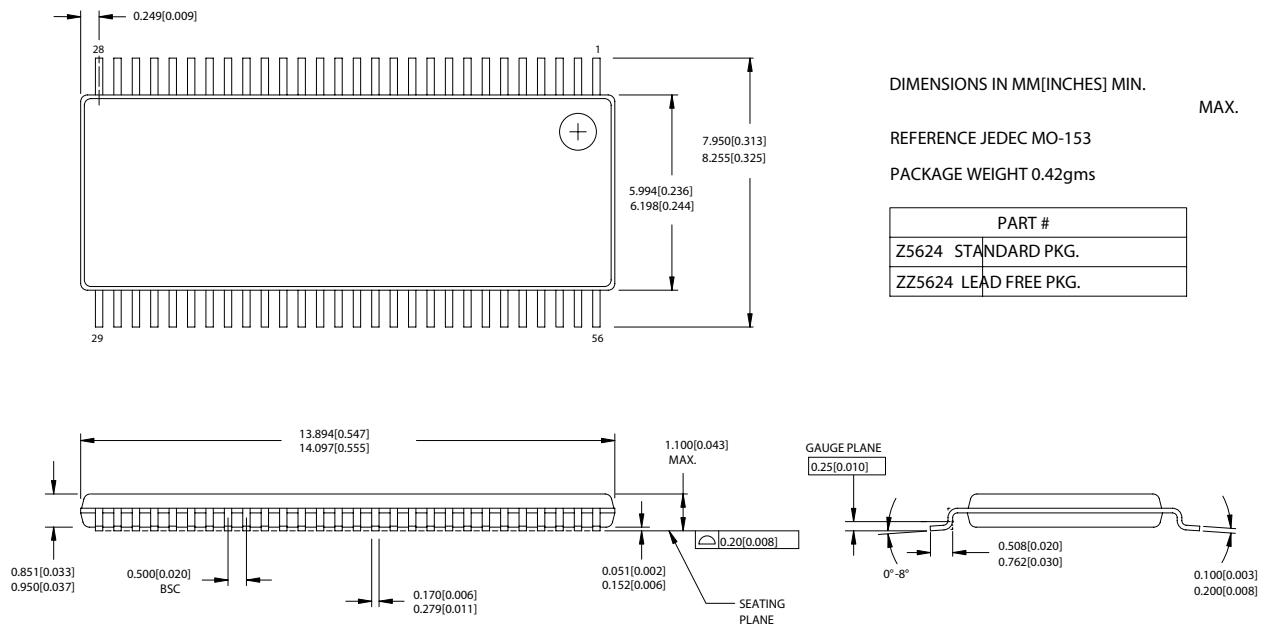
Package Drawings and Dimensions

56-lead Shrunk Small Outline Package O56



51-85062-°C

56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



51-85060-°C

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Document History Page

| Document Title: CY28409 Clock Synthesizer with Differential SRC and CPU Outputs | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-07445 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 121414 | 12/04/02 | RGL | New Data Sheet |
| *A | 124795 | 07/07/03 | RGL | Changed revision code to 4 Corrected rise/fall time value on DOT from 1.0/2.0 to 0.5/1.0 ns, respectively Changed USB and DOT from long-term jitter to cycle-to-cycle jitter Changed USB and DOT period value from 28.8257/28.8340 to 20.8271/20.8396 ns, respectively |
| *B | 128864 | 08/29/03 | RGL | Fixed the I ² C registers to match the actual device Removed all items referencing to 166 MHz |
| *C | 340360 | See ECN | RGL | Changed Byte 6 Bit 3 to Reserve |
| *D | 417655 | See ECN | RGL | Added Lead-free devices |