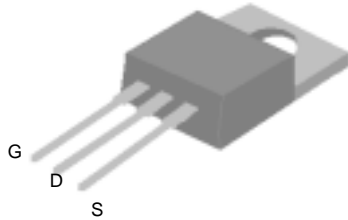


# N-channel Enhancement-mode Power MOSFET

## PRODUCT SUMMARY

$BV_{DSS}$	650V
$R_{DS(ON)}$	2.4Ω
$I_D$	4A

 **Pb-free; RoHS-compliant TO-220**



TO-220 (suffix P)

## DESCRIPTION

The SSM04N70BGP-A achieves fast switching performance with low gate charge without a complex drive circuit. It is suitable for high voltage applications such as AC/DC converters, SMPS and general off-line switching circuits.

The SSM04N70BGP-A is in TO-220 for through-hole mounting where a small footprint is required on the board, and/or an external heatsink is to be attached.

These devices are manufactured with an advanced process, providing improved on-resistance and switching performance.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	±30	V
$I_D$	Continuous drain current, $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	4	A
		2.5	A
$I_{DM}$	Pulsed drain current <sup>1</sup>	15	A
$P_D$	Total power dissipation, $T_C = 25^\circ\text{C}$	62.5	W
	Linear derating factor	0.5	W/°C
$E_{AS}$	Single pulse avalanche energy <sup>3</sup>	100	mJ
$I_{AR}$	Avalanche current	4	A
$E_{AR}$	Repetitive avalanche energy	4	mJ
$T_{STG}$	Storage temperature range	-55 to 150	°C
$T_J$	Operating junction temperature range	-55 to 150	°C

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Maximum thermal resistance, junction-case	2	°C/W
$R_{\theta JA}$	Maximum thermal resistance, junction-ambient	62	°C/W

### Notes:

1. Pulse width must be limited to avoid exceeding the safe operating area.
2. Pulse width <300us, duty cycle <2%.
3. Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 50\text{V}$ ,  $L = 25\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 4\text{A}$ .

**ELECTRICAL CHARACTERISTICS** (at  $T_j = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-source breakdown voltage	$V_{GS}=0V, I_D=1mA$	650	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown voltage temperature coefficient	Reference to $25^\circ\text{C}$ , $I_D=1mA$	-	0.6	-	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static drain-source on-resistance	$V_{GS}=10V, I_D=2A$	-	-	2.4	$\Omega$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
$g_{fs}$	Forward transconductance	$V_{DS}=20V, I_D=1A$	-	2.5	-	S
$I_{DSS}$	Drain-source leakage current	$V_{DS}=600V, V_{GS}=0V$ $V_{DS}=480V, V_{GS}=0V, T_j = 150^\circ\text{C}$	-	-	10 100	$\mu A$ $\mu A$
$I_{GSS}$	Gate-source leakage current	$V_{GS}=\pm 30V$	-	-	$\pm 100$	nA
$Q_g$	Total gate charge <sup>2</sup>	$I_D=4A$	-	16.7	-	nC
$Q_{gs}$	Gate-source charge	$V_{DS}=480V$	-	4.1	-	nC
$Q_{gd}$	Gate-drain ("Miller") charge	$V_{GS}=10V$	-	4.9	-	nC
$t_{d(on)}$	Turn-on delay time <sup>2</sup>	$V_{DS}=300V$	-	11	-	ns
$t_r$	Rise time	$I_D=4A$	-	8.3	-	ns
$t_{d(off)}$	Turn-off delay time	$R_G=10\Omega, V_{GS}=10V$	-	23.8	-	ns
$t_f$	Fall time	$R_D=75\Omega$	-	8.2	-	ns
$C_{iss}$	Input capacitance	$V_{GS}=0V$	-	950	-	pF
$C_{oss}$	Output capacitance	$V_{DS}=25V$	-	65	-	pF
$C_{rss}$	Reverse transfer capacitance	$f=1.0MHz$	-	6	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward voltage <sup>2</sup>	$I_S=4A, V_{GS}=0V$	-	-	1.5	V
$I_S$	Continuous source current (body diode)	$V_D=V_G=0V, V_S=1.3V$	-	-	4	A
$I_{SM}$	Pulsed source current (body diode) <sup>1</sup>		-	-	15	A

**Notes:**

1. Pulse width must be limited to avoid exceeding the maximum junction temperature of  $150^\circ\text{C}$ .

2. Pulse width  $<300\mu s$ , duty cycle  $<2\%$ .

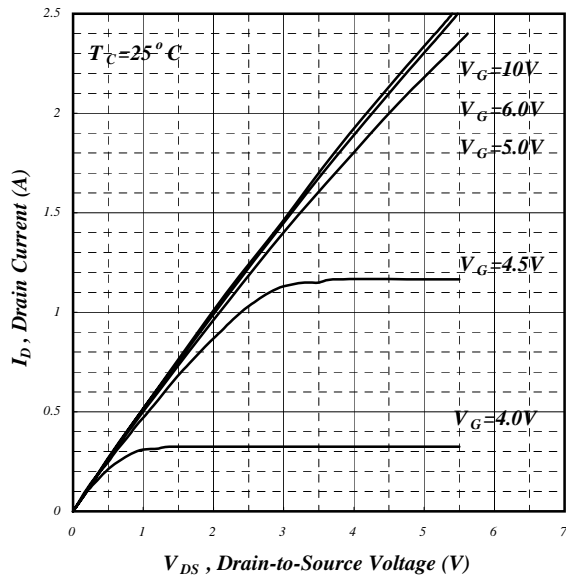


Fig 1. Typical Output Characteristics

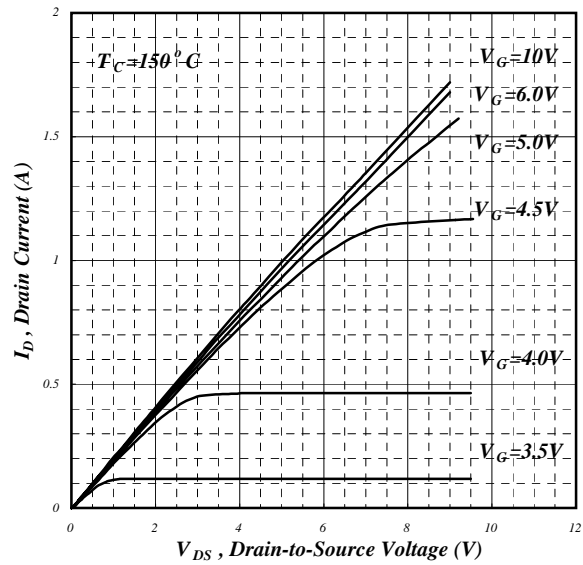


Fig 2. Typical Output Characteristics

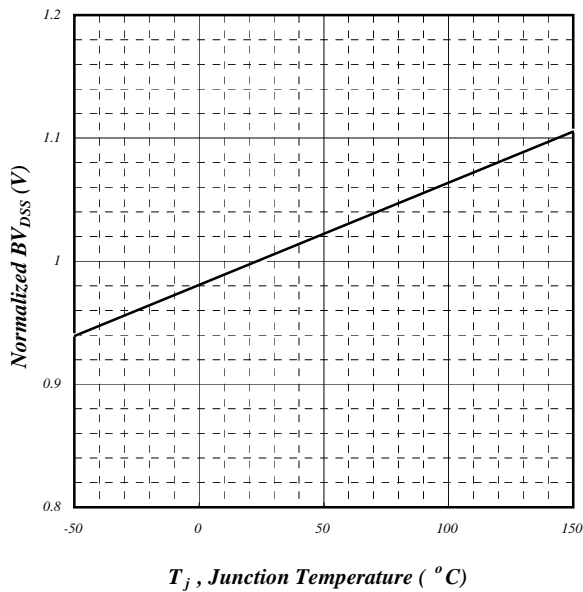


Fig 3. Normalized BVDSS vs. Junction Temperature

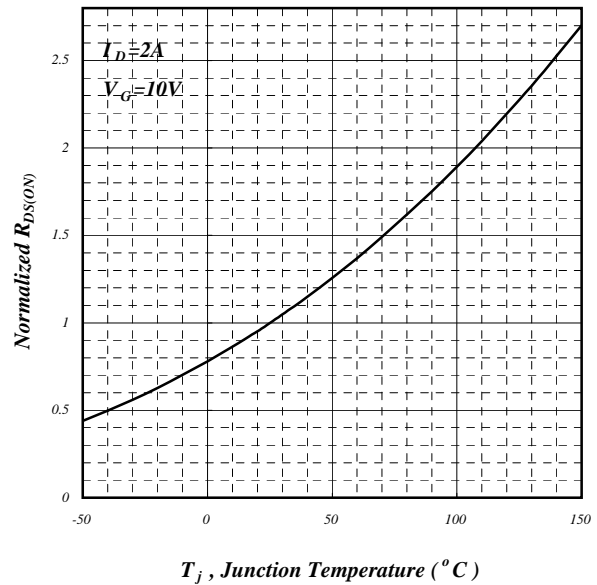


Fig 4. Normalized On-Resistance vs. Junction Temperature

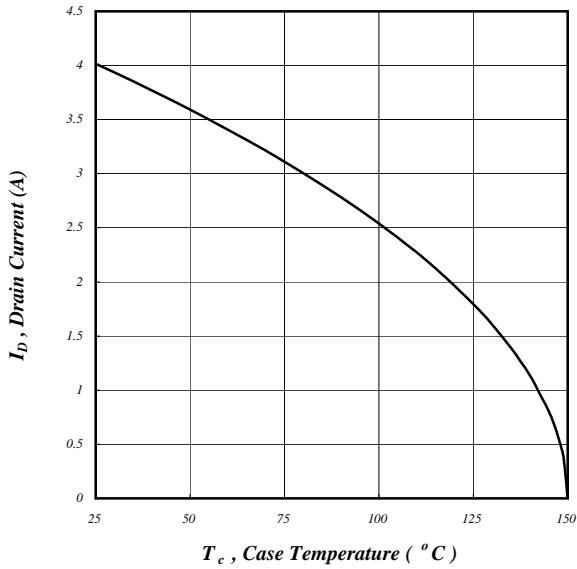


Fig 5. Maximum Drain Current vs. Case Temperature

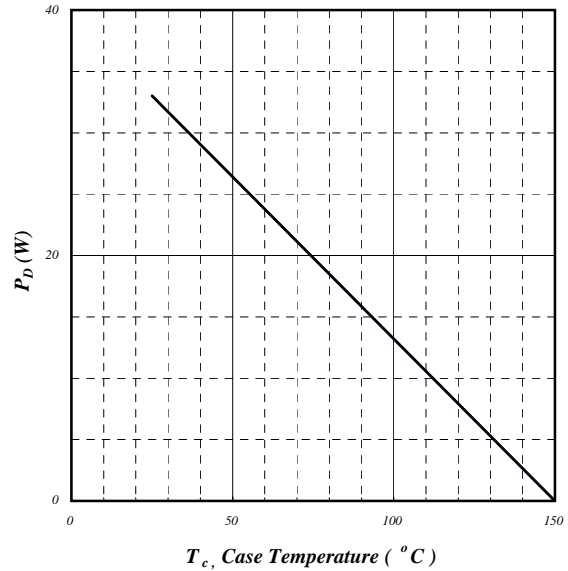


Fig 6. Typical Power Dissipation

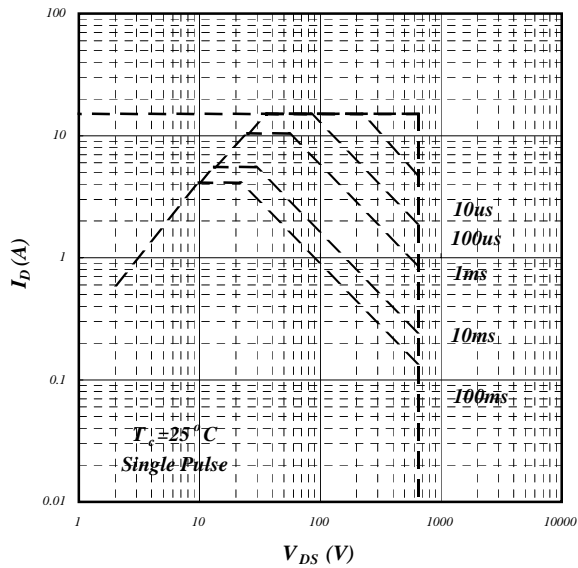


Fig 7. Maximum Safe Operating Area

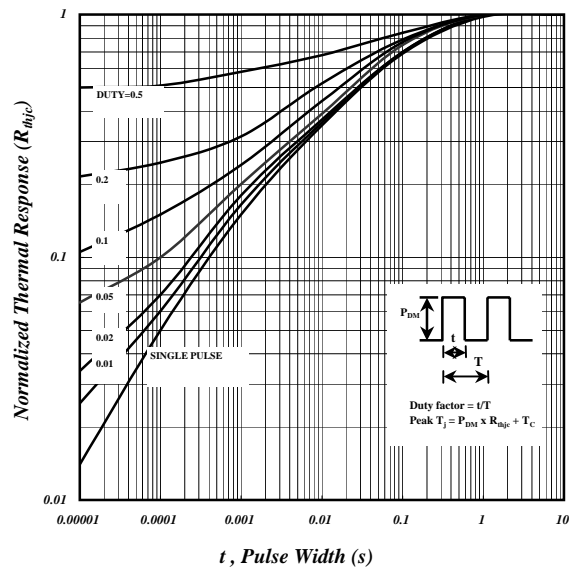


Fig 8. Effective Transient Thermal Impedance

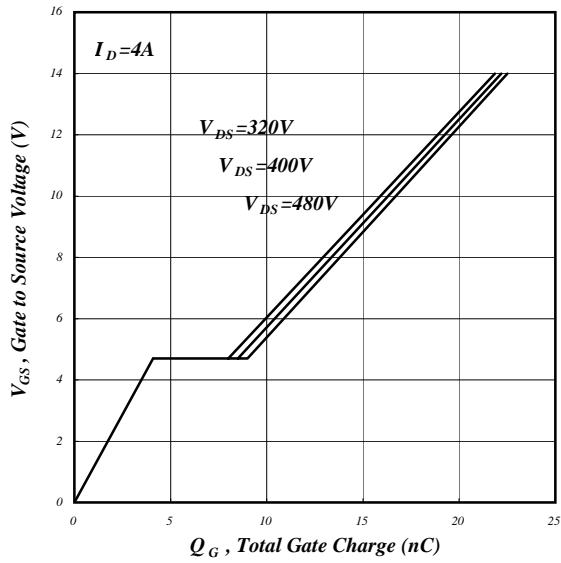


Fig 9. Gate Charge Characteristics

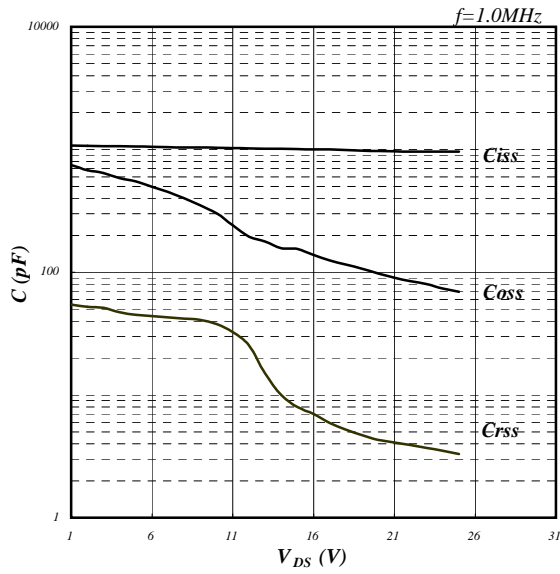


Fig 10. Typical Capacitance Characteristics

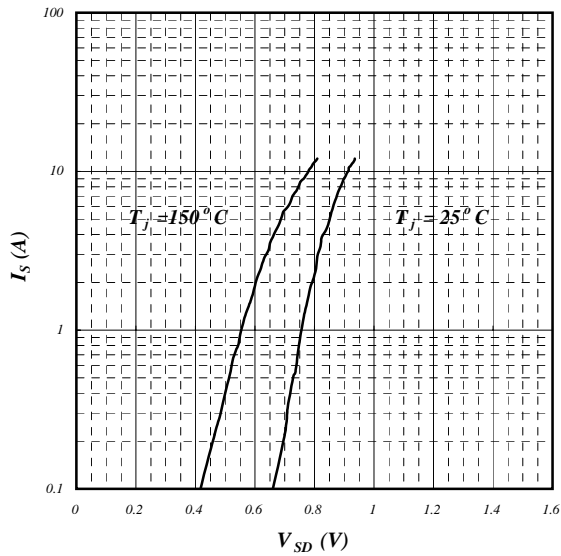


Fig 11. Forward Characteristic of Reverse Diode

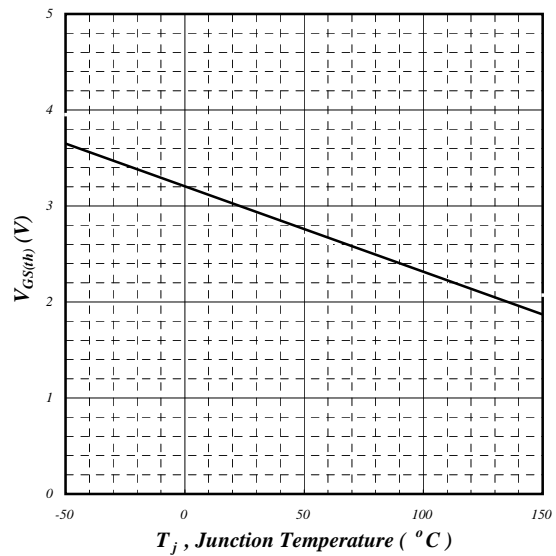


Fig 12. Gate Threshold Voltage vs. Junction Temperature

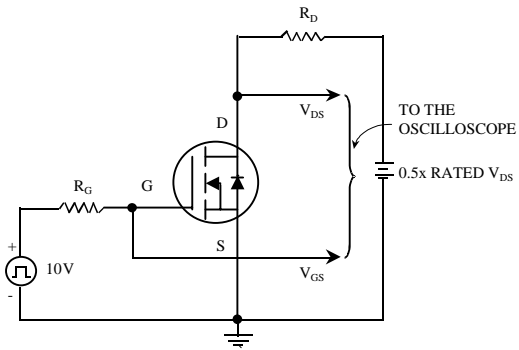


Fig 13. Switching Time Circuit

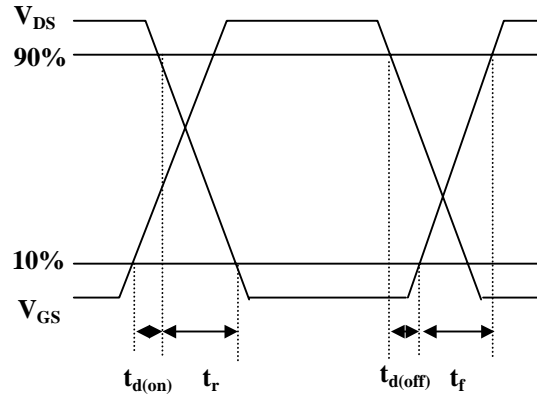


Fig 14. Switching Time Waveform

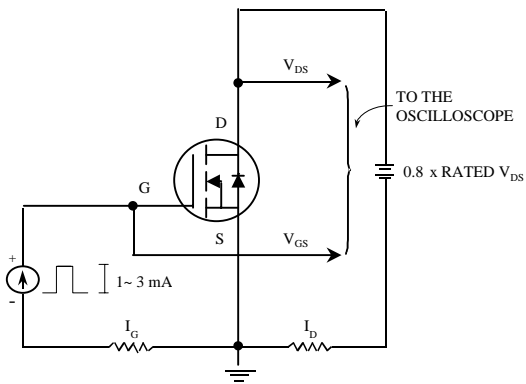


Fig 15. Gate Charge Circuit

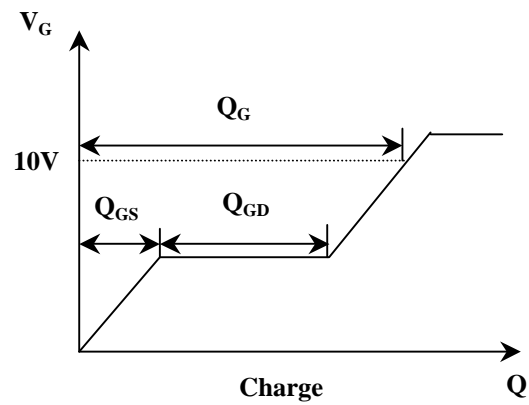
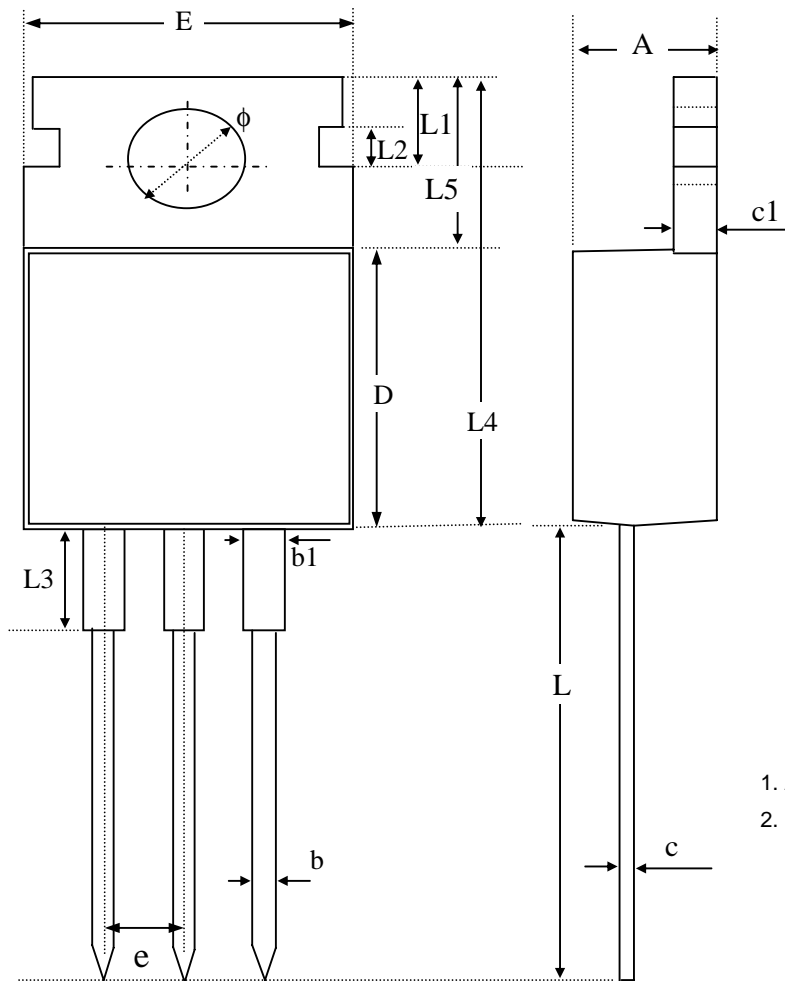


Fig 16. Gate Charge Waveform

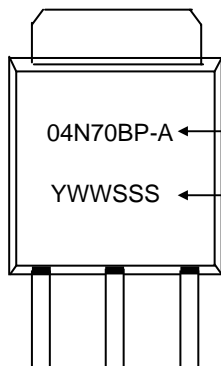
## PHYSICAL DIMENSIONS - TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.25	4.48	4.70
b	0.65	0.80	0.90
b1	1.15	1.38	1.60
c	0.40	0.50	0.60
c1	1.00	1.20	1.40
E	9.70	10.00	10.40
e	----	2.54	----
L	12.70	13.60	14.50
L1	2.60	2.80	3.00
L2	1.00	1.40	1.80
L3	2.6	3.10	3.6
L4	14.70	15.50	16
L5	6.30	6.50	6.70
φ	3.50	3.60	3.70
D	8.40	8.90	9.40

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

## PART MARKING - TO-220



04N70BP-A

YWSSS

PART NUMBER: 04N70BGP-A = SSM04N70BGP-A

DATE/LOT CODE:

Y = last digit of the year

WW = work week (01 -> 52)

SSS = lot code sequence

## PACKING: Moisture sensitivity level MSL3

1000pcs in tubes packed inside a moisture barrier bag (MBB).

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