ARIZONA MICROTEK, INC.

AZP94

ECL/PECL ÷1, ÷2 Clock Generation Chip with Tristate Compatible Outputs

FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Package Available
- 3.0V to 5.5V Operation
- Selectable Divide Ratio
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Tristate Compatible Outputs
- Input Buffer Powers Down when Disabled
- Selectable Input Biasing
- High Bandwidth for ≥1GHz
- Available in a MLP 8 (2x2) Package
- S Parameter and IBIS Model Files Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZP94NAG	J4G <Date Code>	1,2

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" for year followed by "WW" for week.

DESCRIPTION

The AZP94 is a specialized ÷1 or ÷2 clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the AZP94 functions as a standard receiver. If DIV-SEL is connected to V_{EE}, it functions as a ÷2 divider.

Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC), V_{EE}, or connected to V_{EE} via a 20kΩ ± 20% resistor. Leaving EN-SEL open or connecting it to V_{EE} allows the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75kΩ pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to V_{EE}, an internal 75kΩ pull-down resistor is selected which disables the outputs whenever EN is left open.

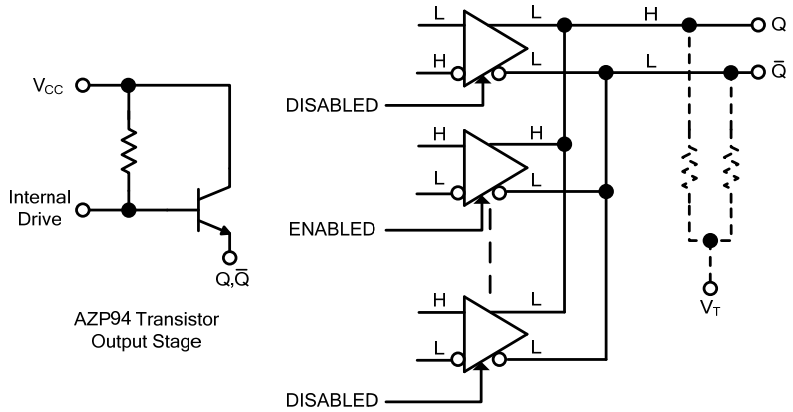
Connecting the EN-SEL to V_{EE} with a 20kΩ resistor will allow the EN pin/pad to function as an active low PECL/ECL enable with an internal 75kΩ pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). The default logic condition can be overridden by connecting the EN to V_{CC} with an external resistor of ≤20kΩ. If the enable signal is CMOS (rail-to-rail) and the logic sense is active low (EN-SEL connected to V_{EE} with a 20kΩ resistor), the EN pin/pad voltage swing must be reduced using two external resistors. Contact the factory for details.

When the AZP94 is disabled, the Q and $\overline{Q}$ outputs are forced LOW and the input buffer is powered down to minimize feed through. This feature allows tristate compatible parallel output connections. Multiple AZP94 chip outputs can be wired together. Since both outputs are forced LOW in the disable mode, an enabled AZP94 can drive the output lines without interference from the unselected units. In addition, the AZP94 can be used in parallel connection with PECL/ECL parts whose outputs are high impedance when disabled.

The EN pin/pad also functions as a reset when the ÷2 mode is selected. In the ÷2 mode, the counter resets when the outputs are disabled.

MLP 8, 2x2 mm Package (AZP94NA)

The AZP94NA provides a V_{BB} with an 1880Ω internal bias resistor from D to V_{BB}. This feature allows AC coupling with minimal external components. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground or V_{CC} with a 0.01 μF capacitor.



TYPICAL TRISTATE COMPATIBLE OPERATION

Tristate Compatible Operation

The outputs of the AZP94 are emitter followers as shown in the left side of the drawing. When a part is disabled, both outputs are set in the LOW state. This allows a HIGH output from an enabled part to override a disabled output and pull the combined line HIGH as seen in the right hand side of the drawing. When the enabled part output is LOW, the combined line remains LOW.

If all connected AZP94 parts are disabled, both output lines will be in the LOW state.

NOTE: The specifications in the ECL/PECL tables are valid when thermal equilibrium has been established.

SIGNAL DESCRIPTION

PIN/PAD	FUNCTION
D	Data Input
Q/$\overline{Q}$	Data Outputs
V_{BB}/$\overline{D}$	Reference Voltage Output
BIAS	Input Bias Return
EN	Enable/Reset Input
EN-SEL	Enable Logic Select
DIV-SEL	Divide Ratio Select
V_{EE}	Negative Supply
V_{CC}	Positive Supply

ENABLE TRUTH TABLE

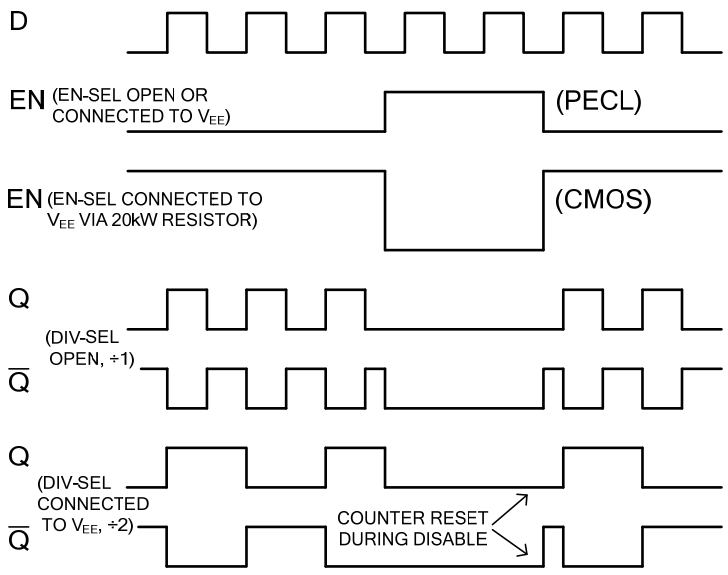
EN-SEL	EN	Q	$\overline{Q}$
NC	CMOS Low or V_{EE}[1]	Low	Low
NC	CMOS High, V_{CC} or NC	Data	Data
V_{EE}	CMOS Low, V_{EE} or NC[1]	Low	Low
V_{EE}	CMOS High or V_{CC}	Data	Data
20kΩ to V_{EE}	PECL Low, V_{EE} or NC[1]	Data	Data
20kΩ to V_{EE}	PECL High or V_{CC}	Low	Low

[1] Counter Reset for ÷2 Ratio

DIVIDE TRUTH TABLE

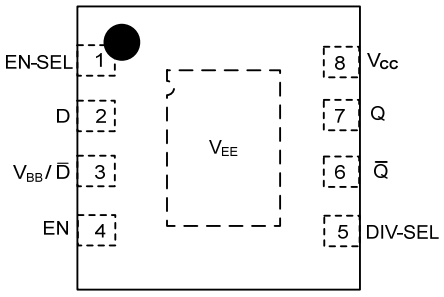
DIV-SEL	DIVIDE RATIO
NC	÷1
V_{EE}[1]	÷2

[1] DIV-SEL connection must be ≤1Ω.

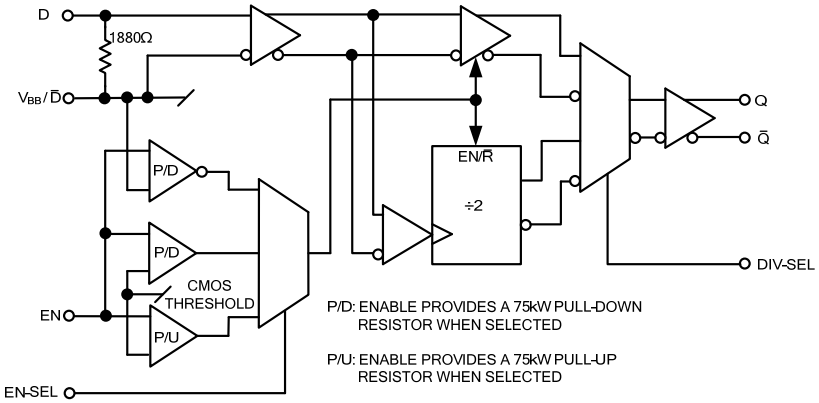


TIMING DIAGRAM

AZP94NA
MLP 8, 2x2 mm



TOP VIEW



Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic		Rating	Unit
V_{CC}	PECL Power Supply	(V_{EE} = 0V)	0 to +6.0	Vdc
V_I	PECL Input Voltage	(V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply	(V_{CC} = 0V)	-6.0 to 0	Vdc
V_I	ECL Input Voltage	(V_{CC} = 0V)	-6.0 to 0	Vdc
I_{HGOUT}	Output Current	— Continuous — Surge	50 100	mA
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1]	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$, EN (ECL)[2] EN (CMOS)[3]	 -1165 V_{EE}+2000	 -740 V_{CC}	 -1165 V_{EE}+2000	 -740 V_{CC}	 -1165 V_{EE}+2000	 -740 V_{CC}	 -1165 V_{EE}+2000	 -740 V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$, EN (ECL)[2] EN (CMOS)[3]	 -1900 V_{EE}	 -1475 V_{EE} + 800	 -1900 V_{EE}	 -1475 V_{EE} + 800	 -1900 V_{EE}	 -1475 V_{EE} + 800	 -1900 V_{EE}	 -1475 V_{EE} + 800	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[2] EN (CMOS)[3]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[1]		34		34		34		37	mA

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
2. EN-SEL connected to V_{EE} through a 20kΩ resistor
3. EN-SEL connected V_{EE} or left open (NC)

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1400	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 2135 2000	 2560 V_{CC}	 2135 2000	 2560 V_{CC}	 2135 2000	 2560 V_{CC}	 2135 2000	 2560 V_{CC}	mV
V_{IL}	Input LOW Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 1400 GND	 1825 800	 1400 GND	 1825 800	 1400 GND	 1825 800	 1400 GND	 1825 800	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (PECL)[3] EN (CMOS)[4]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[2]		34		34		34		37	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL connected to V_{EE} through a 20kΩ resistor
4. EN-SEL connected V_{EE} or left open (NC)

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3100	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 3835 2000	 4260 V_{CC}	 3835 2000	 4260 V_{CC}	 3835 2000	 4260 V_{CC}	 3835 2000	 4260 V_{CC}	mV
V_{IL}	Input LOW Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 3100 GND	 3525 800	 3100 GND	 3525 800	 3100 GND	 3525 800	 3100 GND	 3525 800	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (PECL)[3] EN (CMOS)[4]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[2]		34		34		34		37	mA

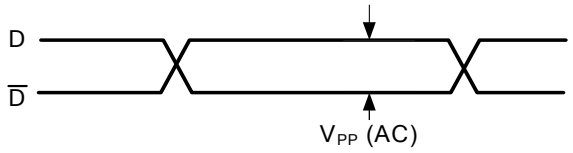
1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL connected to V_{EE} through a 20kΩ resistor
4. EN-SEL connected V_{EE} or left open (NC)

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC} = GND or V_{EE} = GND; V_{CC} = +3.0V to +5.5V)

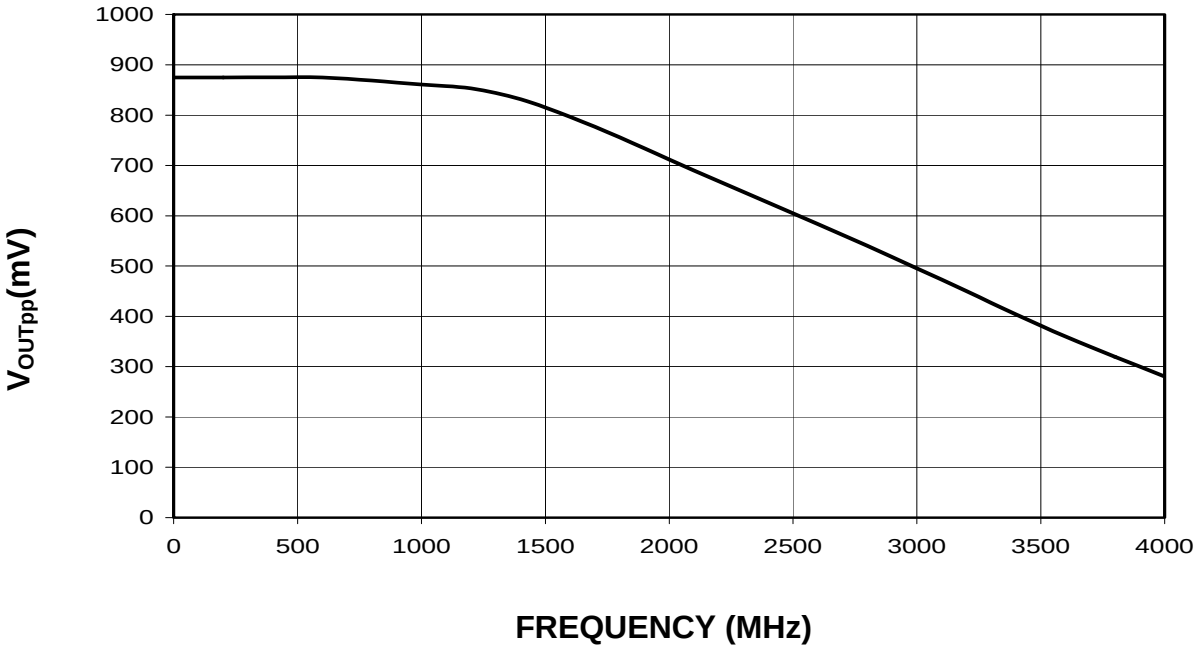
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay D to Q/$\overline{Q}$ Outputs[1] (SE) EN to Q/$\overline{Q}$ Outputs[1,2]			 450 3000			 450 3000			 450 3000			 450 3000	ps
t_{SKEW}	Duty Cycle Skew[3] (SE)		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Differential Input Swing[4]	150		1000	150		1000	150		1000	150		1000	mV
t_r / t_f	Output Rise/Fall[1] (20% - 80%)	100		240	100		240	100		240	100		240	ps

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
2. Specified from 50% EN input edge to V_{OH} min or V_{OL} max of the Q/$\overline{Q}$ outputs
3. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
4. The peak-to-peak differential input swing is the range for which AC parameters are guaranteed. The device has a voltage gain of ≈ 100.

AC PP INPUT

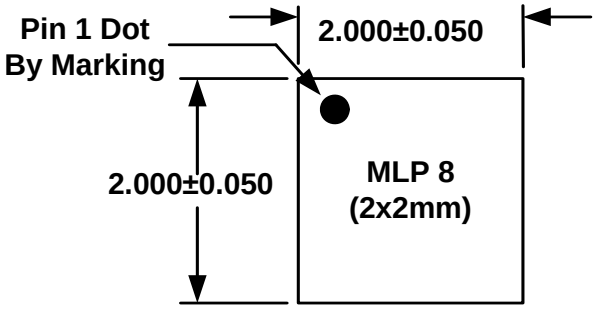


Typical Large Signal Outputs, Q/$\overline{Q}$

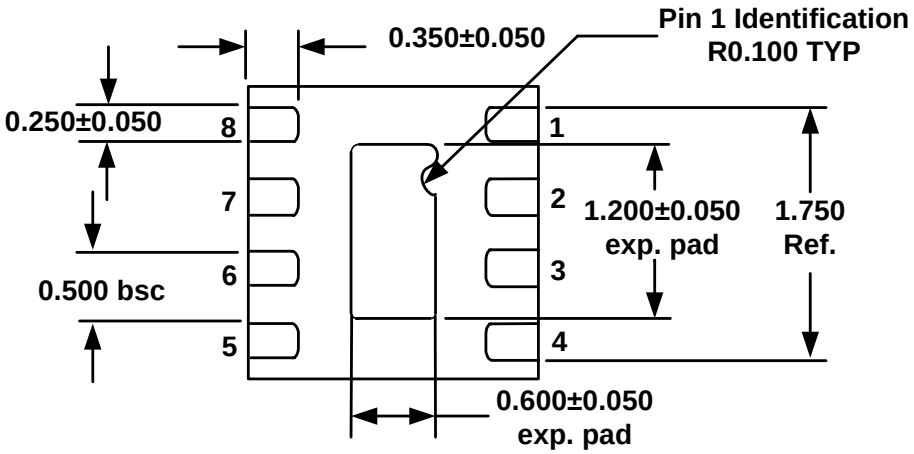


Measured with 750mv D input, Q/$\overline{Q}$ each terminated to V_{CC}-2V via 50 Ω resistors.

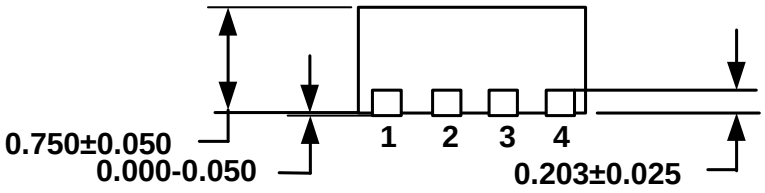
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



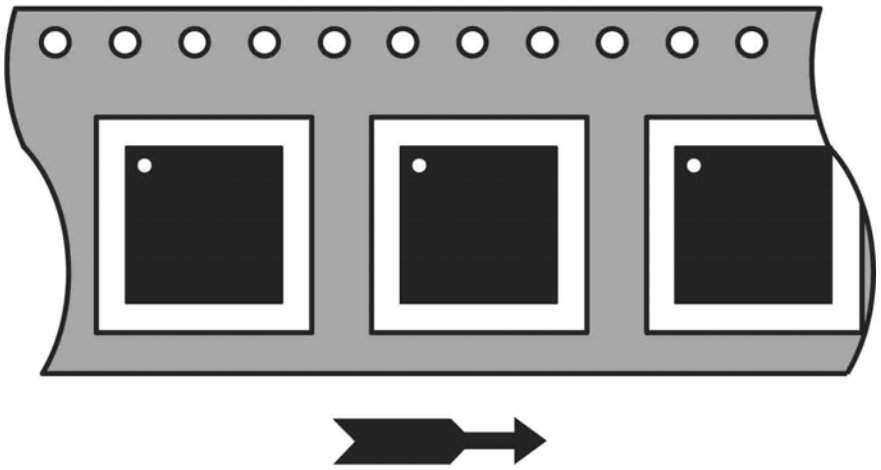
BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm

TAPE & REEL PACKAGING
MLP 8 2x2mm



Direction of Travel

Package	Suffix	Reel Diameter	Quantity	Carrier Tape Width	Carrier Tape Pitch
MLP 8 (2x2mm)	R1	7”	1000	8mm	4mm
	R2	13”	2500	8mm	4mm