

## SM77D Series 3.3 V CMOS Clock Oscillators

Feb 2008

**Lead Free** 

- Pletronics' SM77D Series is a quartz crystal controlled precision square wave generator with a CMOS output.
- The SM77D series will directly interface TTL devices also.
- The package is designed for high density surface mount designs.
- This is a low cost mass produced oscillator.
- Tape and Reel or cut tape packaging is available.
- 70 to 180 MHz
- 5 x 7 mm LCC Ceramic Package
- Enable/Disable Function
- Disable function includes low standby power mode
- 3<sup>rd</sup> Overtone Crystals used
- Improved circuit to minimize oscillator issues such as multi-mode output signal.
- Low Jitter
- Capable of driving up to 50pF capacitive loads

**Pletronics Inc. certifies this device is in accordance with the  
RoHS 6/6 (2002/95/EC) and WEEE (2002/96/EC) directives.**

Pletronics Inc. guarantees the device does not contain the following:  
Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's  
Weight of the Device: 0.17 grams  
Moisture Sensitivity Level: 1 As defined in J-STD-020C  
Second Level Interconnect code: e4

### Absolute Maximum Ratings:

Parameter	Unit
V <sub>CC</sub> Supply Voltage	-0.5V to +7.0V
V <sub>i</sub> Input Voltage	-0.5V to V <sub>CC</sub> + 0.5V
V <sub>o</sub> Output Voltage	-0.5V to V <sub>CC</sub> + 0.5V

### Thermal Characteristics

The maximum die or junction temperature is 155°C  
The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

**Part Number:**

SM77	45	D	E	V	-125.0M	-XX	
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	<b>Packaging code or blank</b> T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel
	<b>Frequency in MHz</b>
	<b>Supply Voltage V<sub>CC</sub></b> V = 3.3V ± 10%
	<b>Optional Enhanced OTR</b> Blank = Temp. range -10 to +70°C E = Temp. range -40 to +85°C
	<b>Series Model</b>
	<b>Frequency Stability</b> 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm
	<b>Series Model</b>

**Part Marking:**

PLE SM77  
FF.FFF M  
• YMDXX

or

PLE SM77  
FF.FFF M  
• YYWWXX

or

7XYWWXX  
FF.FFF M  
• PLE XXX

**Marking Legend:**

PLE = Pletronics

FF.FFF M = Frequency in MHz

YYWW or YWW or YMD = Date of Manufacture (year and week, or year-month-day)

All other marking is internal factory codes

Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from the marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

**Codes for Date Code YMD**

Code	6	7	8	9	0	1	2
Year	2006	2007	2008	2009	2010	2011	2012

Code	A	B	C	D	E	F	G	H	J	K	L	M
Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

Code	1	2	3	4	5	6	7	8	9	A	B	C
Day	1	2	3	4	5	6	7	8	9	10	11	12
Code	D	E	F	G	H	J	K	L	M	N	P	R
Day	13	14	15	16	17	18	19	20	21	22	23	24
Code	T	U	V	W	X	Y	Z					
Day	25	26	27	28	29	30	31					

**Legacy Part Numbers:**

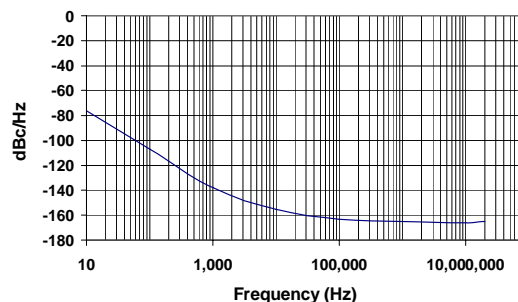
**'S'** Denoted Symmetry of 45%/55% at 50% of V<sub>CC</sub>. This is now the standard Duty Cycle and is no longer needed in the part number. We will still support part numbers with the 'S'. For example: SM7745DV and SM7745DSV describe the same specifications and can be used interchangeably by the customer.

**-30 or -50** Denoted Output Load other than the standard 15 pF. Data sheets now reflect the specifications at all available loads so this load designation is no longer needed. We will still support part numbers with this load designation.

**Electrical Specification for 3.30V  $\pm 10\%$  over the specified temperature range**

Item	Min	Max	Unit	Condition	
Frequency Range	70	180	MHz		
Frequency Accuracy	"45"	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures	
	"44"	+25			
	"20"	+20			
Output Waveform	CMOS				
Output High Level	90	-	%	of $V_{CC}$ (See load circuit)	
Output Low Level	-	10	%		
Output Symmetry	45	55	%	at 50% point of $V_{CC}$ (See load circuit)	
Jitter	-	0.6	pS RMS	12 KHz to 20 MHz from the output frequency	
	-	2.5	pS RMS	10 Hz to 1 MHz from the output frequency	
Enable/Disable Internal Pull-up	50	-	Kohm	to $V_{CC}$	
V disable	-	30	%	of $V_{CC}$ applied to pad 1	
V enable	70	-	%		
Output leakage	$V_{OUT} = V_{CC}$	-10	+10	uA	Pad 1 low, device disabled
	$V_{OUT} = 0V$	-10	+10		
Standby Current $I_{CC}$	-	3	uA		
Enable time	-	100	nS	Time for output to reach a logic state	
Disable time	-	100	nS	Time for output to reach a high Z state	
Start up time	-	10	mS	Time for output to reach specified frequency	
Operating Temperature Range	-10	+70	$^{\circ}C$	Standard Temperature Range	
	-40	+85	$^{\circ}C$	Extended Temperature Range "E" Option	
Storage Temperature Range	-55	+125	$^{\circ}C$		

Typical phase-noise characteristics at 106.25MHz

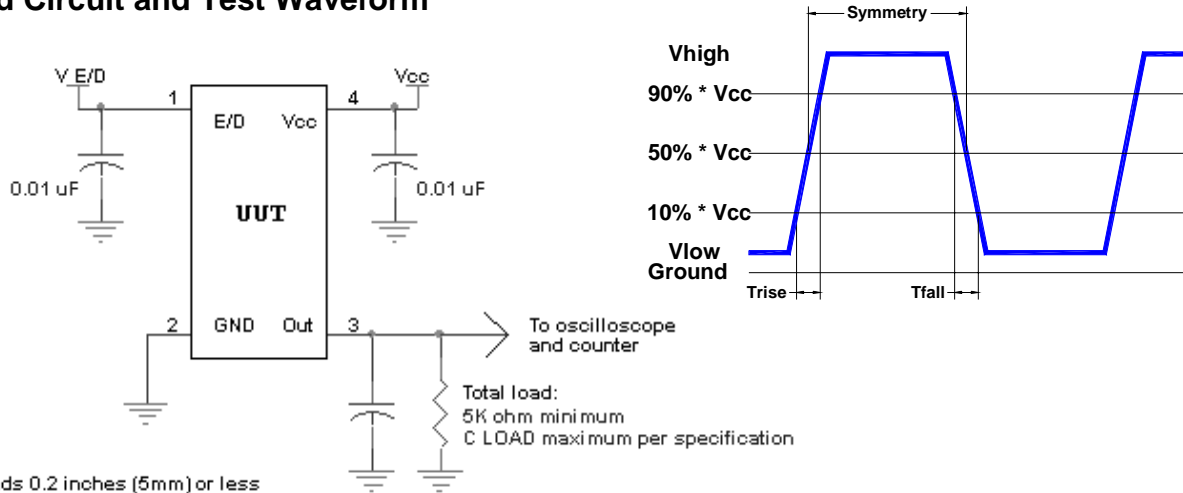


## Electrical Specification for 3.30V $\pm 10\%$ over the specified temperature range

Item	Min	Typ	Max	Unit	Condition	
V <sub>OUT</sub> High (V <sub>OH</sub> )	2.5	2.7	-	V	V <sub>CC</sub> = 2.97V, I <sub>OH</sub> = +8 mA	
V <sub>OUT</sub> Low (V <sub>OL</sub> )	-	0.3	0.4	V	V <sub>CC</sub> = 2.97V, I <sub>OL</sub> = -8 mA	
Output T <sub>RISE</sub> and T <sub>FALL</sub>	-	0.8	1.5	nS	>130 MHz	C <sub>LOAD</sub> = 15 pF 10% to 90% of V <sub>CC</sub> See Load Circuit
	-	1.0	2.0	nS	>110 MHz and $\leq$ 130 MHz	
	-	1.2	2.5	nS	>80 MHz and $\leq$ 110 MHz	
	-	2.0	3.0	nS	$\leq$ 80 MHz	
	-	1.2	2.0	nS	>130 MHz	C <sub>LOAD</sub> = 30 pF 10% to 90% of V <sub>CC</sub> See Load Circuit
	-	1.3	2.5	nS	>110 MHz and $\leq$ 130 MHz	
	-	1.4	3.0	nS	>80 MHz and $\leq$ 110 MHz	
	-	2.0	4.0	nS	$\leq$ 80 MHz	
	-	2.1	3.5	nS	>110 MHz and $\leq$ 130 MHz	C <sub>LOAD</sub> = 50 pF 10% to 90% of V <sub>CC</sub> See Load Circuit
	-	2.1	4.5	nS	>80 MHz and $\leq$ 110 MHz	
	-	3.0	5.0	nS	$\leq$ 80 MHz	
	V <sub>CC</sub> Supply Current (I <sub>CC</sub> )	-	30	70	mA	>130 MHz
-		25	60	mA	>110 MHz and $\leq$ 130 MHz	
-		20	50	mA	>80 MHz and $\leq$ 110 MHz	
-		18	40	mA	$\leq$ 80 MHz	
-		40	90	mA	>130 MHz	C <sub>LOAD</sub> = 30 pF
-		32	70	mA	>110 MHz and $\leq$ 130 MHz	
-		26	57	mA	>80 MHz and $\leq$ 110 MHz	
-		22	45	mA	$\leq$ 80 MHz	
-		44	80	mA	>110 MHz and $\leq$ 130 MHz	C <sub>LOAD</sub> = 50 pF
-		34	65	mA	>80 MHz and $\leq$ 110 MHz	
-		29	50	mA	$\leq$ 80 MHz	

Specifications with Pad 1 E/D open circuit

## Load Circuit and Test Waveform



## Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

## ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

## Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Courier New

Bar code is 39-Full ASCII

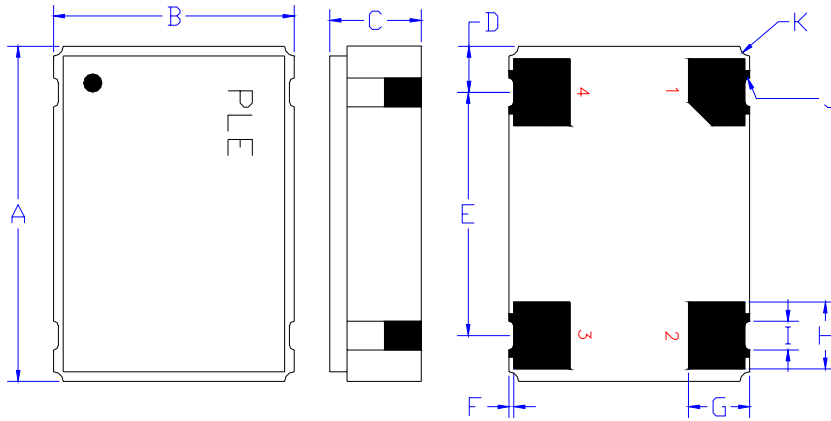
Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Arial

P/N:		
	SM7745DV-106.25M	
Customer P/N:		
	12345678	
Qty:		D/C 
	1000	75409MM

<p><b>RoHS Compliant</b></p> <p>2nd Lvl Interconnect</p> <p>Category=e4</p> <p>Max Safe Temp=260C for 10s 2X Max</p>
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## Mechanical:



	Inches	mm
A	0.276 $\pm$ 0.006	7.00 $\pm$ 0.15
B	0.197 $\pm$ 0.006	5.00 $\pm$ 0.15
C	0.068 $\pm$ 0.018	1.73 $\pm$ 0.44
D <sup>1</sup>	0.038	0.96
E <sup>1</sup>	0.200	5.08
F <sup>1</sup>	0.004	0.10
G <sup>1</sup>	0.050	1.27
H <sup>1</sup>	0.055	1.40
I <sup>1</sup>	0.024	0.60
J <sup>1</sup>	0.004	0.10R
K <sup>1</sup>	0.008	0.020R

Not to Scale

<sup>1</sup> Typical dimensions

### Contacts :

Gold 11.8 pinches 0.3  $\mu$ m minimum over Nickel 50 to 350 pinches 1.27 to 8.89  $\mu$ m

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is logic low the output will be inhibited (high impedance state.) Recommend connecting this pad to V <sub>CC</sub> if the oscillator is to be always on.
2	Ground (GND)	
3	Output	
4	Supply Voltage (V <sub>CC</sub> )	Recommend connecting appropriate power supply bypass capacitors as close as possible.

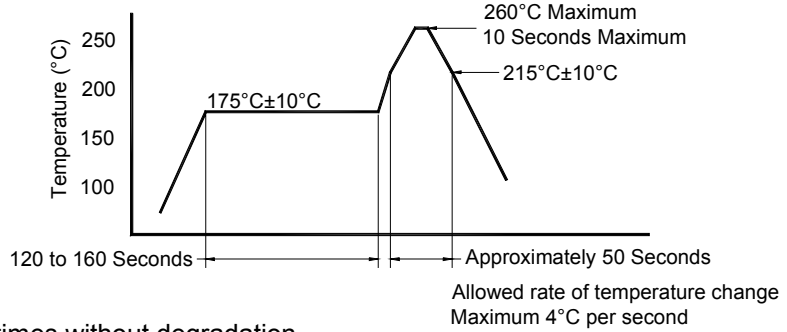
## Layout and application information

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.



## Reflow Cycle (typical for lead free processing)



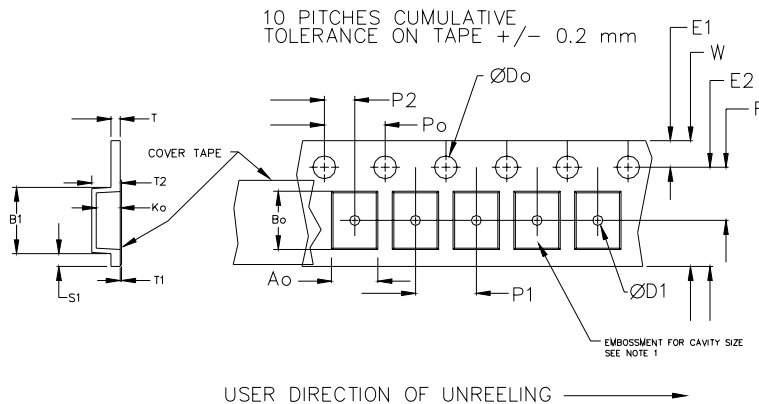
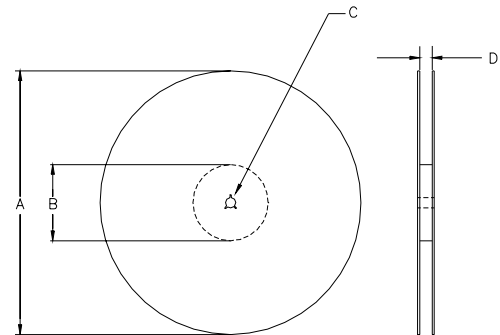
The part may be reflowed 2 times without degradation.

## Tape and Reel: available for quantities of 250 to 1000 per reel (< 250 = cut tape)

Constant Dimensions Table 1								
Tape Size	D0	D1 Min	E1	P0	P2	S1 Min	T Max	T1 Max
8mm	1.5	1.0	1.75	4.0	2.0 ±0.05	0.6	0.6	0.1
12mm		1.5			2.0 ±0.1			
16mm		+0.1 -0.0			1.5			
24mm		1.5			1.5			

Variable Dimensions Table 2							
Tape Size	B1 Max	E2 Min	F	P1	T2 Max	W Max	Ao, Bo & Ko
16 mm	12.1	14.25	7.5 ± 0.1	8.0 ± 0.1	8.0	16.3	Note 1

Note 1: Embossed cavity to conform to EIA-481-B      Dimensions in mm      Not to scale



		REEL DIMENSIONS			Tape Width
A	inches	7.0	10.0	13.0	
	mm	177.8	254.0	330.2	
B	inches	2.50	4.00	3.75	
	mm	63.5	101.6	95.3	
C	mm	13.0 +0.5 / -0.2			
D	mm	16.4 +2.0 -0.0	16.4 +2.0 -0.0	16.4 +2.0 -0.0	16.0

Reel dimensions may vary from the above



# SM77D Series 3.3 V CMOS Clock Oscillators

Feb 2008

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## IMPORTANT NOTICE

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