Low Frequency EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 20dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- Optimized for 10MHz to 35MHz input frequency range
- Internal loop filter minimizes external components and board space
- 4 selectable spread ranges
- SSON control pin for spread spectrum enable and disable options
- Low Cycle-to-cycle jitter
- Wide operating range (3V to 5V)
- 16mA output drives
- TTL or CMOS compatible outputs
- Low power CMOS design
- Available in 8 pin SOIC and TSSOP Packages

Product Description

The P2010A is a selectable spread spectrum frequency modulator designed specifically for PC peripheral and embedded controller markets. The P2010A reduces electromagnetic interference (EMI) at the clock source which provides system wide reduction of EMI of all clock dependent signals. The P2010A allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.
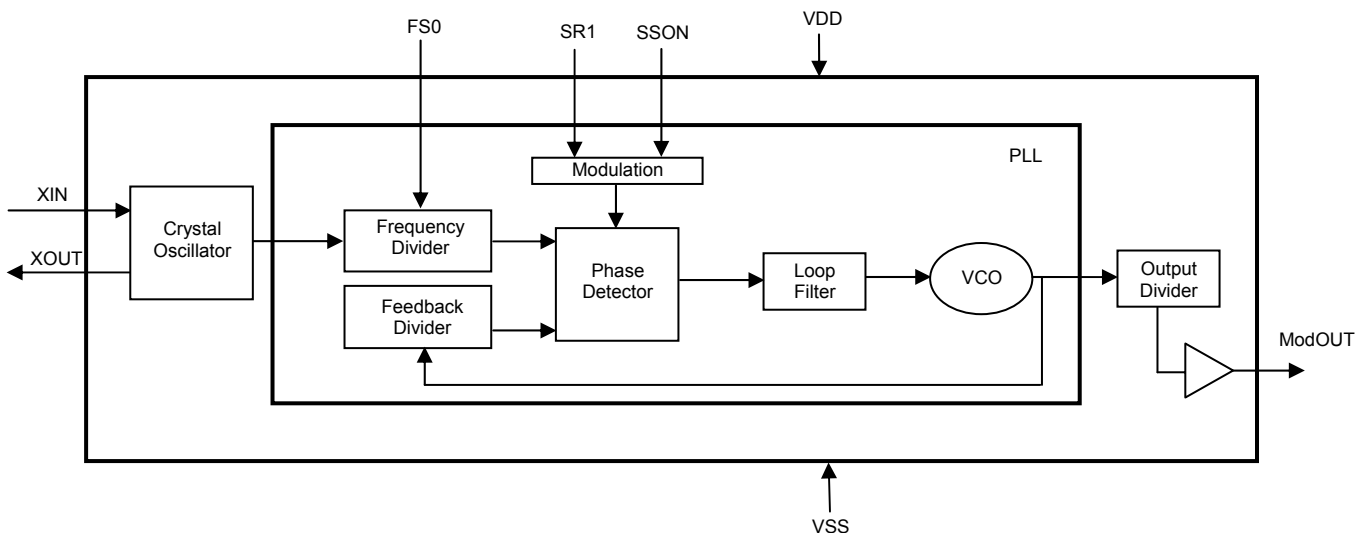
The P2010A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

The P2010A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called "spread spectrum clock generation".
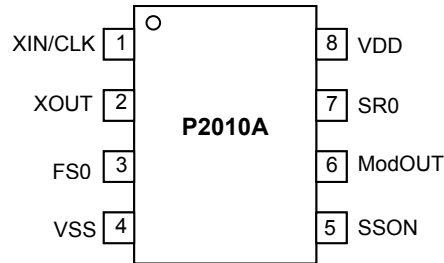
Applications

The P2010A is targeted towards the embedded controller market and PC peripheral markets including scanners, facsimile, MFP's, printers, PDA, IA, and GPS devices.

Block Diagram

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Pin Configuration

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           ┌─────○─────┐
XIN/CLK  1 │           │ 8  VDD
           │           │
  XOUT   2 │   P2010A  │ 7  SR0
           │           │
   FS0   3 │           │ 6  ModOUT
           │           │
   VSS   4 │           │ 5  SSON
           └───────────┘
```

Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLK	I	Connect to crystal or externally generated clock signal.
2	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.
3	FS0	I	Digital logic input used to select Input Frequency Range (see Table 1). This pin has an internal pull-up resistor.
4	VSS	P	Ground Connection. Connect to system ground.
5	SSON	I	Digital logic input used to enable Spread Spectrum function (Active Low). Spread Spectrum function enable when low. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread Spectrum Clock Output.
7	SR0	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
8	VDD	P	Connect to +3.3V or +5.0V

Table 1 - Spread Range Selection

FS0	SR0	Spreading Range	Input Frequency	Modulation rate
1	0	+/- 1.50%	10MHz to 20MHz	(Fin/10)*20.83KHz
1	1	+/- 2.50%	10MHz to 20MHz	(Fin/10)*20.83KHz
0	0	+/- 1.25%	20MHz to 35MHz	(Fin/10)*20.83KHz
0	1	+/- 2.00%	20MHz to 35MHz	(Fin/10)*20.83KHz

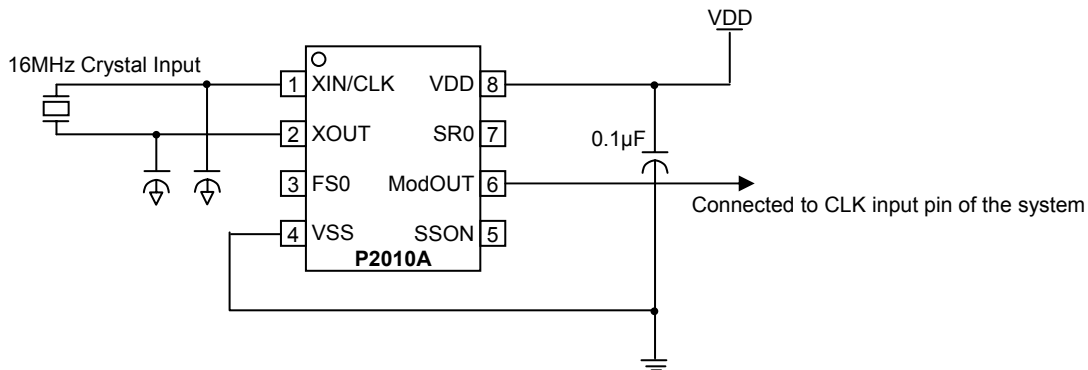**rev 0.2**

Spread Spectrum Selection

Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency
(Note: the center frequency is the frequency of the external reference input on XIN/CLK, Pin 1).

Example of a typical printer or scanner application that operates on a clock frequency of 16MHz:

A spreading selection of FS0=1 and SR0=1 provides a percentage deviation of +/-2.50%* (see Table 1) of Center Frequency. This results in the frequency on ModOUT being swept from 16.40MHz to 15.60MHz at a modulation rate of 33.33KHz (see Table 1). This particular example (see Figure below) given here is a common EMI reduction method for scanner, printer or embedded applications and has already been adopted by most of the leading manufacturers.

Note: Spreading range selection varies from different system manufacturers and their designs.

P2010A Application Schematic for Flat-Bed Scanner

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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +7	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	-40 to+85	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV
Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.			

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GND	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	VDD + 0.3	V
I_{IL}	Input Low Current (pull-up resistor on inputs SR0, FS0)	-	-	-35	μA
I_{IH}	Input High Current (pull-down resistor on input SSON)	-	-	35	μA
I_{XOL}	XOUT output low current (at 0.4V, VDD = 3.3V)	-	3	-	mA
I_{XOH}	XOUT output high current (at 2.5V, VDD = 3.3V)	-	3	-	mA
V_{OL}	Output Low Voltage (VDD=3.3V, I_{OL} = 20mA)	-	-	0.4	V
V_{OH}	Output High Voltage (VDD=3.3V, I_{OH} = 20mA)	2.5	-	-	V
I_{DD}	Static Supply Current	-	0.6	-	mA
I_{CC}	Dynamic Supply Current (3.3V and 15pF loading)	4	6	8	mA
VDD	Operating Voltage	2.7	3.3	5.5	V
t_{ON}	Power Up Time (First locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock Output Impedance		50		Ω

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency	10	20	35	MHz
t_{LH}*	Output rise time (Measured at 0.8V to 2.0V)	0.7	0.9	1.1	nS
t_{HL}*	Output fall time (Measured at 2.0V to 0.8V)	0.6	0.8	1.0	nS
t_{JC}	Jitter (Cycle to cycle)	-	-	360	pS
t_D	Output duty cycle	45	50	55	%
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

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Package Information

<div align="center">

8-lead (150-mil) SOIC Package

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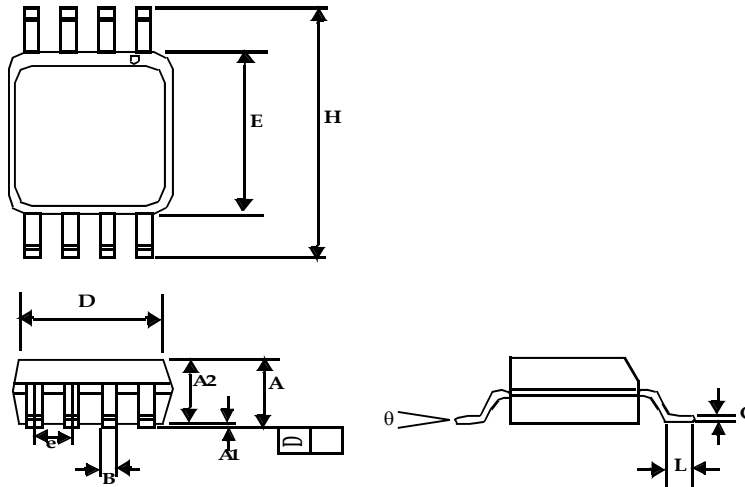
Symbol	Dimensions			
	Inches		Millimeters	
	Min	**Max**	**Min**	**Max**
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

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8-lead TSSOP (4.40-MM Body)
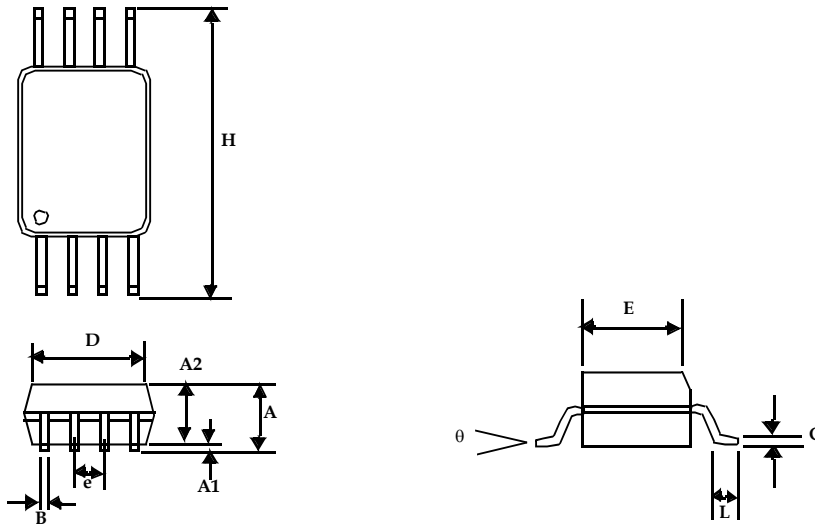
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

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Ordering Information

Part number	Marking	Package Type	Temperature
P2010AF-08ST	P2010AF	8-Pin SOIC, Tube, Pb Free	Commercial
P2010AF-08SR	P2010AF	8-Pin SOIC, Tape and Reel, Pb Free	Commercial
P2010AG-08ST	P2010AG	8-Pin SOIC, Tube, Green	Commercial
P2010AG-08SR	P2010AG	8-Pin SOIC, Tape and Reel, Green	Commercial
I2010AF-08ST	I2010AF	8-Pin SOIC, Tube, Pb Free	Industrial
I2010AF-08SR	I2010AF	8-Pin SOIC, Tape and Reel, Pb Free	Industrial
I2010AG-08ST	I2010AG	8-Pin SOIC, Tube, Green	Industrial
I2010AG-08SR	I2010AG	8-Pin SOIC, Tape and Reel, Green	Industrial
P2010AF-08TT	P2010AF	8-Pin TSSOP, Tube, Pb Free	Commercial
P2010AF-08TR	P2010AF	8-Pin TSSOP, Tape and Reel, Pb Free	Commercial
P2010AG-08TT	P2010AG	8-Pin TSSOP, Tube, Green	Commercial
P2010AG-08TR	P2010AG	8-Pin TSSOP, Tape and Reel, Green	Commercial
I2010AF-08TT	I2010AF	8-Pin TSSOP, Tube, Pb Free	Industrial
I2010AF-08TR	I2010AF	8-Pin TSSOP, Tape and Reel, Pb Free	Industrial
I2010AG-08TT	I2010AG	8-Pin TSSOP, Tube, Green	Industrial
I2010AG-08TR	I2010AG	8-Pin TSSOP, Tape and Reel, Green	Industrial

Device Ordering Information

P 2 0 1 0 A F - 0 8 - S T

SR - SOIC, T/R
TT – TSSOP, TUBE
TR - TSSOP, T/R
ST – SOIC. TUBE

PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE, LEAD FREE, and RoHS

Deviation (%) and Spread option Identifier

DEVICE NUMBER

P = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
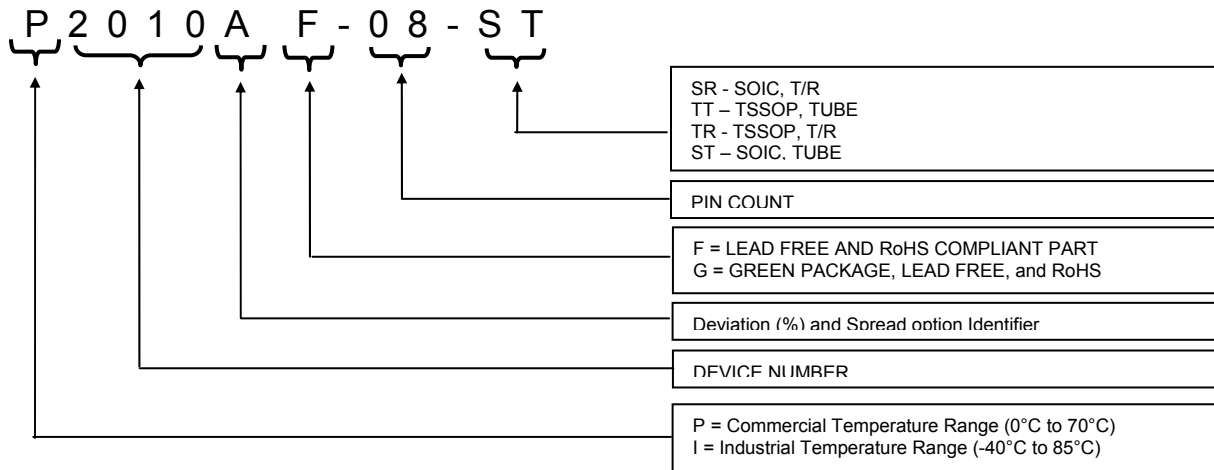
Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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