19-4144; Rev 1; 10/08

High-Voltage, Adjustable Sequencing/Supervisory Circuits

General Description

The MAX16052/MAX16053 are a family of small, low-power, high-voltage monitoring circuits with sequencing capability. These miniature devices offer very wide flexibility with an adjustable voltage threshold and an external capacitor-adjustable time delay. These devices are ideal for use in power-supply sequencing, reset sequencing, and power switching applications. Multiple devices can be cascaded for complex sequencing applications.

A high-impedance input (IN) with a 0.5V threshold allows an external resistive divider to set the monitored threshold. The output (OUT) asserts high when the input voltage rises above the 0.5V threshold and the enable input (EN) is asserted high. When the voltage at IN falls below 0.495V or when the enable input is deasserted (EN = low), the output deasserts (OUT = low). The MAX16052/MAX16053 provide a capacitor programmable delay time from when the voltage at IN rises above 0.5V to when the output is asserted.

The MAX16052 offers an active-high open-drain output while the MAX16053 offers an active-high push-pull output. Both devices operate from a 2.25V to 16V supply voltage and feature an active-high enable input. The MAX16052/MAX16053 are available in a tiny 6-pin SOT23 package and are fully specified over the automotive temperature range (-40°C to +125°C).

Applications

Automotive	Computers/Servers
Medical Equipment	Critical µP Monitoring
Intelligent Instruments	Set-Top Boxes
Portable Equipment	Telecom

Features

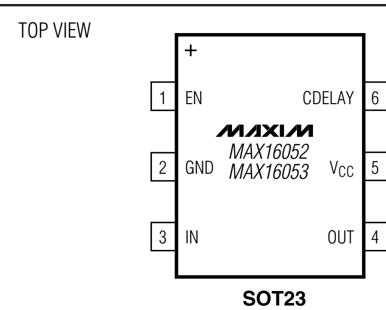
- ♦ **1.8% Accurate Adjustable Threshold Over Temperature**
- ♦ **Open-Drain (28V Tolerant) Output Allows Interfacing to 12V Intermediate Bus Voltage**
- ♦ **Operates from V_{CC} of 2.25V to 16V**
- ♦ **Low Supply Current (18µA typ)**
- ♦ **Capacitor-Adjustable Delay**
- ♦ **Active-High Logic-Enable Input**
- ♦ **Fully Specified from -40°C to +125°C**
- ♦ **Small 6-Pin SOT23 Package**

Ordering Information

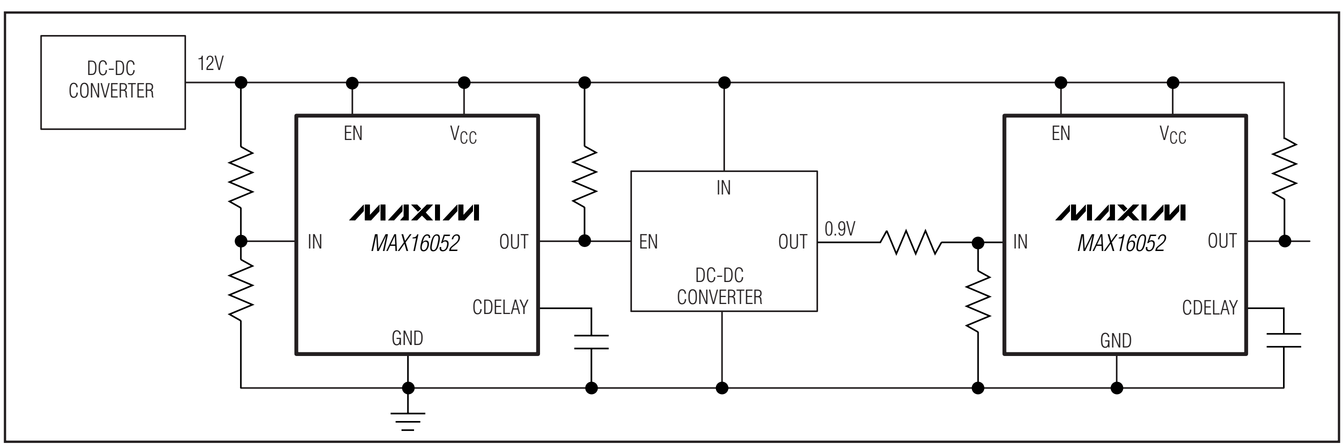
PART	OUTPUT	PIN-PACKAGE	TOP MARK
MAX16052AUT+T	Open-Drain	6 SOT23	+ACLW
MAX16053AUT+T	Push-Pull	6 SOT23	+ACLX

Note: *All devices operate over the -40°C to +125°C operating automotive temperature range.*
+Denotes a lead-free/RoHS-compliant package.
T = Tape and reel, offered in 2.5k increments.

Pin Configuration



Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Voltage, Adjustable Sequencing/Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} ....-0.3V to +30V
OUT (push-pull, MAX16053) ....-0.3V to (V_{CC} + 0.3V)
OUT (open-drain, MAX16052)..............................-0.3V to +30V
EN, IN ....-0.3V to (V_{CC} + 0.3V)
CDELAY..-0.3V to +6V
Input/Output Current (all pins)..±20mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C).........695.7mW
Operating Temperature Range ....-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.25V to 16V, V_{EN} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY							
Operating Voltage Range	V_{CC}			2.25		16	V
Undervoltage Lockout	UVLO	V_{CC} falling (Note 2)		1.8		2	V
V_{CC} Supply Current	I_{CC}	MAX16052, no load	V_{CC} = 3.3V		18	37	µA
			V_{CC} = 12V		23	45	
		MAX16053, no load	V_{CC} = 3.3V		22	47	
			V_{CC} = 12V		29	57	
IN							
Threshold Voltage	V_{TH}	V_{IN} rising, 2.25V ≤ V_{CC} ≤ 16V		0.491	0.500	0.509	V
Hysteresis	V_{HYST}	V_{IN} falling			5		mV
Input Current	I_{IN}	V_{IN} = 0 or 16V		-40	+5	+60	nA
CDELAY							
CDELAY Charge Current	I_{CD}	V_{CDELAY} = 0V		200	250	300	nA
CDELAY Threshold	V_{TCD}	V_{CDELAY} rising		0.95	1.00	1.05	V
CDELAY Pulldown Resistance	R_{CDELAY}	V_{CC} ≥ 2.25V, I_{SINK} = 200µA			15	60	Ω
		V_{CC} ≥ 3.3V, I_{SINK} = 1mA			15	60	
EN							
EN Low Voltage	V_{IL}					0.5	V
EN High Voltage	V_{IH}			1.4			V
EN Leakage Current	I_{LEAK}	V_{EN} = 0V or V_{CC}		-55	+15	+55	nA
OUT							
OUT Low Voltage (Open-Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90µA				0.2	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA				0.3	
		V_{CC} > 4.5V, I_{SINK} = 1mA				0.4	
OUT High Voltage (Push-Pull, MAX16053)	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 500µA		0.8 x V_{CC}			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA		0.9 x V_{CC}			
OUT Leakage Current (Open-Drain, MAX16052)	I_{LKG}	Output not asserted low, V_{OUT} = 28V				150	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.25V to 16V, V_{EN} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
IN to OUT Propagation Delay	t_{DELAY}	V_{CC} = 3.3V, V_{IN} rising, V_{IN} = V_{TH} + 25mV; MAX16052, 100kΩ pullup resistor, C_{CDELAY} = 0		30		µs
		V_{CC} = 3.3V, V_{IN} rising, V_{IN} = V_{TH} + 25mV; MAX16053, C_{CDELAY} = 0		30		µs
		V_{CC} = 3.3V, V_{IN} rising, V_{IN} = V_{TH} + 25mV; MAX16052, 100kΩ pullup resistor, C_{CDELAY} = 0.047µF		190		ms
		V_{CC} = 3.3V, V_{IN} rising, V_{IN} = V_{TH} + 25mV; MAX16053, C_{CDELAY} = 0.047µF		190		ms
		V_{CC} = 12V, V_{IN} rising, V_{IN} = V_{TH} + 25mV; MAX16052, 100kΩ pullup resistor, C_{CDELAY} = 0		30		µs
		V_{CC} = 12V, V_{IN} rising, V_{IN} = V_{TH} + 25mV; MAX16053, C_{CDELAY} = 0		30		µs
	t_{DL}	V_{CC} = 3.3V, V_{IN} falling, V_{IN} = V_{TH} - 30mV		18		µs
		V_{CC} = 12V, V_{IN} falling, V_{IN} = V_{TH} - 30mV		18		µs
Startup Delay (Note 3)		V_{CC} = 2.25V, V_{IN} = 0.525V, C_{CDELAY} = 0		0.5		ms
		V_{CC} = 12V, V_{IN} = 12V, C_{CDELAY} = 0		0.5		ms
EN Minimum Input Pulse Width	t_{MPW}		1			µs
EN Glitch Rejection				100		ns
EN to OUT Delay	t_{OFF}	From device enabled to device disabled; MAX16052, 100kΩ pullup resistor; V_{CC} = 3.3V		250		ns
		From device enabled to device disabled; MAX16052, 100kΩ pullup resistor; V_{CC} = 12V		300		ns
		From device enabled to device disabled; MAX16053; V_{CC} = 3.3V		350		ns
		From device enabled to device disabled; MAX16053; V_{CC} = 12V		400		ns
EN to OUT Delay	t_{PROP}	From device disabled to device enabled; MAX16052, 100kΩ pullup resistor, C_{CDELAY} = 0; V_{CC} = 3.3V		14		µs
		From device disabled to device enabled; MAX16052, 100kΩ pullup resistor, C_{CDELAY} = 0; V_{CC} = 12V		14		µs
		From device disabled to device enabled; MAX16053, C_{CDELAY} = 0; V_{CC} = 3.3V		14		µs
		From device disabled to device enabled; MAX16053, C_{CDELAY} = 0; V_{CC} = 12V		14		µs
		From device disabled to device enabled; MAX16052, 100kΩ pullup resistor, C_{CDELAY} = 0.047µF		190		ms
		From device disabled to device enabled; MAX16053, C_{CDELAY} = 0.047µF		190		ms

Note 1: All devices are production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: When V_{CC} falls below the UVLO threshold, the outputs deassert (OUT goes low). When V_{CC} falls below 1.2V, the output state cannot be determined.
Note 3: During the initial power-up, V_{CC} must exceed 2.25V for at least 0.5ms before OUT can go high.

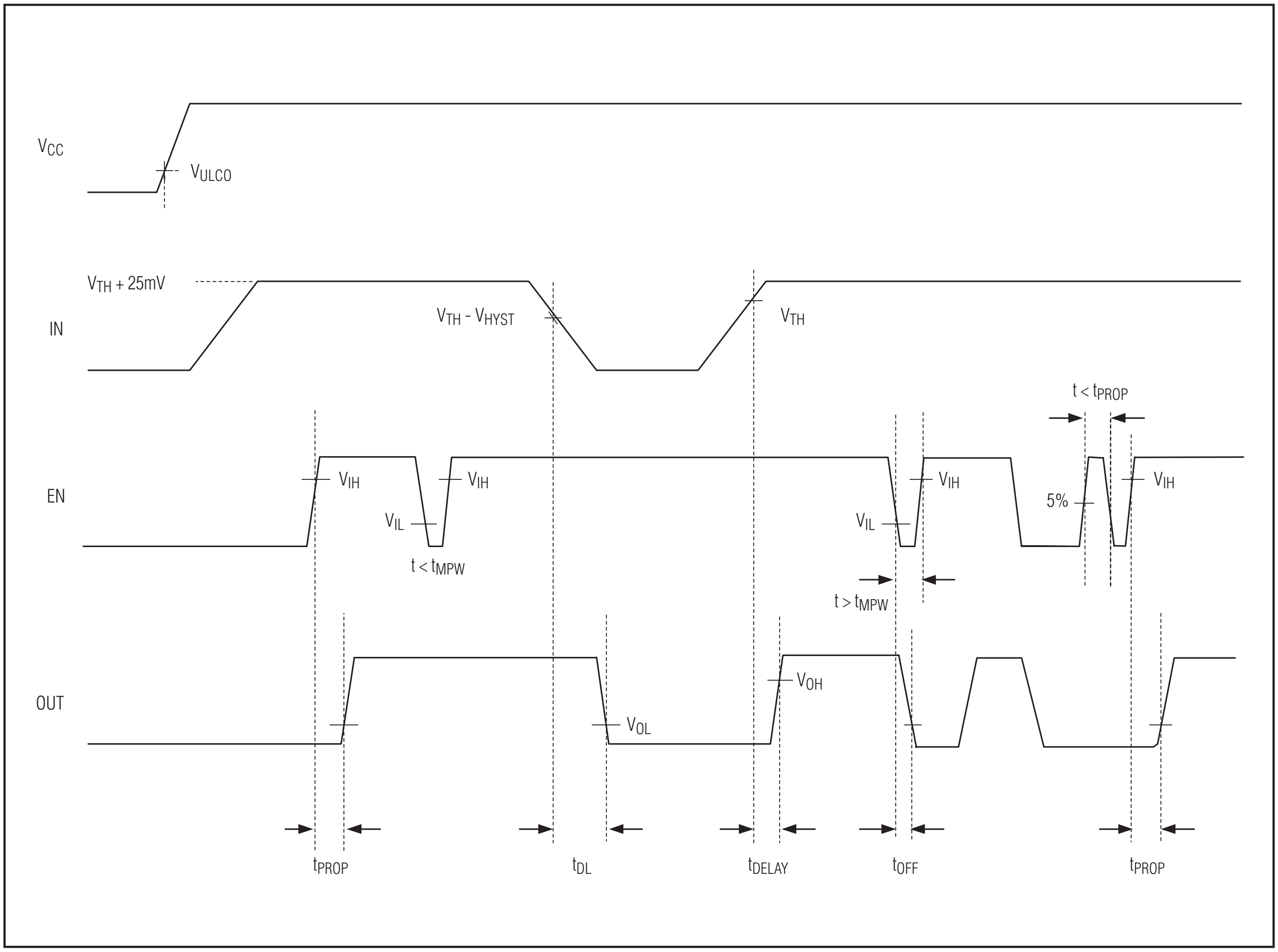
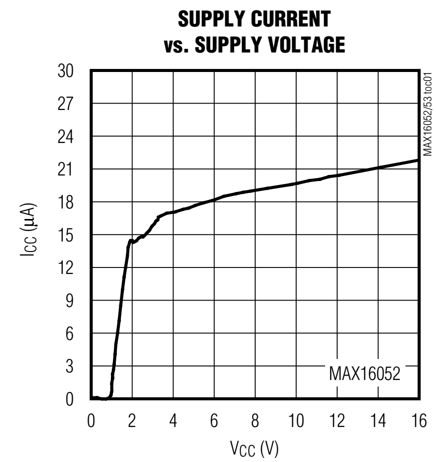
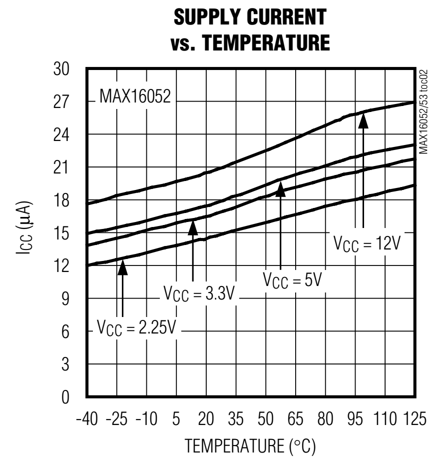


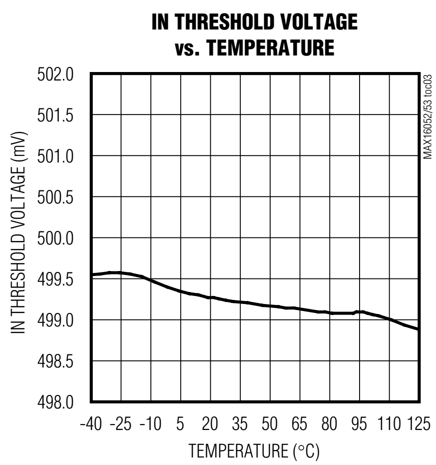
Figure 1. MAX16052/MAX16053 Timing Diagram (C_{CDELAY} = 0)

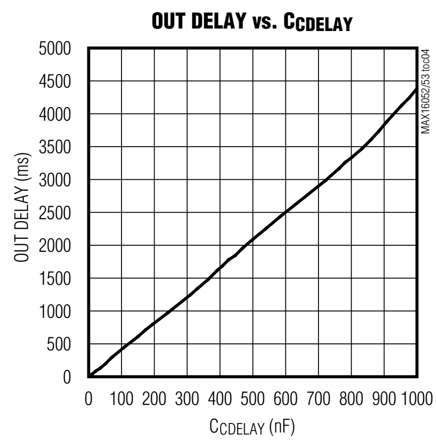
Typical Operating Characteristics

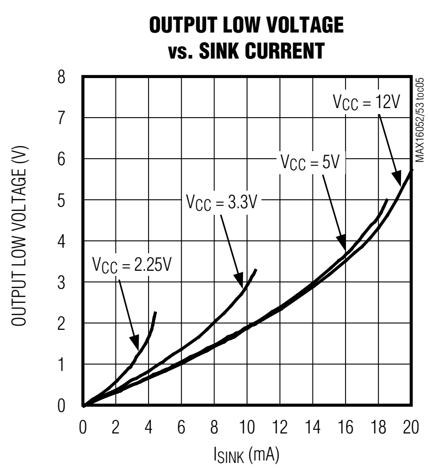
(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)

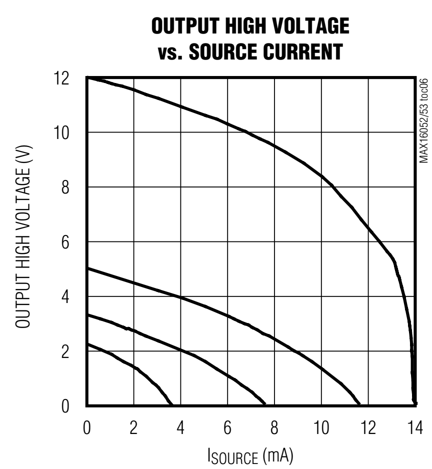








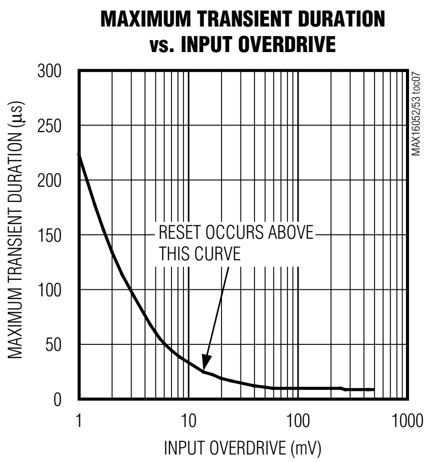


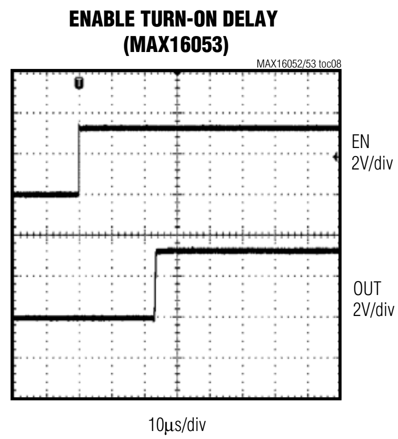


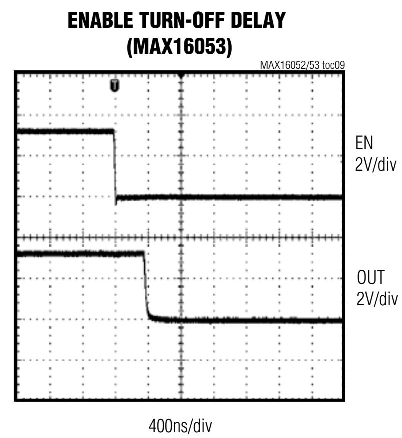
High-Voltage, Adjustable Sequencing/Supervisory Circuits

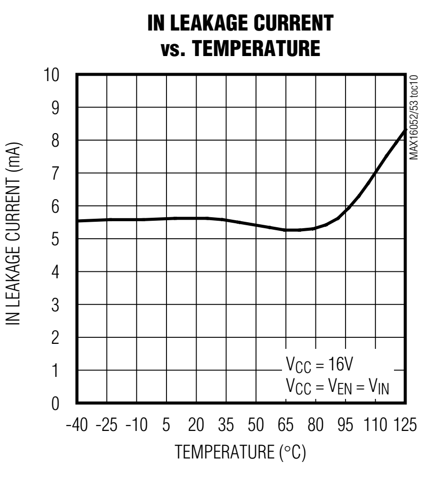
Typical Operating Characteristics

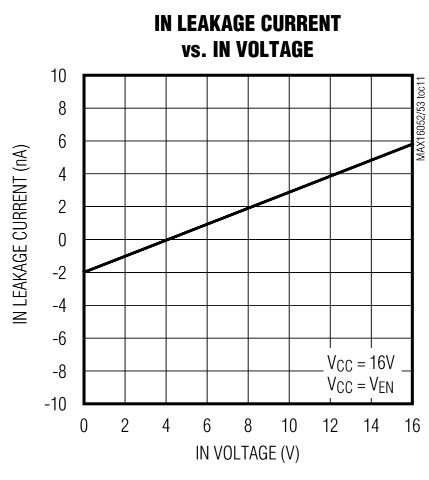
(T_A = +25°C, unless otherwise noted.)





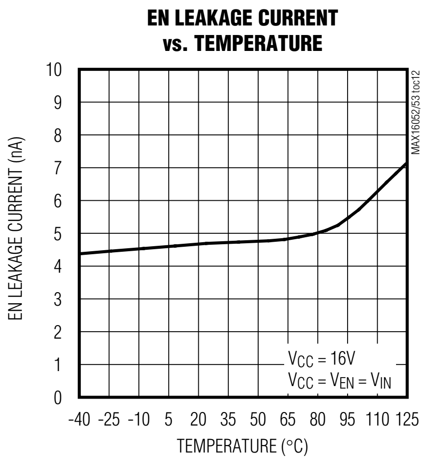


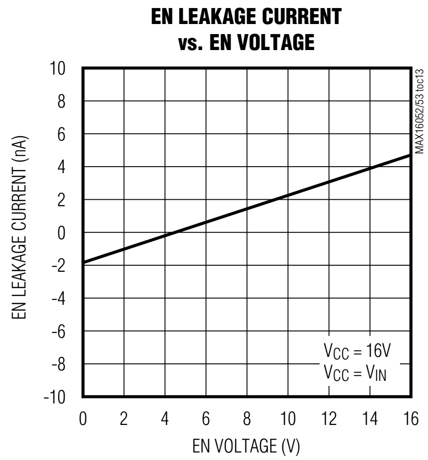




Typical Operating Characteristics (continued)

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	EN	Active-High Logic-Enable Input. Drive EN low to immediately deassert the output to its false state (OUT = low) independent of V_{IN}. With V_{IN} above V_{TH}, drive EN high to assert the output to its true state (OUT = high) after the adjustable delay period. Connect EN to V_{CC}, if not used.
2	GND	Ground
3	IN	High-Impedance Monitor Input. Connect IN to an external resistive divider to set the desired monitor threshold. The output changes state when V_{IN} rises above 0.5V and when V_{IN} falls below 0.495V.
4	OUT	Active-High Sequencer/Monitor Output. Open-drain (MAX16052) or push-pull (MAX16053). OUT is asserted to its true state (OUT = high) when V_{IN} is above V_{TH} and the enable input is in its true state (EN = high) after the capacitor-adjusted delay period. OUT is deasserted to its false state (OUT = low) immediately after V_{IN} drops below 0.495V or the enable input is in its false state (EN = low). The MAX16052 open-drain output requires an external pullup resistor.
5	V_{CC}	Supply Voltage Input. Connect a 2.25V to 16V supply to V_{CC} to power the device. For noisy systems, bypass with a 0.1µF ceramic capacitor to GND.
6	CDELAY	Capacitor-Adjustable Delay Input. Connect an external capacitor (C_{CDELAY}) from CDELAY to GND to set the IN-to-OUT and EN-to-OUT delay period. For V_{IN} rising, $t_{DELAY} = (C_{CDELAY} \times 4.0 \times 10^6) + 30µs$. For EN rising, $t_{PROP} = (C_{CDELAY} \times 4.0 \times 10^6) + 14µs$.

High-Voltage, Adjustable Sequencing/Supervisory Circuits

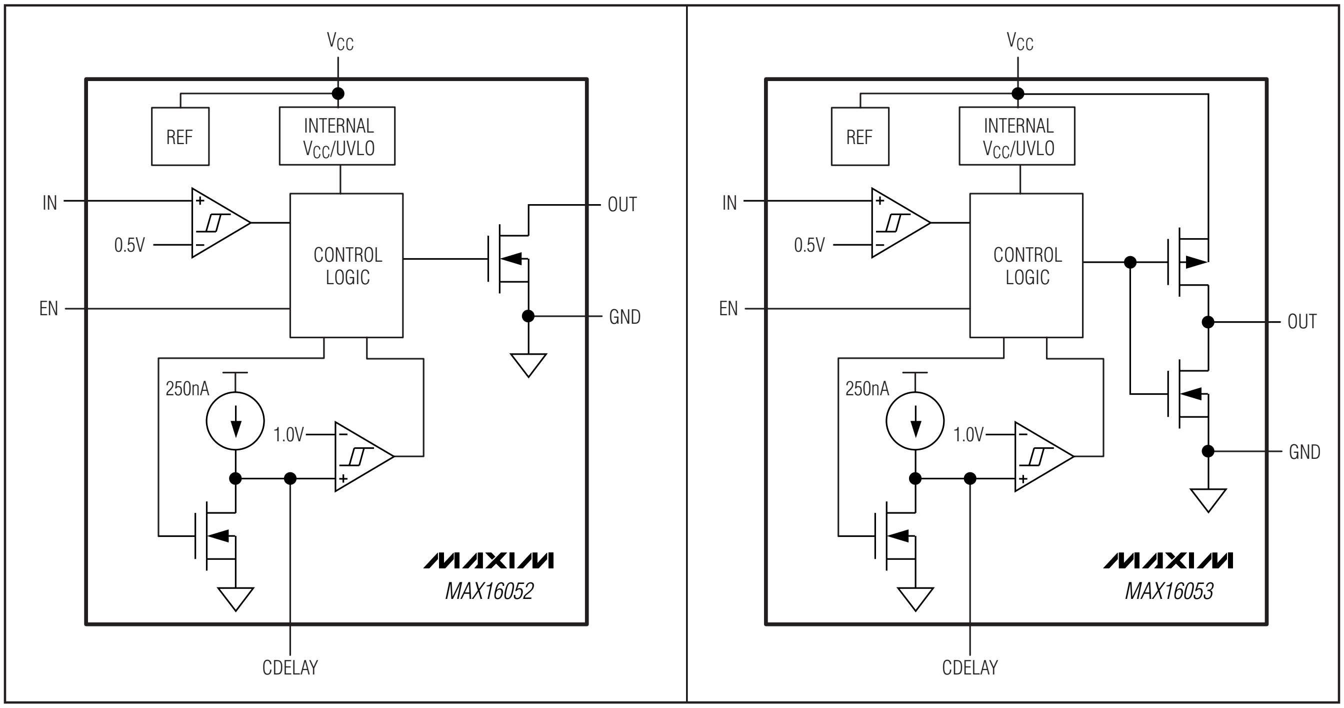


Figure 2. Simplified Functional Diagram

Detailed Description

The MAX16052/MAX16053 family of high-voltage, sequencing/supervisory circuits provide adjustable voltage monitoring for inputs down to 0.5V. These devices are ideal for use in power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

The MAX16052/MAX16053 perform voltage monitoring using a high-impedance input (IN) with an internally fixed 0.5V threshold. When the voltage at IN falls below 0.5V or when the enable input is deasserted (EN = low) OUT goes low. When V_{IN} rises above 0.5V and the enable input is asserted (EN = high), OUT goes high after a capacitor-adjustable time delay.

With V_{IN} above 0.5V, the enable input can be used to turn on or off the output. Table 1 details the output state depending on the various input and enable conditions.

Table 1. MAX16052/MAX16053

IN	EN	OUT
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	OUT = High Impedance (MAX16052)
		OUT = V_{CC} (MAX16053)

Supply Input (V_{CC})

The device operates with a V_{CC} supply voltage from 2.25V to 16V. In order to maintain a 1.8% accurate threshold at IN, V_{CC} must be above 2.25V. When V_{CC} falls below the UVLO threshold, the output deasserts low. When V_{CC} falls below 1.2V, the output state is not guaranteed. For noisy systems, connect a 0.1µF ceramic capacitor from V_{CC} to GND as close to the device as possible.

Monitor Input (IN)

Connect the center point of a resistive divider to IN to monitor external voltages (see R1 and R2 of Figure 4). IN has a rising threshold of V_{TH} = 0.5V and a falling threshold of 0.495V (5mV hysteresis). When V_{IN} rises above V_{TH} and EN is high, OUT goes high after the adjustable t_{DELAY} period. When V_{IN} falls below 0.495V, OUT goes low after a 18µs delay. IN has a maximum input current of 60nA, so large value resistors are permitted without adding significant error to the resistive divider.

Adjustable Delay (CDELAY)

When V_{IN} rises above V_{TH} with EN high, the internal 250nA current source begins charging an external capacitor connected from CDELAY to GND. When the voltage at CDELAY reaches 1V, the output asserts (OUT goes high). When the output asserts, C_{CDELAY} is immediately discharged. Adjust the delay (t_{DELAY}) from when V_{IN} rises above V_{TH} (with EN high) to OUT going high according to the equation:

$$t_{DELAY} = C_{CDELAY} \times (4 \times 10^6 \Omega) + (30\mu s)$$

where t_{DELAY} is in seconds and C_{CDELAY} is in Farads.

Enable Input (EN)

The MAX16052/MAX16053 offer an active-high enable input (EN). With V_{IN} above V_{TH}, drive EN high to force OUT high after the capacitor-adjustable delay time. The EN-to-OUT delay time (t_{PROP}) can be calculated from when EN goes above the EN threshold using the equation:

$$t_{PROP} = C_{CDELAY} \times (4 \times 10^6 \Omega) + (14\mu s)$$

where t_{PROP} is in seconds and C_{CDELAY} is in Farads. Drive EN low to force OUT low within 300ns for the MAX16052 and within 400ns for the MAX16053.

Output (OUT)

The MAX16052 offers an active-high, open-drain output while the MAX16053 offers an active-high push-pull output. The push-pull output is referenced to V_{CC}. The open-drain output requires a pullup resistor and can be pulled up to 28V.

Applications Information

Input Threshold

The MAX16052/MAX16053 monitor the voltage on IN with an external resistive divider (Figure 4). R1 and R2 can have very high values to minimize current consumption due to low IN leakage currents (60nA max). Set R2 to some conveniently high value (200kΩ for ±1% additional variation in threshold, for example) and calculate R1 based on the desired monitored voltage using the following formula:

$$R1 = R2 \times \left[\frac{V_{MONITOR}}{V_{TH}} - 1\right]$$

where $V_{MONITOR}$ is the desired monitored voltage and V_{TH} is the reset input threshold (0.5V).

Pullup Resistor Values (MAX16052 Only)

The exact value of the pullup resistor for the open-drain output is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{CC} = 2.25V and the pullup voltage is 28V, keep the sink current less than 0.5mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 56kΩ. For a 12V pullup, the resistor should be larger than 24kΩ. Note that the ability to sink current is dependent on the V_{CC} supply voltage.

Ensuring a Valid OUT Down to V_{CC} = 0V (Push-Pull OUT)

In applications in which OUT must be valid down to V_{CC} = 0V, add a pulldown resistor between OUT and GND for the push-pull output (MAX16053). The resistor sinks any stray leakage currents, holding OUT low (Figure 3). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load OUT and small enough to pull OUT to ground. The external pulldown cannot be used with the open-drain OUT output.

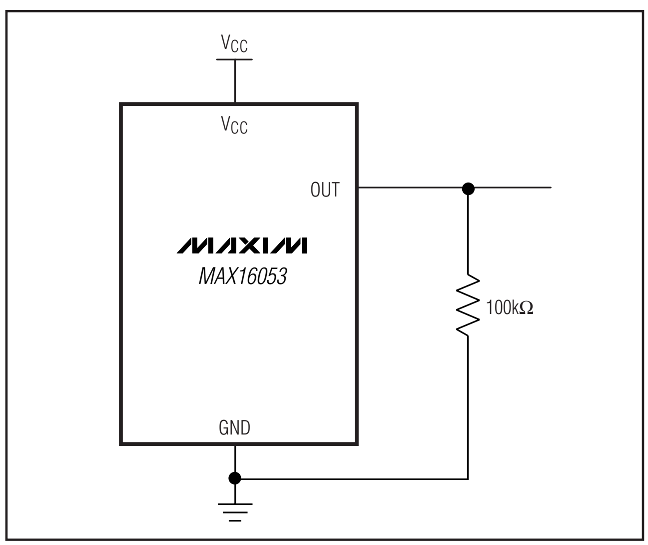


Figure 3. Ensuring OUT Valid to V_{CC} = 0V

High-Voltage, Adjustable Sequencing/Supervisory Circuits

Typical Application Circuits

Figures 4–6 show typical applications for the MAX16052/MAX16053. Figure 4 shows the MAX16052 used with a p-channel MOSFET in an overvoltage protection circuit. Figure 5 shows the MAX16053 in a low-voltage sequencing application using an n-channel MOSFET. Figure 6 shows the MAX16053 used in a multiple output sequencing application.

Using an n-Channel Device for Sequencing

In higher power applications, using an n-channel device reduces the loss across the MOSFET as it offers a lower drain-to-source on-resistance. However, an n-channel MOSFET requires a sufficient V_{GS} voltage to fully enhance it for a low R_{DS_ON}. The application shown in Figure 5 shows the MAX16053 in a switch sequencing application using an n-channel MOSFET.

Similarly, if a higher voltage is present in the system, the open-drain version can be used in the same manner.

Power-Supply Bypassing

In noisy applications, bypass V_{CC} to ground with a 0.1µF capacitor as close to the device as possible. The additional capacitor improves transient immunity. For fast-rising V_{CC} transients, additional capacitors may be required.

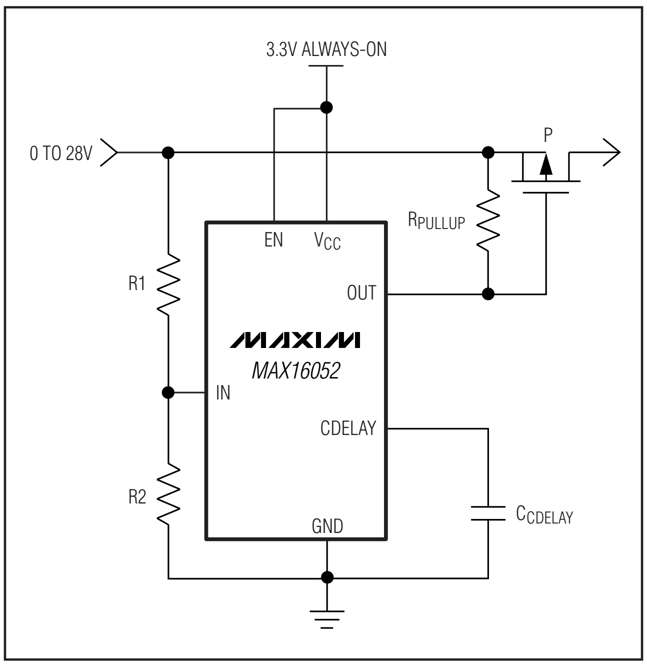


Figure 4. Overvoltage Protection

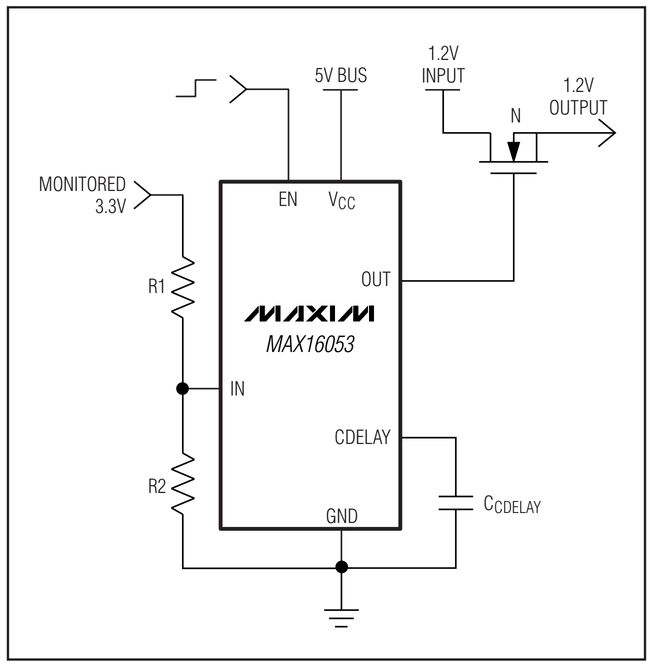


Figure 5. Low-Voltage Sequencing Using an n-Channel MOSFET

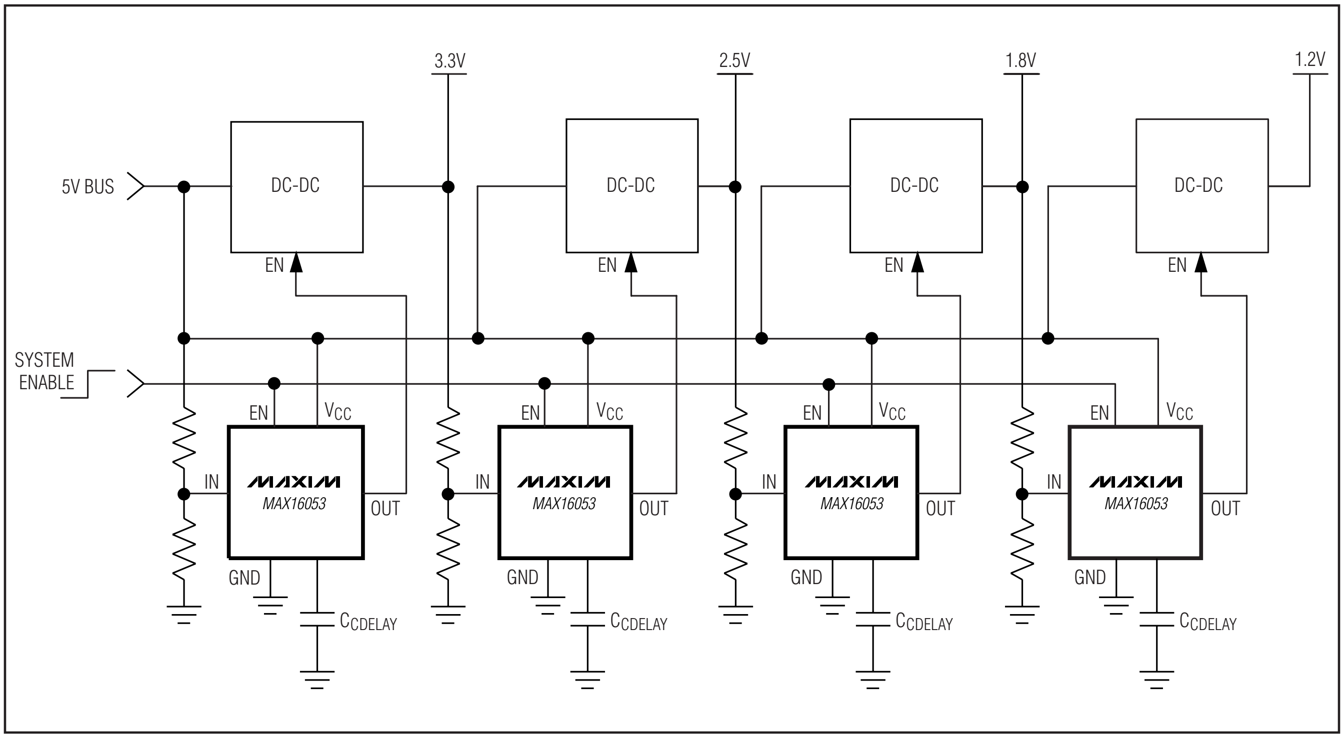


Figure 6. Multiple Output Sequencing

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SOT23	U6+1	21-0058

High-Voltage, Adjustable Sequencing/Supervisory Circuits

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	10/08	Update *Adjustable Delay (CDELAY)* and *Power-Supply Bypassing* sections.	8, 10