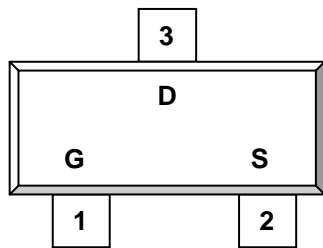


**DESCRIPTION**

The ST7407 is the P-Channel logic enhancement mode power field effect transistors It is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

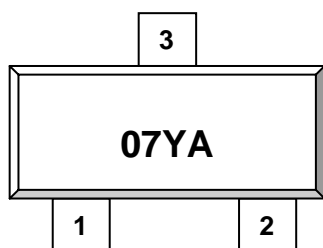
These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION**  
**SOT-323 (SC-70)**


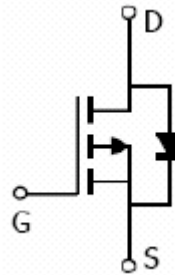
1.Gate 2.Source 3.Drain

**FEATURE**

- -20V/-3.4A,  $R_{DS(ON)} = 100\text{m-ohm}$  @VGS = -4.5V
- -20V/-2.4A,  $R_{DS(ON)} = 125\text{m-ohm}$  @VGS = -2.5V
- -20V/-1.8A,  $R_{DS(ON)} = 170\text{m-ohm}$  @VGS = -1.8V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-323 (SC-70) package design

**PART MARKING**  
**SOT-323 (SC-70)**


Y: Year Code A: Process Code


**ORDERING INFORMATION**

Part Number	Package	Part Marking
ST7407S32RG	SOT-323	07YA

※ Process Code : A ~ Z ; a ~ z

※ ST7407S32RG S32 : SOT-323 ; R : Tape Reel ; G : Pb – Free



**ST7407**   
Lead-free

P Channel Enhancement Mode MOSFET

**-3.4A**

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±12	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C -2.3	A
		T <sub>A</sub> =70°C -1.7	
Pulsed Drain Current	I <sub>DM</sub>	-6	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.4	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 0.35	W
		T <sub>A</sub> =70°C 0.22	
Operation Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	120	°C/W

**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-0.8	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-20V, V_{GS}=0V$			-1	$\mu A$
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-5.0	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$	-6			A
		$V_{DS}\leq -5V, V_{GS}=-2.5V$	-3			
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.4A$		0.090	0.100	$\Omega$
		$V_{GS}=-2.5V, I_D=-2.4A$		0.115	0.125	
		$V_{GS}=-1.8V, I_D=-1.8A$		0.150	0.170	
Forward Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-2.8V$		6.0		S
Diode Forward Voltage	$V_{SD}$	$I_s=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-6V$ $V_{GS}=-4.5V$ $I_D=-2.8A$		4.8	8.0	nC
Gate-Source Charge	$Q_{gs}$			1.0		
Gate-Drain Charge	$Q_{gd}$			1.0		
Input Capacitance	$C_{iss}$	$V_{DS}=-6.0V$ $V_{GS}=0V$ $F=1MHz$		485		pF
Output Capacitance	$C_{oss}$			85		
Reverse Transfer Capacitance	$C_{rss}$			40		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=-6V$ $R_L=6\Omega$ $I_D=-1.0A$ $V_{GEN}=-4.5V$ $R_G=6\Omega$		10	16	nS
				13	23	
Turn-Off Time	$t_{d(off)}$ $t_f$			18	25	
				15	20	

**TYPICAL CHARACTERISTICS (25°C Unless noted)**

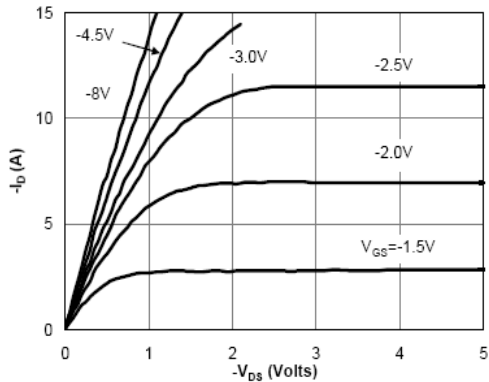


Fig 1: On-Region Characteristics

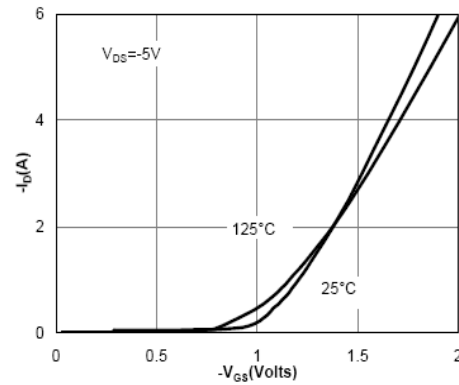


Figure 2: Transfer Characteristics

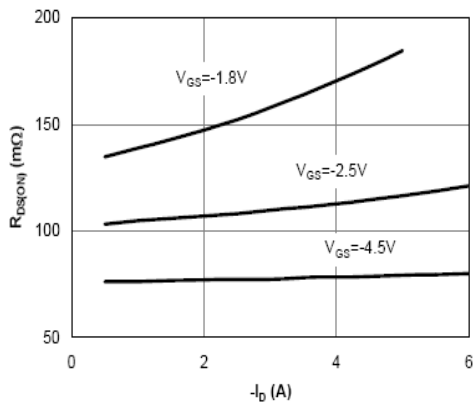


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

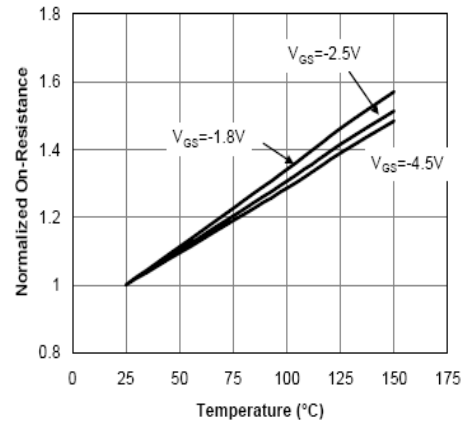


Figure 4: On-Resistance vs. Junction Temperature

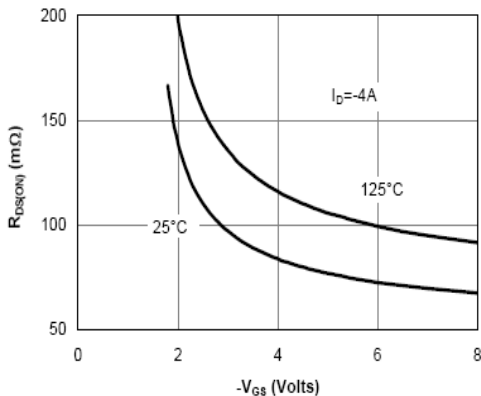


Figure 5: On-Resistance vs. Gate-Source Voltage

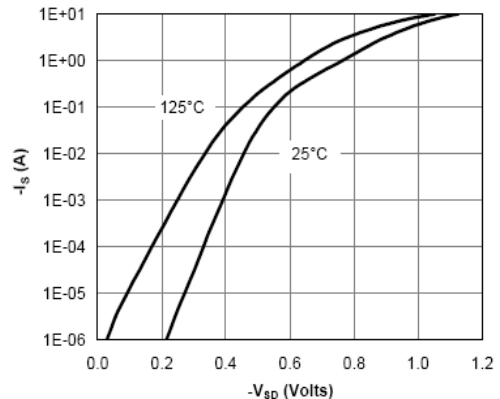


Figure 6: Body-Diode Characteristics



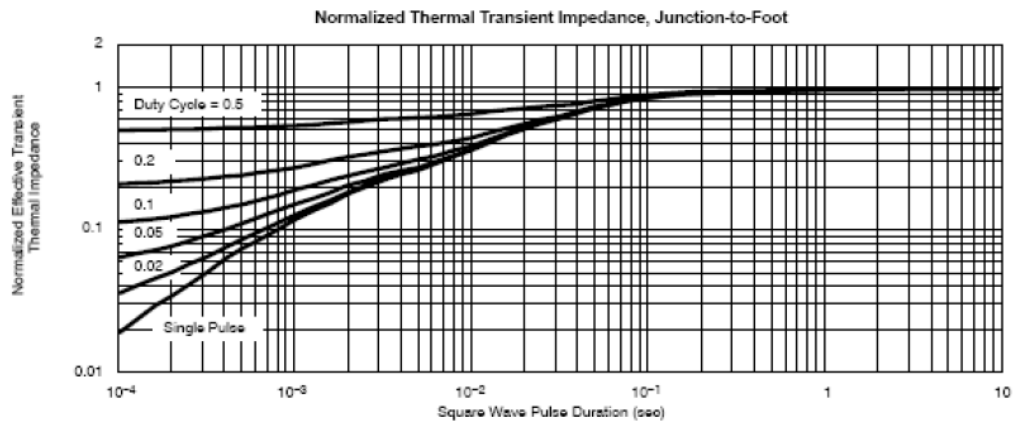
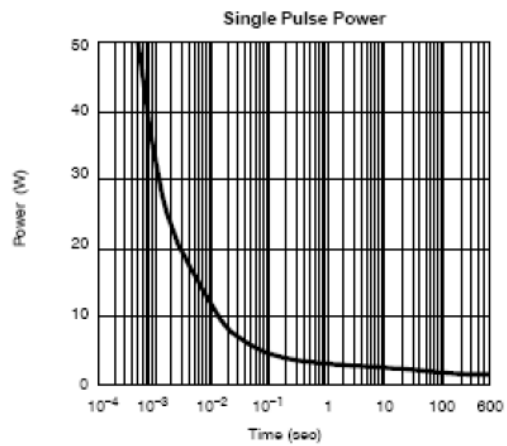
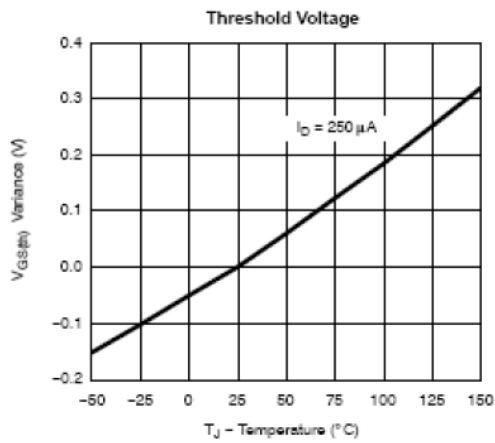
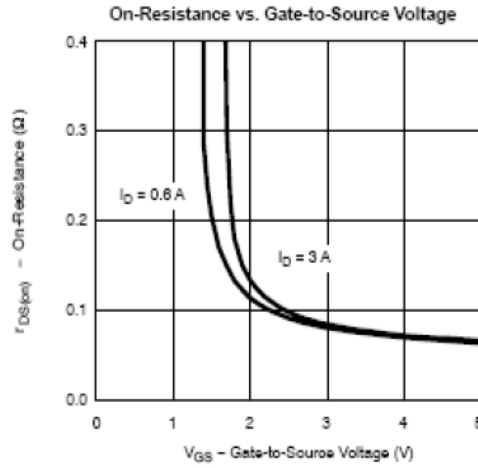
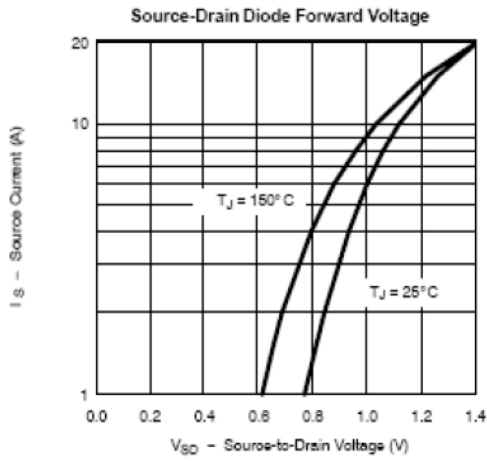
**ST7407**  Lead-free

P Channel Enhancement Mode MOSFET

**-3.4A**

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**TYPICAL CHARACTERISTICS** (25°C Unless noted)



**SOT-323 (SC-70) PACKAGE OUTLINE**
