TOSHIBA Field Effect Transistor with Built-in Schottky Barrier Diode

Silicon N-Channel MOS Type (U-MOS V -H)

TPC8A07-H

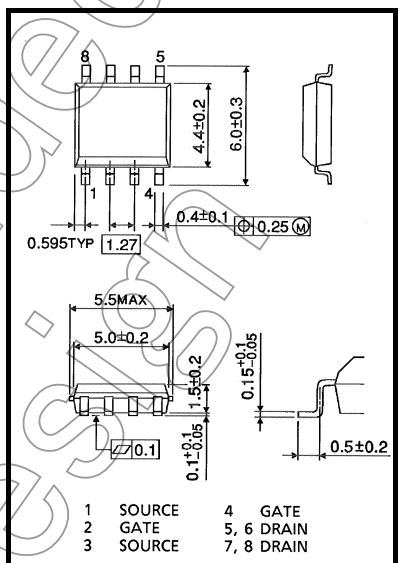
High Efficiency DC-DC Converter Applications

Notebook PC Applications

Portable-Equipment Applications

- Small footprint due to a small and thin package
- High-speed switching
- Small gate charge: (Q1) Q_{SW} = 3.4 nC (typ.)
  (Q2) Q_{SW} = 3.6 nC (typ.)
- Low drain-source ON-resistance: (Q1) $R_{DS\ (ON)}$ = 21 mΩ (typ.)
  (Q2) $R_{DS\ (ON)}$ = 14 mΩ (typ.)
- Low leakage current: (Q1) I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
  (Q2) I_{DSS} =100μA (max) (V_{DS} = 30 V)
- Enhancement mode: (Q1) V_{th} = 1.5 to 2.5 V (V_{DS} = 10 V, I_D = 1.0 mA)
  (Q2) V_{th} = 1.3 to 2.3 V (V_{DS} = 10 V, I_D = 1.0 mA)

Unit: mm



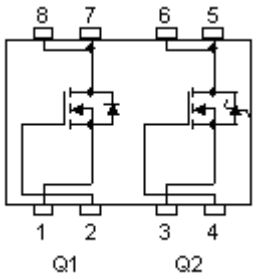
JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.085 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating (Q1)	Rating (Q2)	Unit
Drain−source voltage		V_{DSS}	30	30	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	30	V
Gate−source voltage		V_{GSS}	±20	±20	V
Drain current	D C (Note 1)	I_D	6.8	8.5	A
	Pulse (Note 1)	I_{DP}	27.2	34	
Drain power dissipation (t = 10 s) (Note 2a)	Single-device operation (Note 3a)	$P_{D\ (1)}$	1.5		W
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	1.1		
Drain power dissipation (t = 10 s) (Note 2b)	Single-device operation (Note 3a)	$P_{D\ (1)}$	0.75		W
	Single-device value at dual operation (Note 3b)	$P_{D\ 2)}$	0.45		
Single-pulse avalanche energy (Note 4)		E_{AS}	60.1	94	mJ
Avalanche current		I_{AR}	6.8	8.5	A
Repetitive avalanche energy (Note 2a, Note 3b, Note 5)		E_{AR}	0.11	0.09	mJ
Channel temperature		T_{ch}	150		°C
Storage temperature range		T_{stg}	−55 to 150		°C

Circuit Configuration



Note: For Notes 1 to 5, refer to the next page.

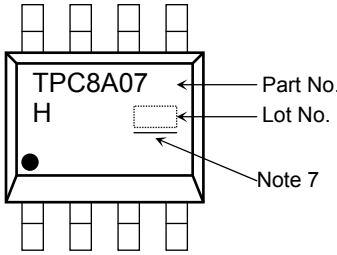
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating” Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Thermal Characteristics

Characteristic		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	114	
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

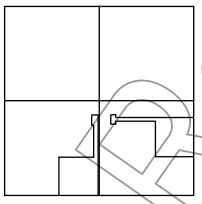
Marking (Note 6)



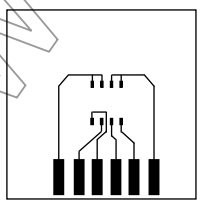
Note 7: A line under a Lot No. identifies the indication of product Labels.
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.
The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



(a)



(b)

Note 3:

a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.)

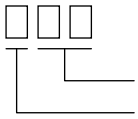
b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.)

Note 4: (Q1) V_{DD} = 24 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 6.8 A
(Q2) V_{DD} = 24 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 8.5 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on the lower left of the marking indicates Pin 1.

* Weekly code: (three digits)

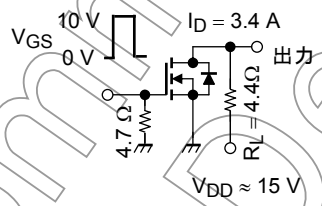


Week of manufacture
(01 for the first week of the year, continuing up to 52 or 53)

Year of manufacture
(the last digit of the year)

Q1

Electrical Characteristics (Ta = 25°C)

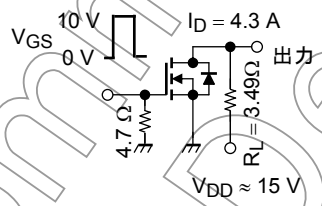
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	15	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	1.5	—	2.5	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 3.4 A	—	21	28	mΩ
			V_{GS} = 10 V, I_D = 3.4 A	—	17	23	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 3.4 A	11	22	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	830	1100	pF
Reverse transfer capacitance		C_{rss}		—	54	82	
Output capacitance		C_{oss}		—	180	—	
Gate resistance		r_g	V_{DS} = 10 V, V_{GS} = 0 V, f = 5 MHz	—	1.7	2.6	Ω
Switching time	Rise time	t_r		—	2.2	—	ns
	Turn-on time	t_{on}		—	7.7	—	
	Fall time	t_f		—	2.5	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	18	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 6.8 A	—	13	—	nC
			V_{DD} ≈ 24 V, V_{GS} = 5 V, I_D = 6.8 A	—	6.9	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 6.8 A	—	2.9	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	2.3	—	
Gate switch charge		Q_{SW}		—	3.4	—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	27.2	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 6.8 A, V_{GS} = 0 V	—	—	−1.2	V

Q2

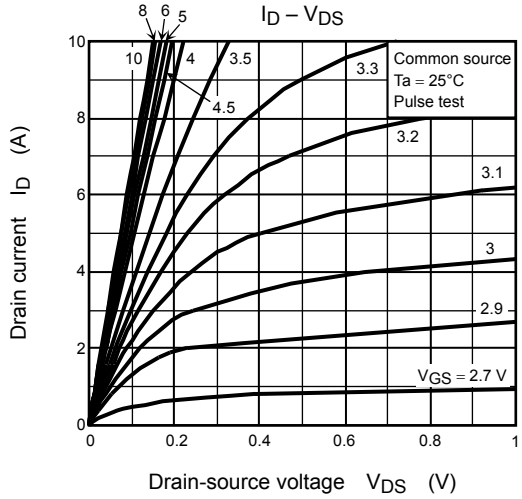
Electrical Characteristics (Ta = 25°C)

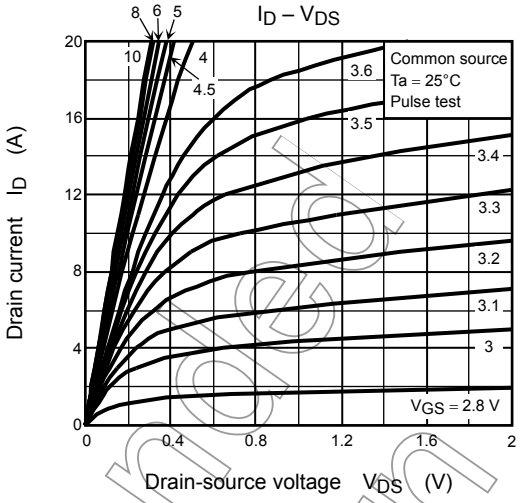
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	15	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	1.3	—	2.3	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 4.3 A	—	14	19	mΩ
			V_{GS} = 10 V , I_D = 4.3 A	—	11	15	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 4.3 A	13	26	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1100	1400	pF
Reverse transfer capacitance		C_{rss}		—	50	75	
Output capacitance		C_{oss}		—	320	—	
Gate resistance		r_g	V_{DS} = 10 V, V_{GS} = 0 V, f = 5 MHz	—	1.9	2.9	Ω
Switching time	Rise time	t_r		—	2.1	—	ns
	Turn-on time	t_{on}		—	7.8	—	
	Fall time	t_f		—	3.1	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	22	—	
Total gate charge (gate-source plus gate-drain) (Note 7)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 8.5 A	—	16	—	nC
			V_{DD} ≈ 24 V, V_{GS} = 5 V, I_D = 8.5 A	—	8.1	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 8.5 A	—	3.4	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	2.2	—	
Gate switch charge		Q_{SW}		—	3.6	—	

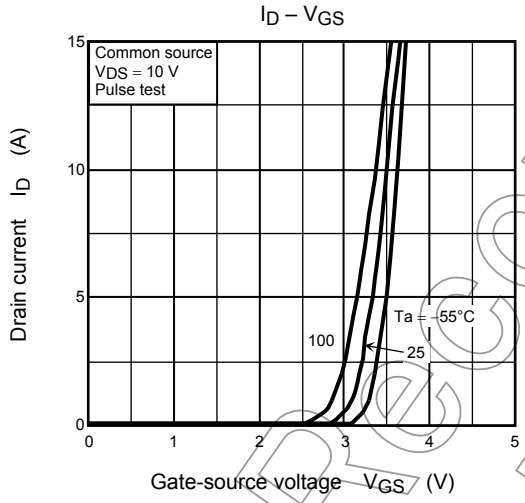
Source−Drain Ratings and Characteristics (Ta = 25°C)

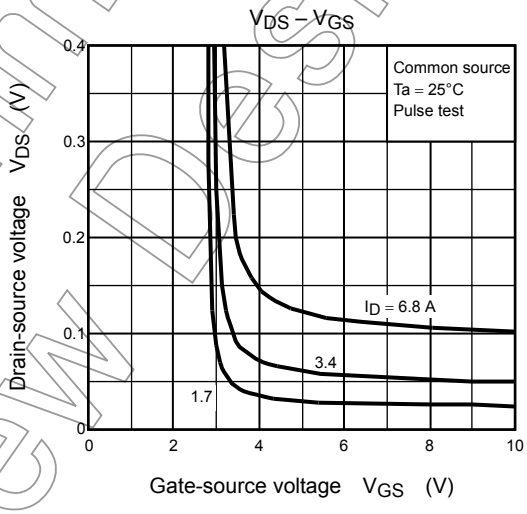
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Peak forward current	Pulse (Note 1)	I_{FP}	—	—	—	34	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 1 A, V_{GS} = 0 V	—	− 0.4	− 0.6	V
			I_{DR} = 8.5 A, V_{GS} = 0 V	—	—	− 1.2	V

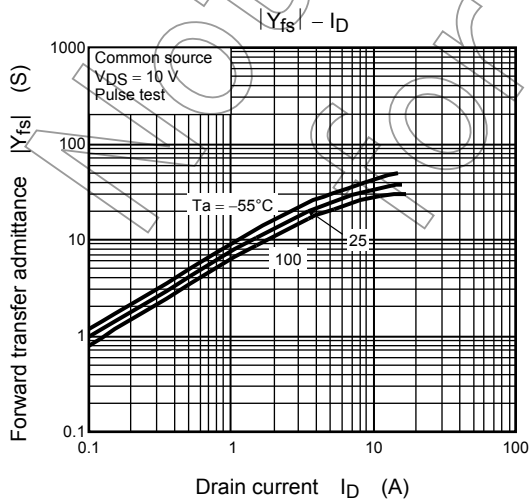
Q1

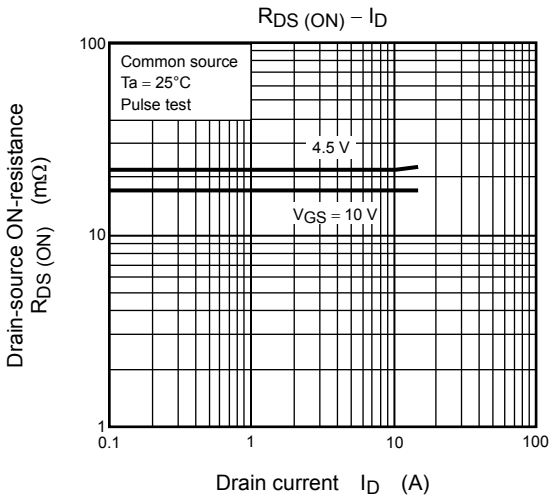






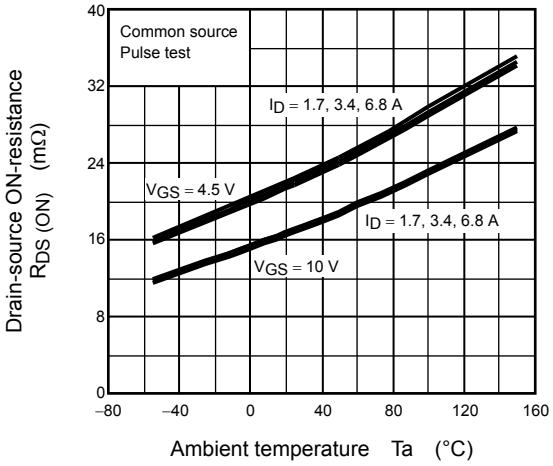




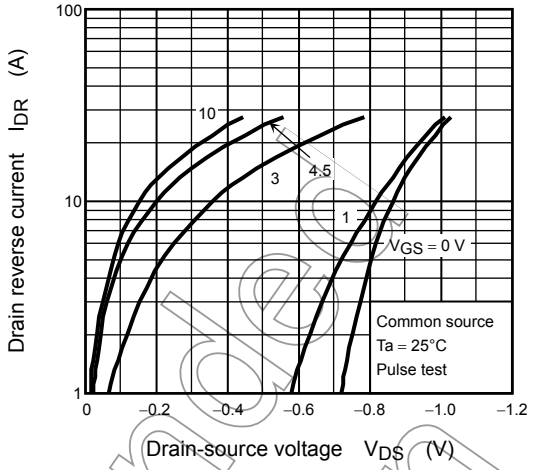


Q1

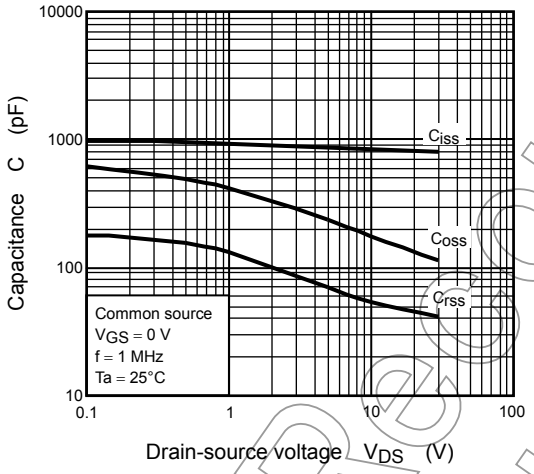
$R_{DS\ (ON)}$ – Ta



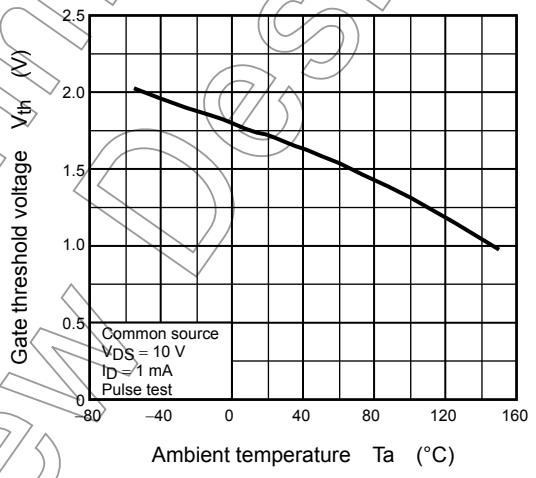
I_{DR} – V_{DS}



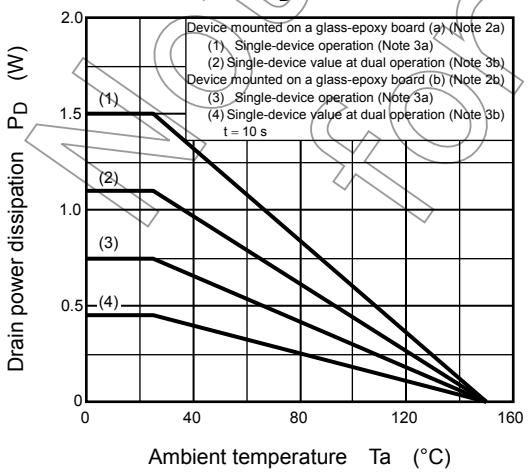
Capacitance – V_{DS}



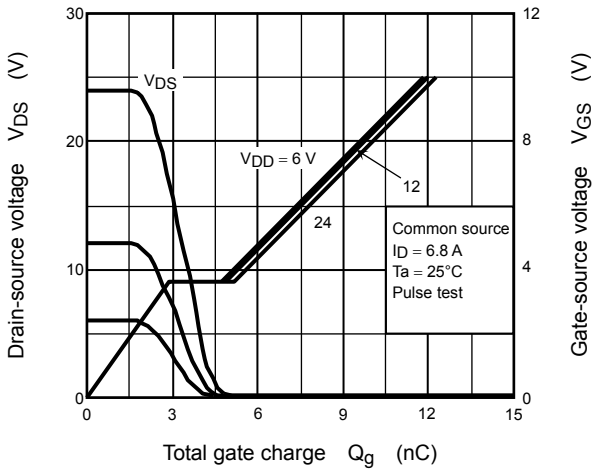
V_{th} – Ta



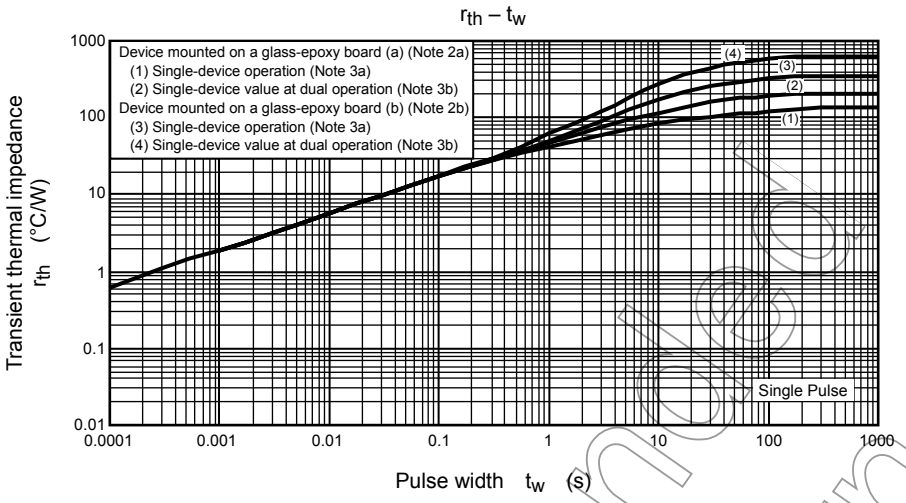
P_D – Ta

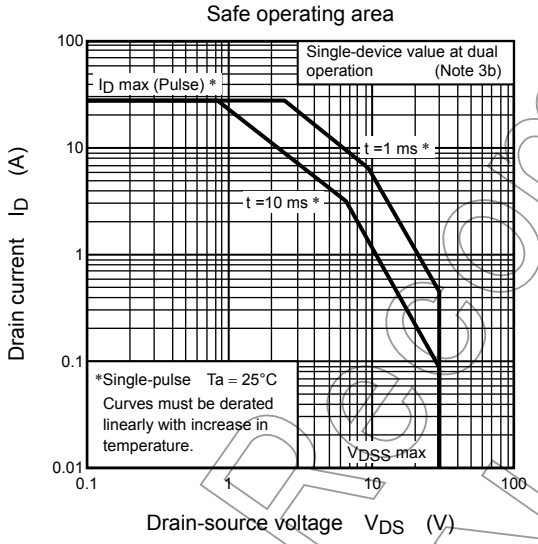


Dynamic input/output characteristics

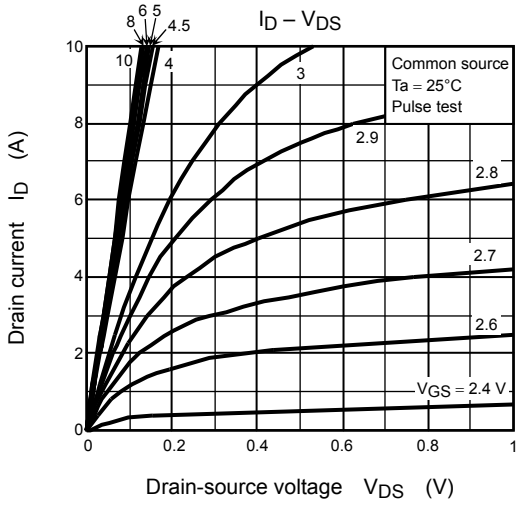


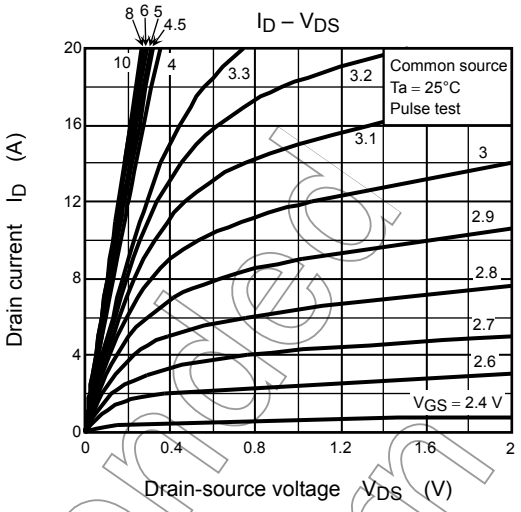
Q1

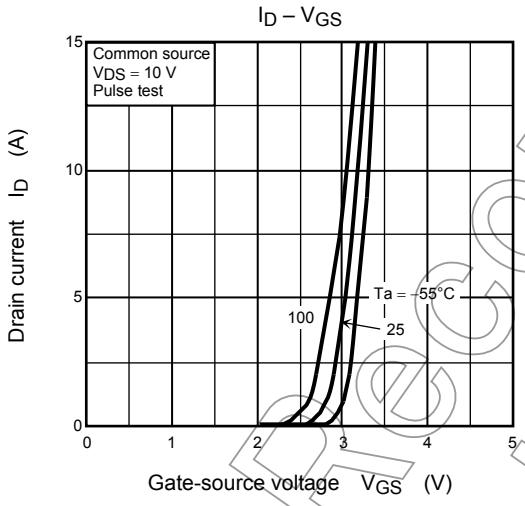


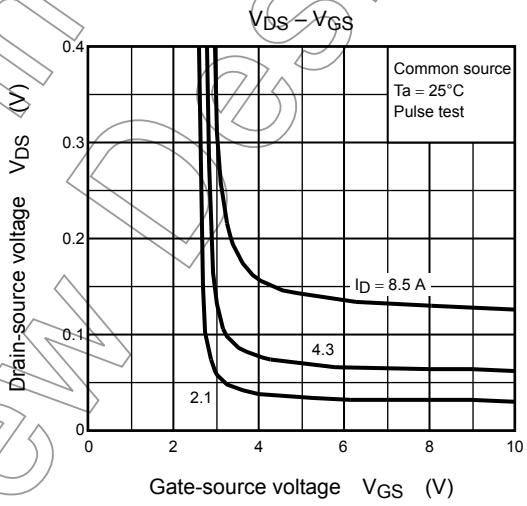


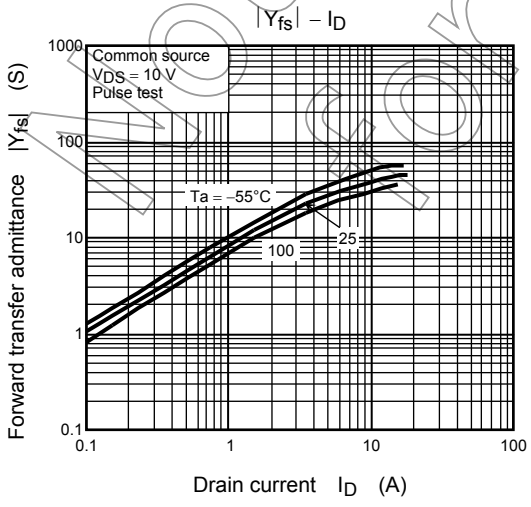
Q2 (Includes Schottky Barrier Diode)

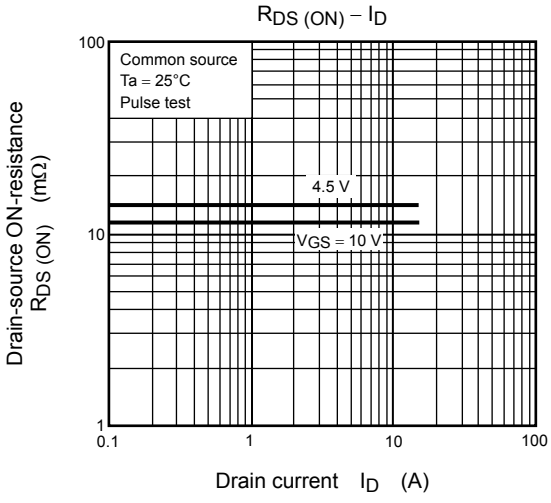






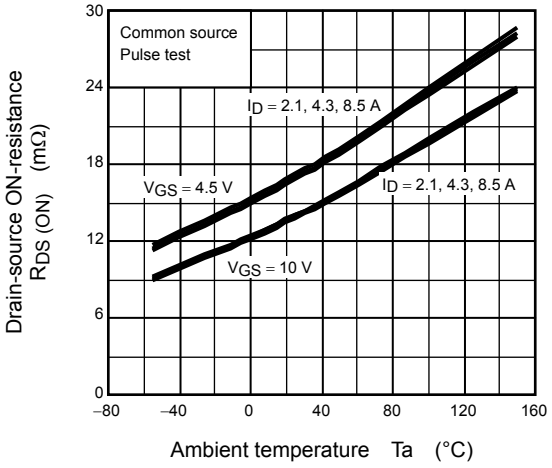




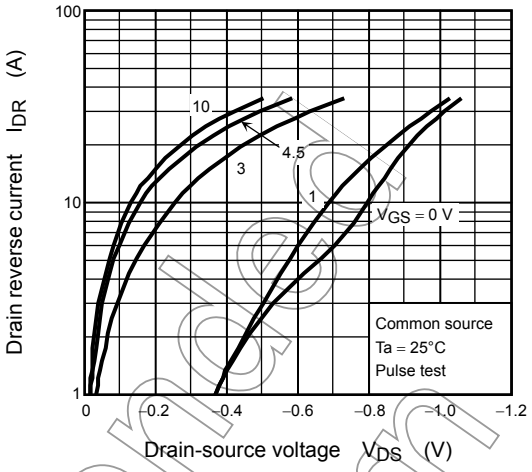


Q2 (Includes Schottky Barrier Diode)

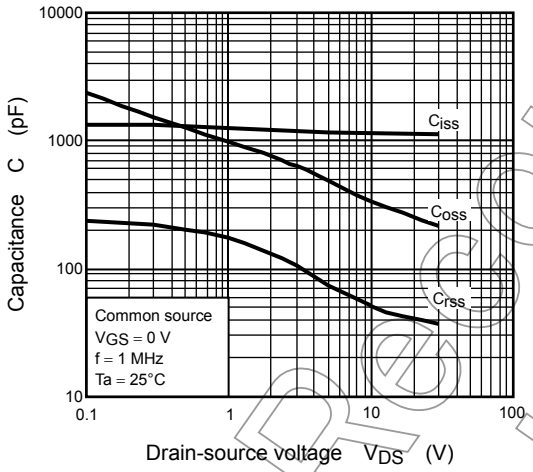
$R_{DS\ (ON)}$ – Ta



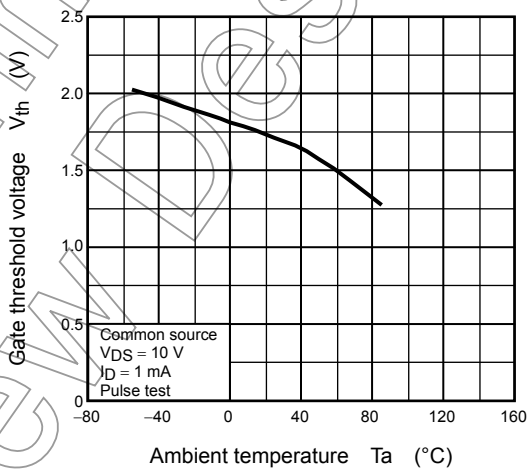
I_{DR} – V_{DS}



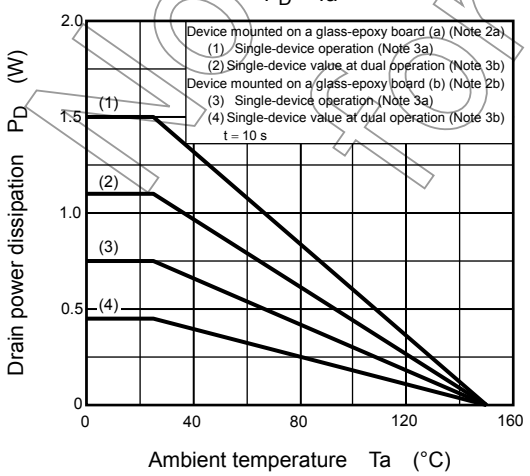
Capacitance – V_{DS}



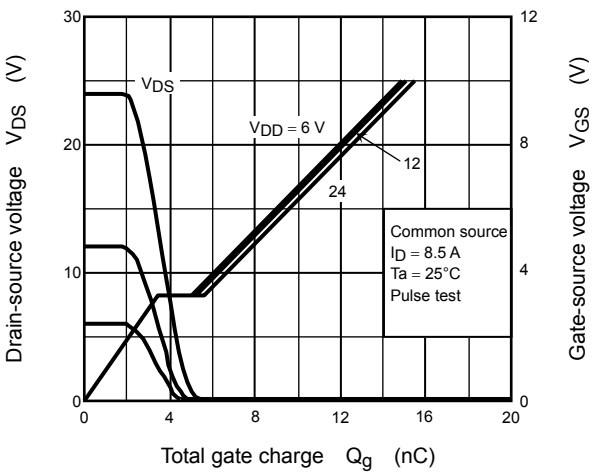
V_{th} – Ta



P_D – Ta

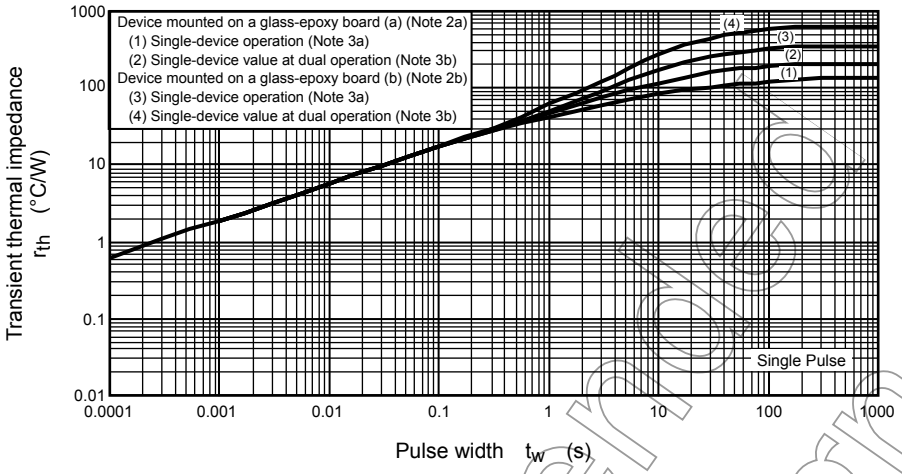


Dynamic input/output characteristics

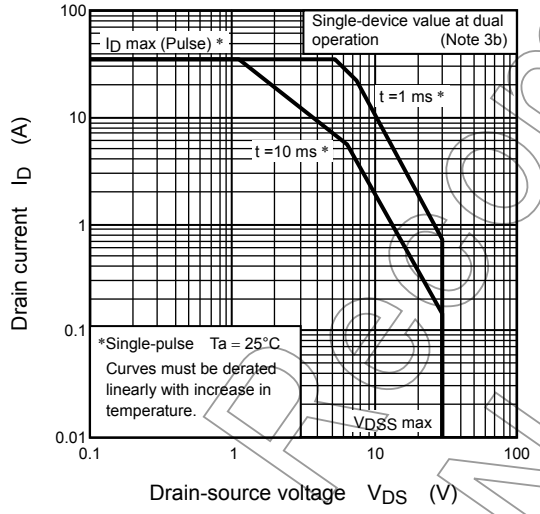


Q2 (Includes Schottky Barrier Diode)

$r_{th} - t_w$

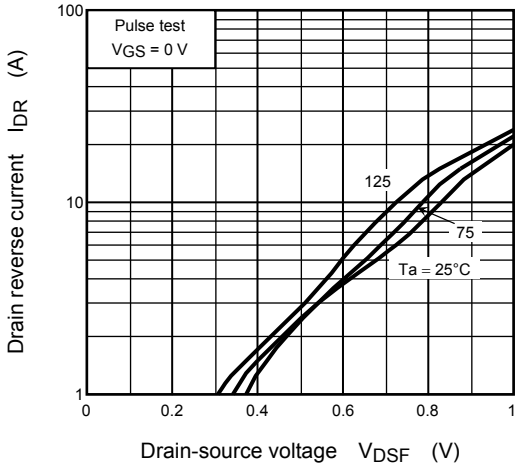


Safe operating area

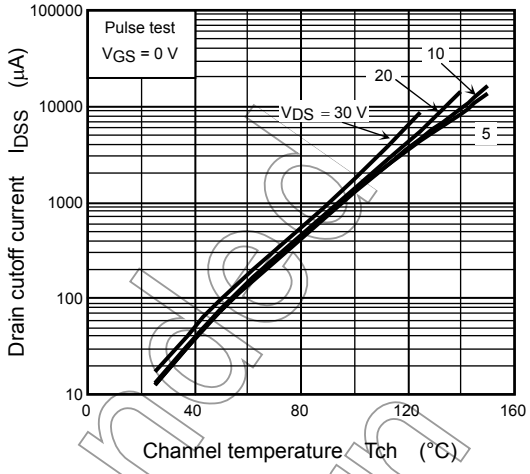


Q2 (V_{GS}= 0V)

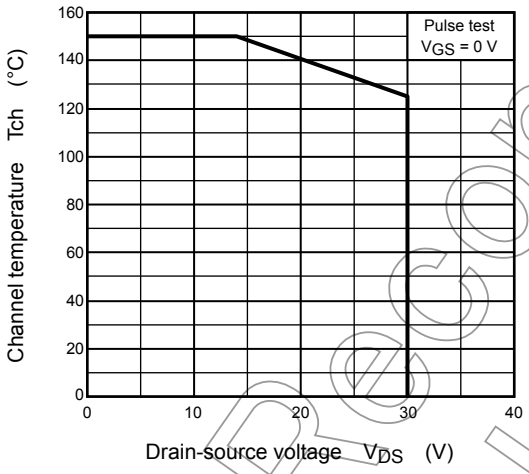
I_{DR} – V_{DSF}



I_{DSS} – Tch (typ.)



Tch – V_{DS}



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