

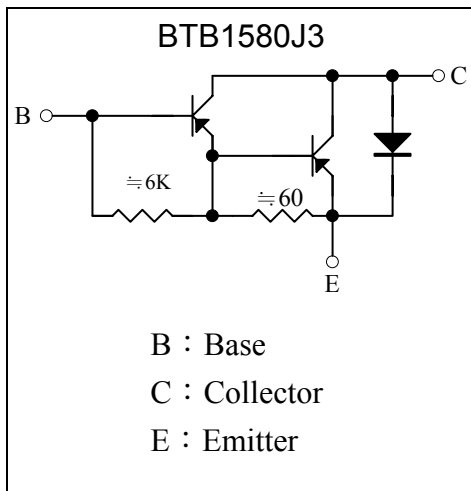
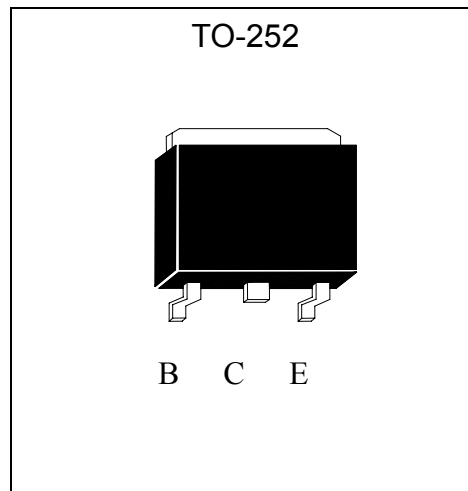
**PNP Epitaxial Planar Transistor**

# BTB1580J3

$BV_{CEO}$	-120V
$I_C$	-4A
$R_{CESAT}$	600m $\Omega$

**Description**

The BTB1580J3 is a PNP Darlington transistor, designed for use in general purpose amplifier and low speed switching application. Pb-free package process is adopted.

**Equivalent Circuit**

**Outline**

**Absolute Maximum Ratings** ( $T_a=25^\circ\text{C}$ )

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	$V_{CB0}$	-120	V
Collector-Emitter Voltage	$V_{CEO}$	-120	V
Emitter-Base Voltage	$V_{EB0}$	-5	V
Collector Current (DC)	$I_C$	-4	A
Collector Current (Pulse)	$I_{CP}$	-6	A
Power Dissipation( $T_A=25^\circ\text{C}$ )	$P_d$	1.5	W
Power Dissipation( $T_C=25^\circ\text{C}$ )		20	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Junction Temperature	$T_j$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55~+150	$^\circ\text{C}$

Note : Single Pulse  $P_w \leq 300\mu\text{s}$ , Duty  $\leq 2\%$ .

**Characteristics (Ta=25°C)**

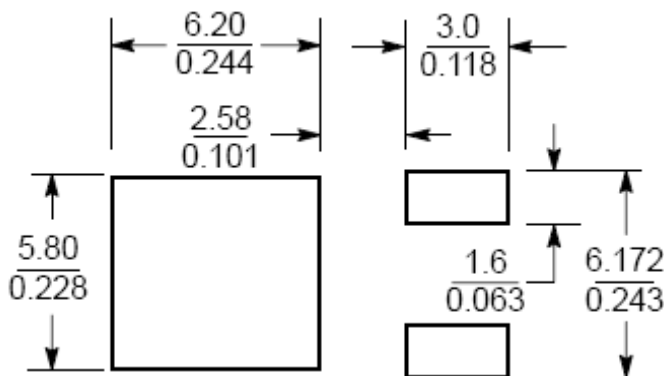
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CEO</sub>	-120	-	-	V	I <sub>C</sub> =-1mA, I <sub>B</sub> =0
BV <sub>CBO</sub>	-120	-	-	V	I <sub>C</sub> =-100μA, I <sub>E</sub> =0
I <sub>CBO</sub>	-	-	-1	mA	V <sub>CB</sub> =-100V, I <sub>E</sub> =0
I <sub>CEO</sub>	-	-	-2	mA	V <sub>CE</sub> =-50V, I <sub>B</sub> =0
I <sub>EBO</sub>	-	-	-2	mA	V <sub>EB</sub> =-5V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-	-2	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-2mA
*V <sub>BE(on)</sub>			-2.8	V	V <sub>CE</sub> =-4V, I <sub>C</sub> =-2A
*h <sub>FE1</sub>	1000	-	-	-	V <sub>CE</sub> =-4V, I <sub>C</sub> =-1A
*h <sub>FE2</sub>	500	-	-	-	V <sub>CE</sub> =-4V, I <sub>C</sub> =-2A
Cob	-		200	pF	V <sub>CB</sub> =-10V, I <sub>E</sub> =0A, f=1MHz

\*Pulse Test : Pulse Width ≤380μs, Duty Cycle ≤2%

**Ordering Information**

Device	Package	Shipping	Marking
BTB1580J3	TO-252 (Pb-free)	2500 pcs / Tape & Reel	B1580

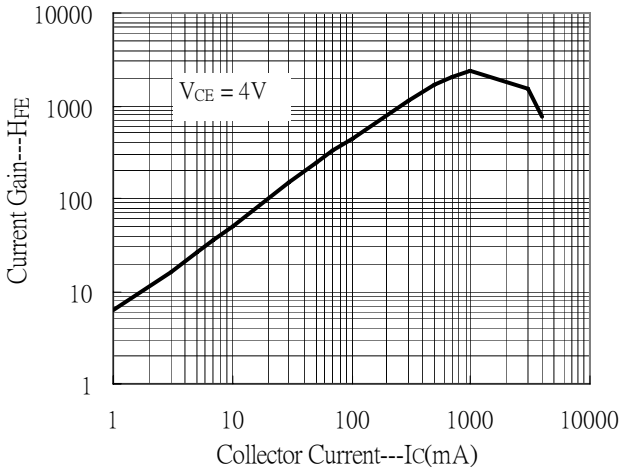
**Recommended soldering footprint**



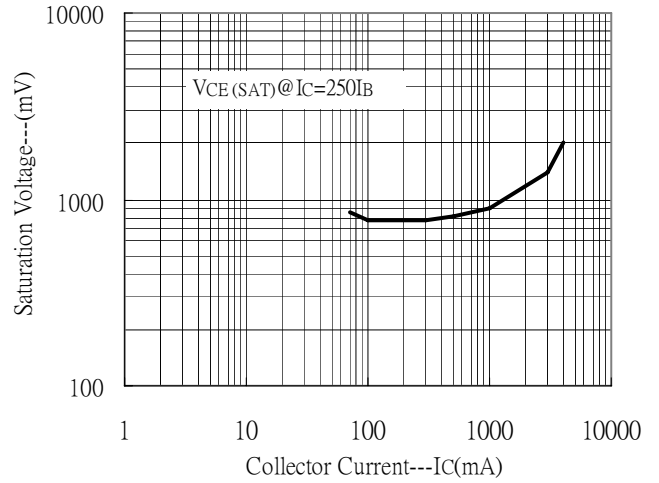
Unit (  $\frac{\text{mm}}{\text{inch}}$  )

**Characteristic Curves**

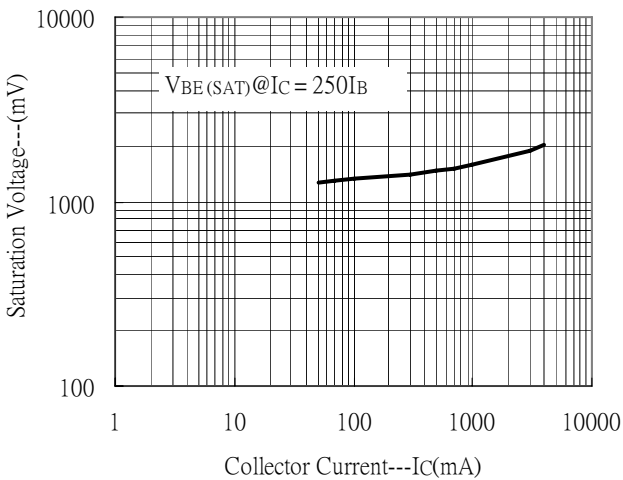
Current Gain vs Collector Current



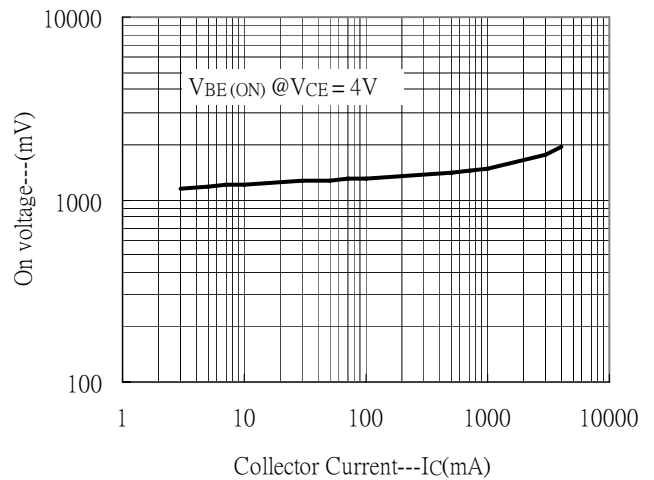
Saturation Voltage vs Collector Current



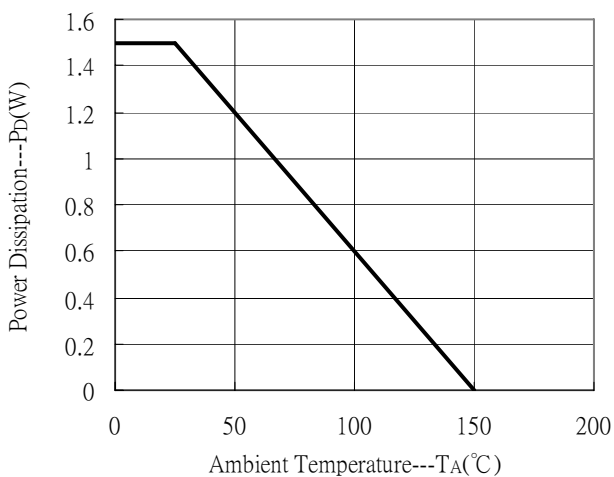
Saturation Voltage vs Collector Current



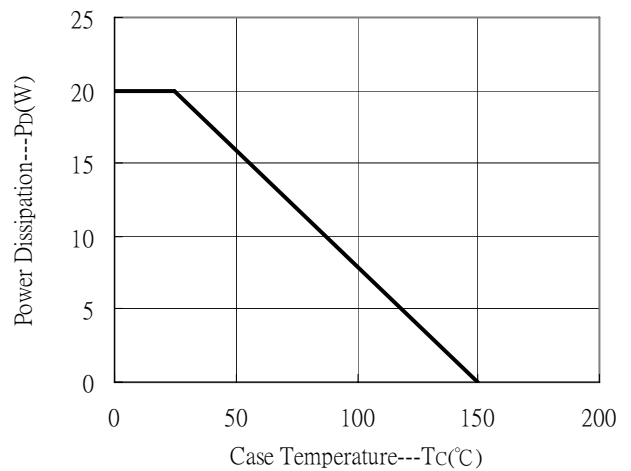
On voltage vs Collector Current



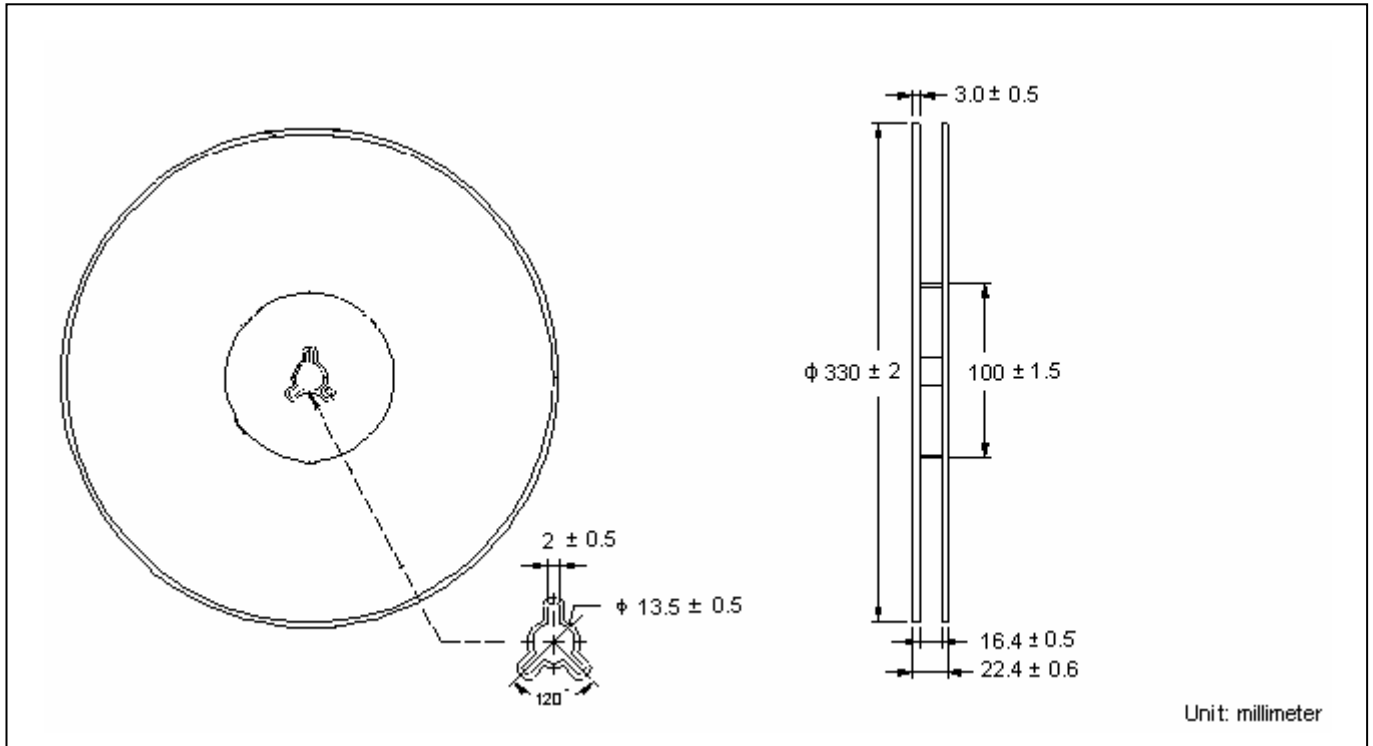
Power Derating Curve



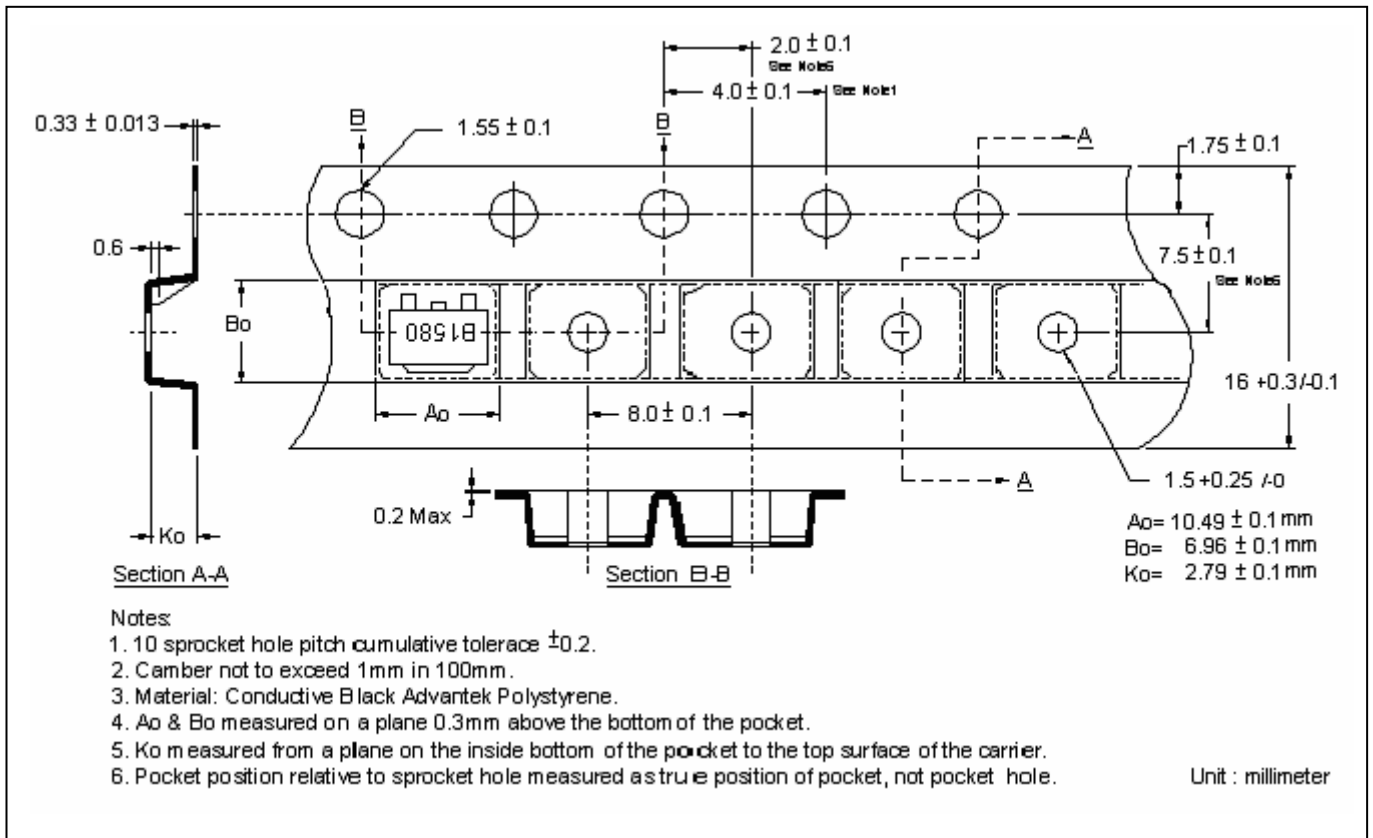
Power Derating Curve



**Reel Dimension**

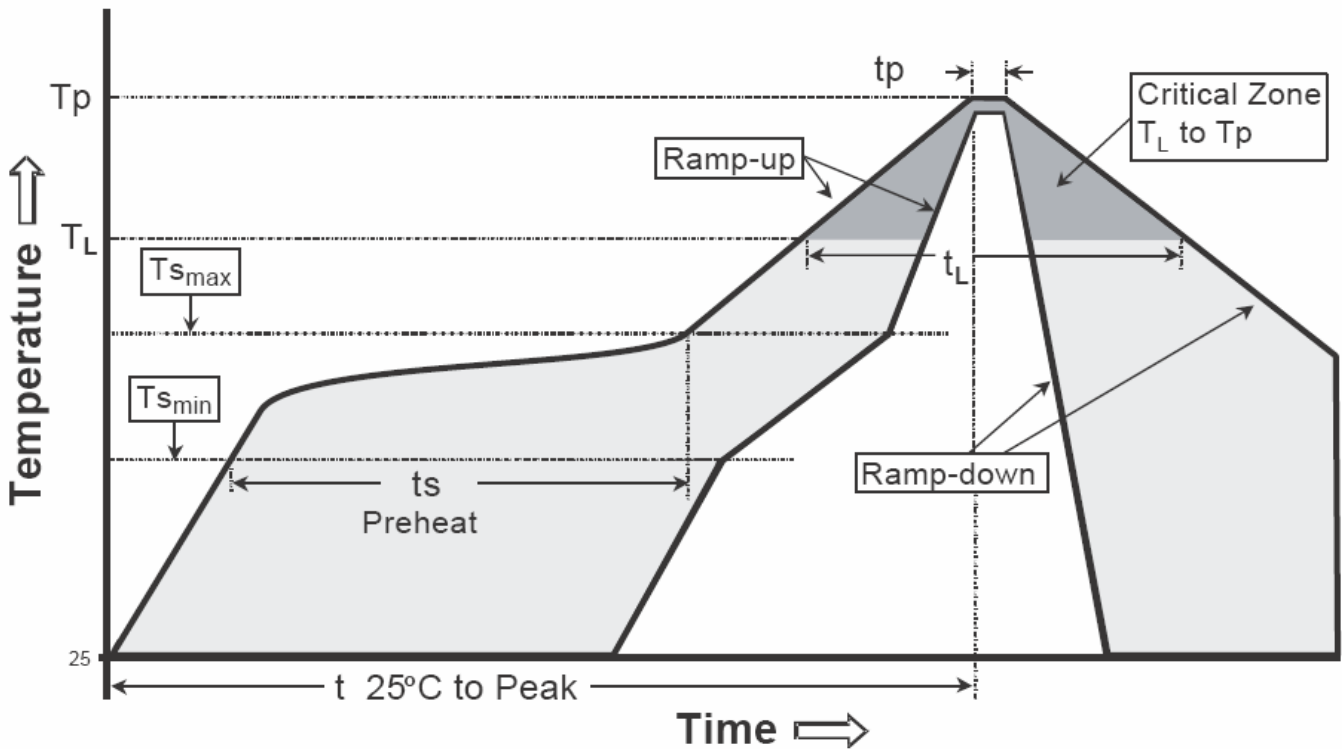


**Carrier Tape Dimension**



**Recommended wave soldering condition**

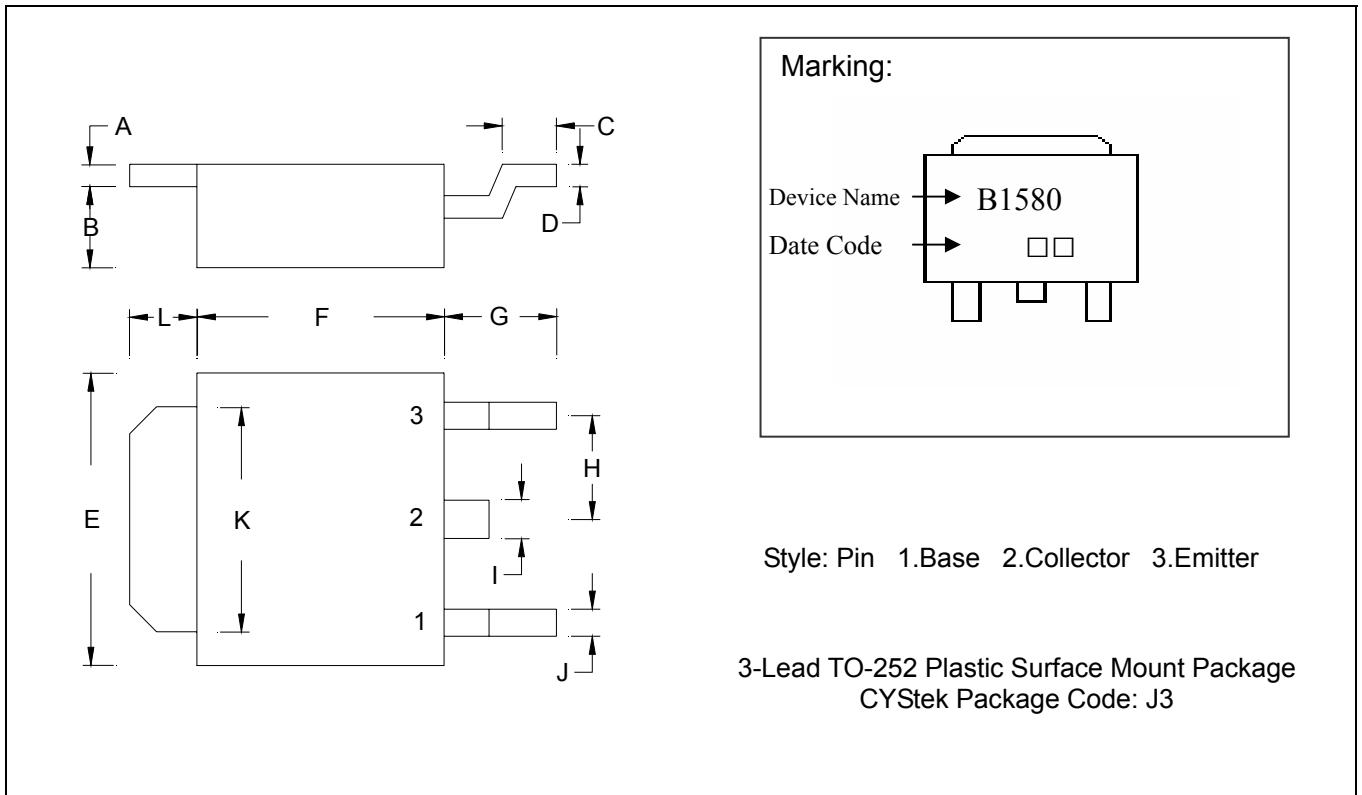
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-252 Dimension**



**Marking:**

Device Name → B1580  
 Date Code → □ □

Style: Pin 1.Base 2.Collector 3.Emitter

3-Lead TO-252 Plastic Surface Mount Package  
 CYStek Package Code: J3

\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.0866	0.1102	2.20	2.80
B	0.0650	0.0768	1.65	1.95	H	-	*0.0906	-	*2.30
C	0.0354	0.0591	0.90	1.50	I	-	0.0449	-	1.14
D	0.0177	0.0236	0.45	0.60	J	-	0.0346	-	0.88
E	0.2441	0.2677	6.20	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2125	0.2283	5.40	5.80	L	0.0551	0.0630	1.40	1.60

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: KFC; tin plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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