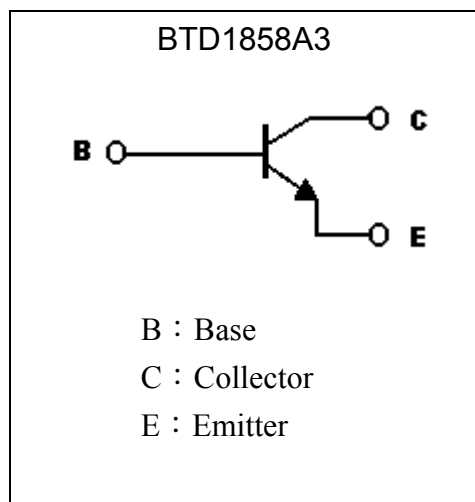
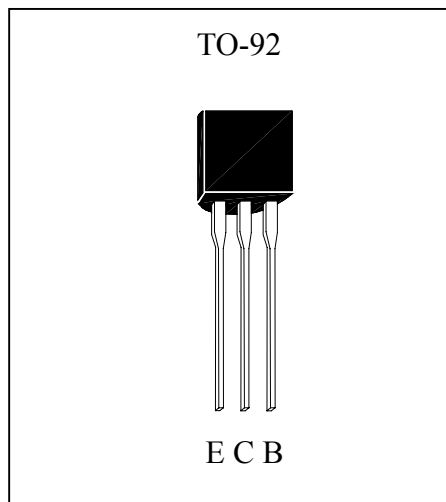


**Silicon NPN Epitaxial Planar Transistor**

# BTD1858A3

**Description**

- High  $BV_{CEO}$
- High current capability
- Pb-free package

**Symbol**

**Outline**

**Absolute Maximum Ratings** ( $T_a=25^\circ\text{C}$ )

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	$V_{CBO}$	180	V
Collector-Emitter Voltage	$V_{CEO}$	180	V
Emitter-Base Voltage	$V_{EBO}$	5	V
Collector Current (DC)	$I_C$	1.5	A
Collector Current (Pulse)	$I_{CP}$	3	A
Power Dissipation @ $T_A=25^\circ\text{C}$	$P_D$	750	mW
Junction Temperature	$T_j$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55~+150	$^\circ\text{C}$

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CB0</sub>	180	-	-	V	I <sub>C</sub> =50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	180	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	5	-	-	V	I <sub>E</sub> =50μA, I <sub>C</sub> =0
I <sub>CB0</sub>	-	-	1	μA	V <sub>CB</sub> =160V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	1	μA	V <sub>EB</sub> =4V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	0.15	0.3	V	I <sub>C</sub> =1A, I <sub>B</sub> =100mA
*V <sub>CE(sat)</sub>	-	-	0.4	V	I <sub>C</sub> =1A, I <sub>B</sub> =50mA
*V <sub>BE(on)</sub>	-	-	0.8	V	V <sub>CE</sub> =5V, I <sub>C</sub> =5mA
h <sub>FE1</sub>	180	-	560	-	V <sub>CE</sub> =5V, I <sub>C</sub> =200mA
h <sub>FE2</sub>	30	-	-	-	V <sub>CE</sub> =5V, I <sub>C</sub> =500mA
f <sub>T</sub>	-	140	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
Cob	-	27	-	pF	V <sub>CB</sub> =10V, I <sub>E</sub> =0, f=1MHz

\*Pulse Test: Pulse Width ≤380μs, Duty Cycle ≤2%

**Classification of h<sub>FE</sub> 1**

Rank	Q	R
Range	180~390	270~560

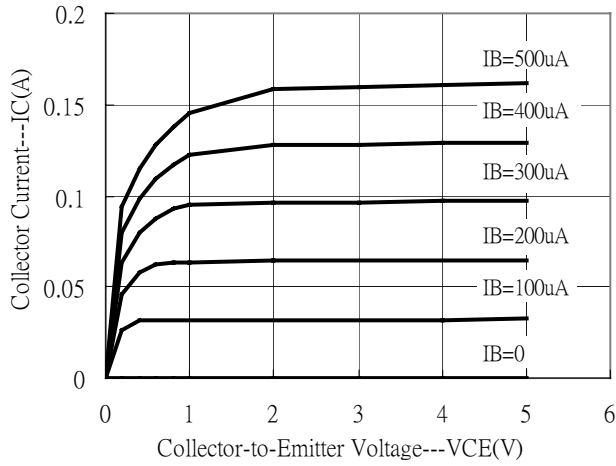
**Ordering Information**

Device	Package	Shipping	Marking
BTD1858A3	TO-92 (Pb-free)	2000 pcs / Tape & Box	D1858

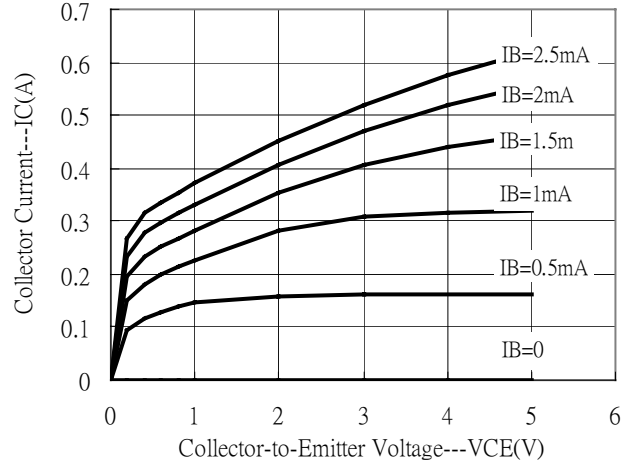


### Characteristic Curves

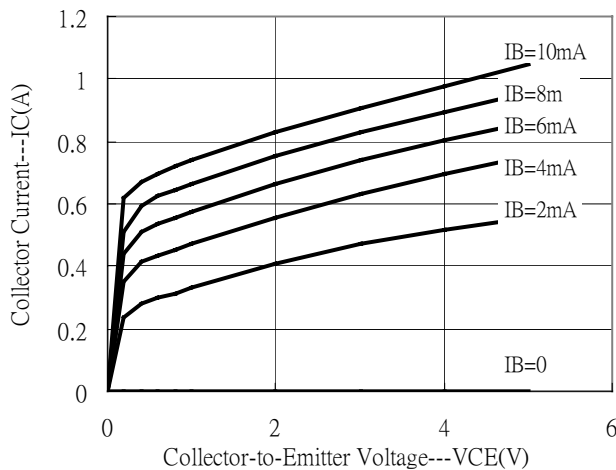
Output Characteristics



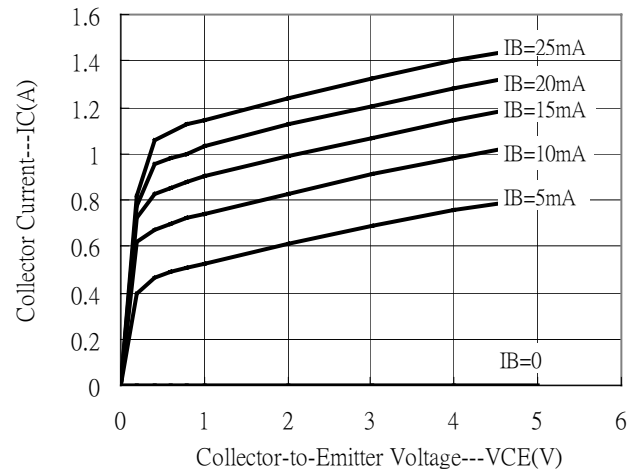
Output Characteristics



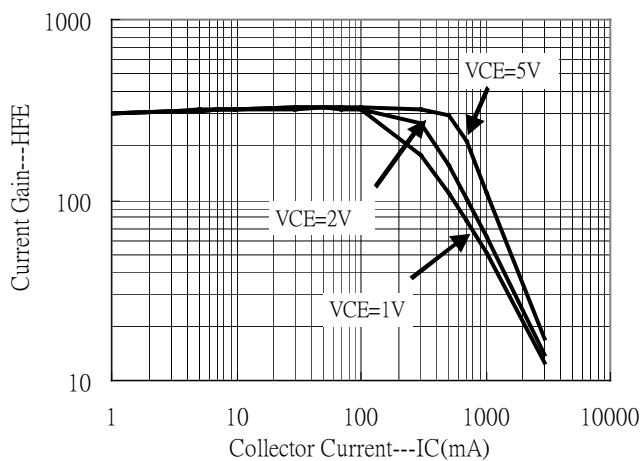
Output Characteristics



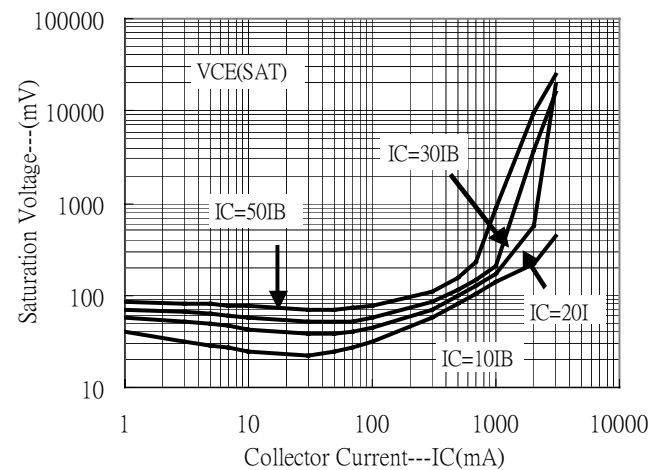
Output Characteristics



Current Gain vs Collector Current



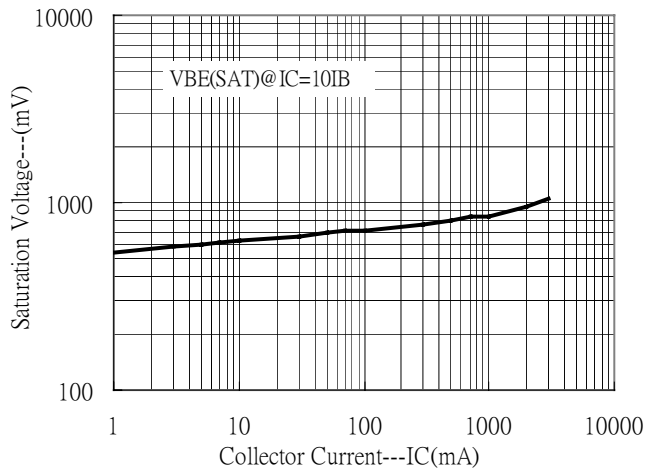
Saturation Voltage vs Collector Current



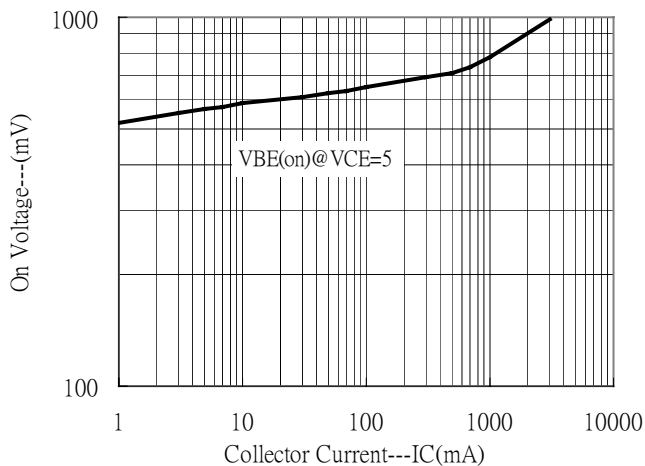


### Characteristic Curves(Cont.)

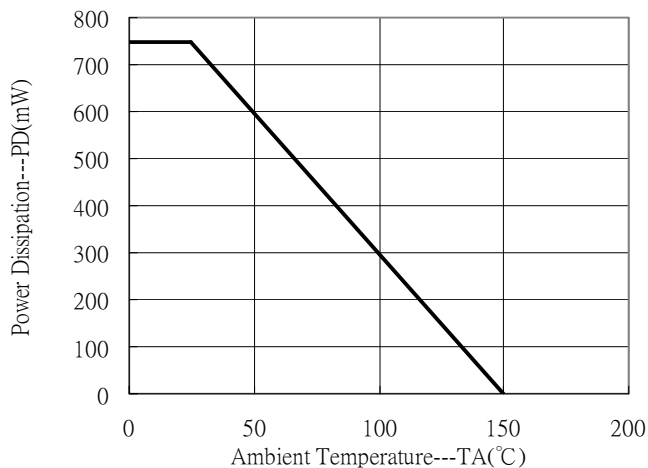
Saturation Voltage vs Collector Current



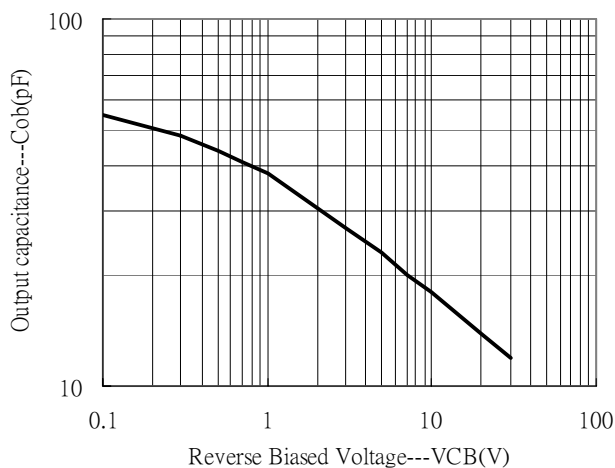
On Voltage vs Collector Current



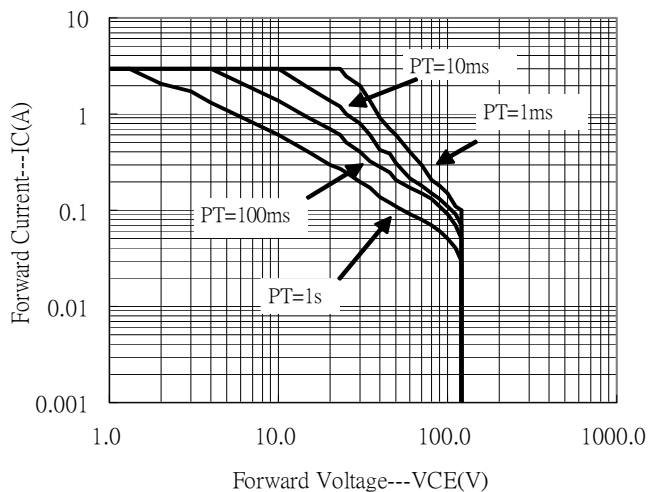
Power Derating Curve



Output Capacitance vs Reverse Biased Voltage



Safe Operating Area





**Product Designation**

BT X XXXX XX  
(1) (2) (3) (4)

(1) Indicates that transistor is bipolar

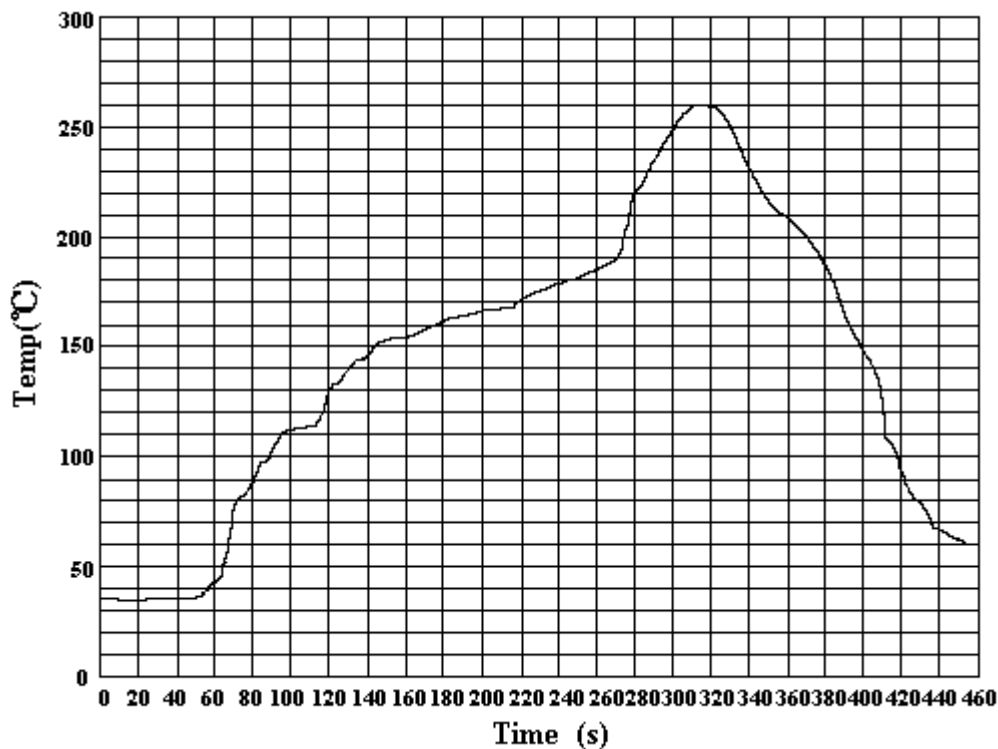
(2) Indicates polarity  
A, B . . . . PNP  
C, D . . . . NPN

(3) Indicates device random number

(4) Indicates package shape  
N3 . . . SOT-23  
A3 . . . TO-92  
E3 . . . TO-220AB  
FP . . . TO-220FP  
J3 . . . TO-252  
I3 . . . TO-251  
F3 . . . TO-263  
D3 . . . TO-126ML  
T3 . . . TO-126  
L3 . . . SOT-223  
M3 . . . SOT-89  
S3 . . . SOT-323

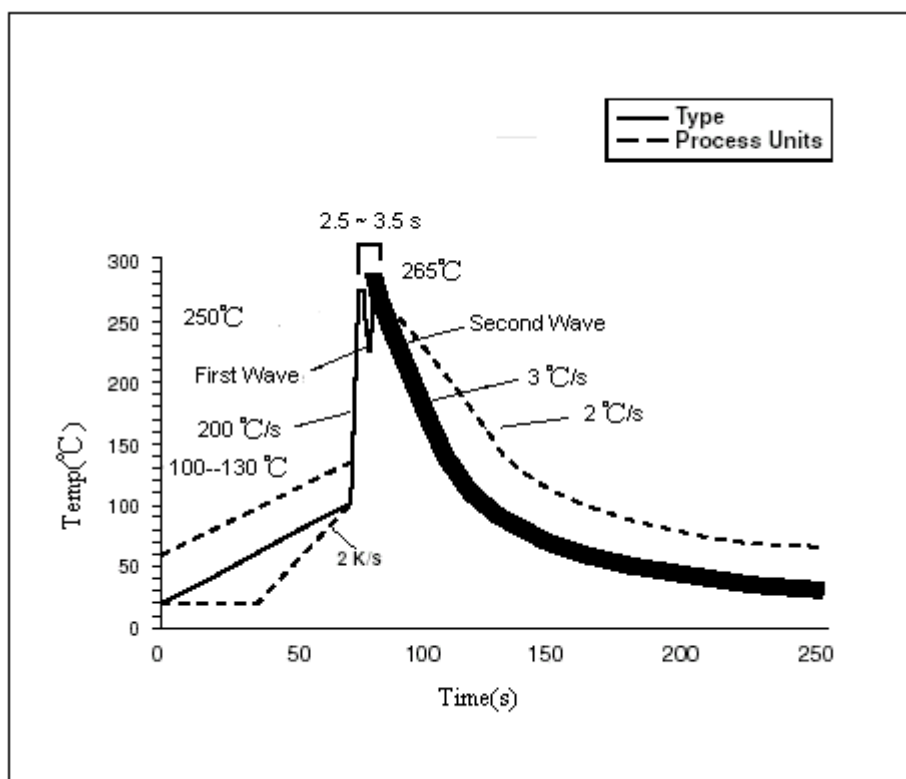


### Recommended IR reflow profile



Average ramp-up rate(25 to 150°C)	1~4 °C/second
Preheat temperature 150~180°C	60~90 seconds
Temperature maintained above 220°C	30 seconds min.
Time within 5°C of actual peak temperature	3~5 seconds
Peak temperature range	255+0/-5°C
Ramp-down rate	2~10 °C/second
Time 25°C to peak temperature	6 minutes max.

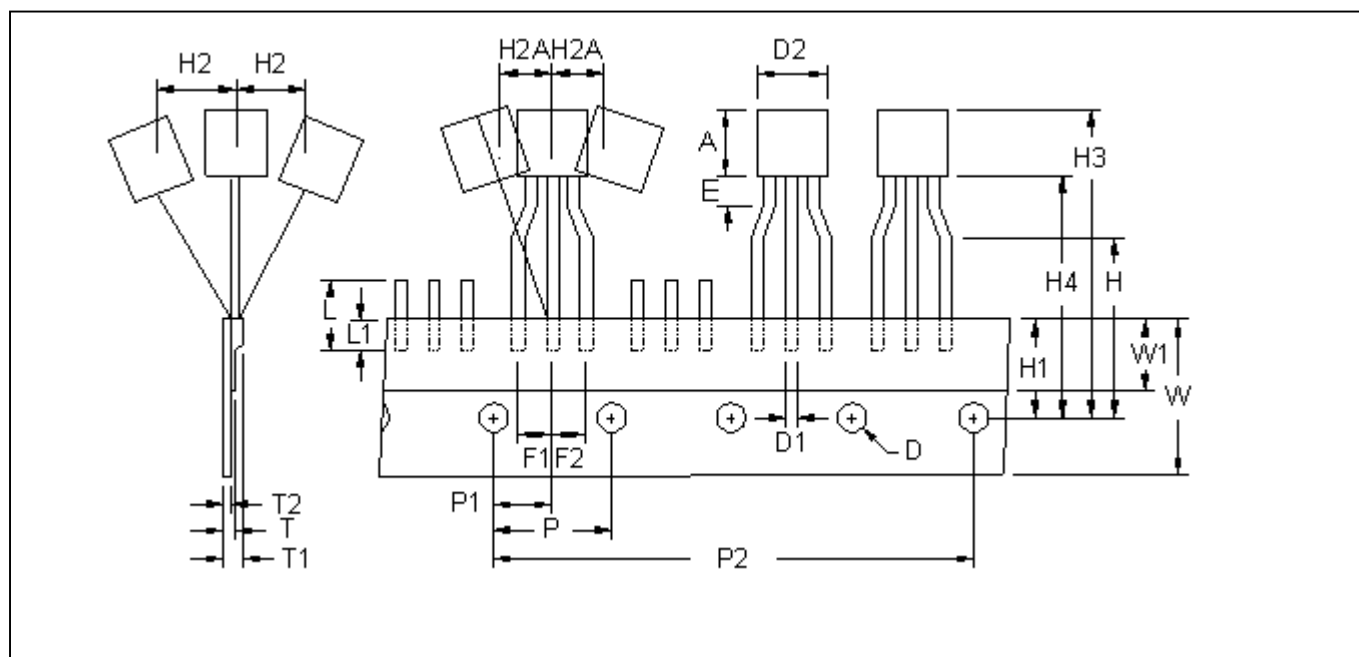
Recommended temperature profile for wave soldering



Recommendation:

1. Preheat temperature at solder side must be between 100 and 130 °C for 80 to 100 seconds.
2. Temperature ramp-up rate : 1~2 °C/s
3. The temperature gradient between preheat and wave soldering must be smaller than +100 °C.
4. Terminations must go through the wave simultaneously.
5. Travel through the wave from 255 to 260°C for 2.5 to 3.5 seconds
6. Temperature ramp-down rate : 2~3 °C/s

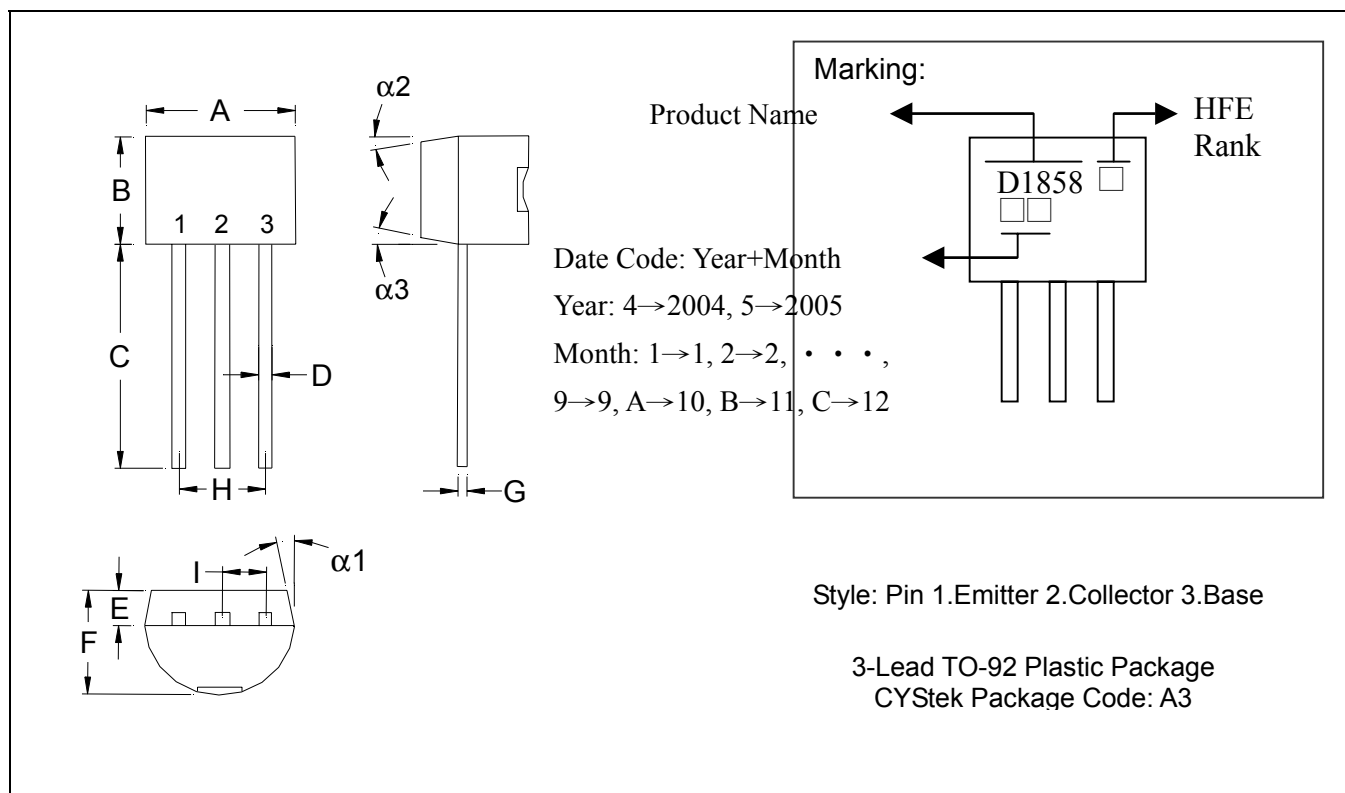
**TO-92 Taping Outline**



DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
E		1.5	2.0
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255



**TO-92 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	$\alpha 1$	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	$\alpha 2$	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	$\alpha 3$	-	*2°	-	*2°

Notes: 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: 42 Alloy ; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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