

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90390 Series

### MB90394HA/F394H/F394HA/ MB90V390H/V390HA/V390HB

#### ■ DESCRIPTION

The MB90390-series with up to five FULL-CAN\* interfaces and Flash ROM is especially designed for automotive and industrial applications. Its main features are up to five on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35 μm CMOS technology, Fujitsu now offers on-chip Flash-ROM program memory up to 512 Kbytes. An internal voltage booster removes the necessity for a second programming voltage.

An on-board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features 6 Stepper Motor Controllers with slew rate controlled high current outputs.

Furthermore, it features an 8-channel Output Compare Unit and a 6-channel Input Capture Unit with two separate 16-bit free running timers. Up to 4 UARTs constitute additional functionality for communication purposes.

\* : Controller Area Network (CAN) - License of Robert Bosch GmbH

Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

URL : <http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

# MB90390 Series

## ■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 42 ns instruction execution time)
- New 0.35  $\mu\text{m}$  CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- Up to five FULL-CAN interfaces; conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 8 external interrupts)
- EI<sup>2</sup>OS - Automatic transfer function indep.of CPU; 16 channels of intelligent I/O Services
- 18-bit Time-base counter
- Watchdog Timer
- 2 full duplex UARTs; support 10.4 Kbps (USA standard )
- Up to 2 full duplex UARTs (LIN/SCI)
- Serial I/O : 1 channel for synchronous data transfer
- Optional I<sup>2</sup>C\* with 400 Kbps
- A/D Converter : 15 channels analog inputs (Resolution 10 bits or 8 bits)
- 16-bit reload timer  $\times$  2 channels
- ICU (Input capture) 16-bit  $\times$  6 channels (2 input pins are shared with OCU outputs)
- OCU (Output capture) 16-bit  $\times$  8 channels (2 output pins are shared with ICU input pins)
- 16-bit free running timer  $\times$  2 channels (FRT0 : ICU 0/1, OCU 0/1/2/3, FRT1 : ICU 2/3/4/5, OCU 4/5/6/7)
- 8/16-bit Programmable Pulse Generator 6 channels  $\times$  16-bit/12 channels  $\times$  8-bit
- Stepping Motor Controller 6 channels with slew rate controlled high current outputs
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16-bit  $\times$  16-bit) and divide (32-bit/16-bit) instructions available
- Program Patch Function
- Fast Interrupt processing
- Low Power Consumption mode
  - Sleep mode
  - Timebase timer mode
  - Stop mode
  - CPU intermittent mode
- Sound Generator
- Real Time Watch Timer
- Built-In Clock Modulation circuit
- Programmable input levels (Automotive Hysteresis / CMOS Hysteresis, initial level is Automotive Hysteresis)
- Package : 120-pin plastic LQFP

\* : Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

# MB90390 Series

## ■ PRODUCT LINEUP

Part Number Parameter	MB90394HA	MB90F394H MB90F394HA	MB90V390H	MB90V390HA/ MB90V390HB
CPU	F <sup>2</sup> MC-16LX CPU			
System clock	On-chip PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)			
ROM	ROM memory 384 Kbytes	Boot-block Flash memory 384 Kbytes Hard-wired reset vector, points to address FFA000 <sub>H</sub>	External	
RAM	10 Kbytes		16 Kbytes	30 Kbytes
Emulator-specific power supply*1	—		Yes	
Technology	0.35 μm CMOS with on-chip voltage regulator for internal power supply	0.35 μm CMOS with on-chip voltage regulator for internal power supply + Flash memory with On-chip charge pump for programming voltage	0.35 μm CMOS with on-chip voltage regulator for internal power supply	
Operating voltage range	3.5 V to 5.5 V (4.0 V to 5.5 V: during Flash programming and erasing, 4.5 V to 5.5 V: if A/D Converter is used)		5 V ± 10%	
Temperature range	-40 °C to +85 °C		—	
Package	LQFP-120		PGA-299	
UART (2 channels)	Full duplex double buffer Supports asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 24 MHz			
UART (LIN/SCI)	1 channel			2 channels
I <sup>2</sup> C (400 Kbps)	1 channel	—	1 channel	
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 24 MHz			
A/D Converter	15 input channels 10-bit or 8-bit resolution Conversion time : Min 4.9 μs include sample time (per one channel, depends on machine clock frequency)			
16-bit Reload Timer (2 channels)	Operation clock frequency : f <sub>sys</sub> /2 <sup>1</sup> , f <sub>sys</sub> /2 <sup>3</sup> , f <sub>sys</sub> /2 <sup>5</sup> (f <sub>sys</sub> = System clock frequency) Supports External Event Count function			

(Continued)

# MB90390 Series

Part Number Parameter	MB90394HA	MB90F394H MB90F394HA	MB90V390H	MB90V390HA/ MB90V390HB
Watch Timer	Directly operates with the oscillation clock Read/Write accessible Second/Minute/Hour registers Signals interrupts			
16-bit I/O Timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ , $f_{sys}/2^5$ , $f_{sys}/2^6$ , $f_{sys}/2^7$ ( $f_{sys}$ = System clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 2/3/4/5, OCU 4/5/6/7			
16-bit Output Compare (8 channels)	Signals an interrupt when a match with 16-bit I/O Timer Eight 16-bit compare registers. A pair of compare registers can be used to generate an output signal. OCU 6/7 outputs are shared with ICU 3/5 inputs			
16-bit Input Capture (6 channels)	Rising edge, falling edge or rising & falling edge sensitive Six 16-bit Capture registers Signals an interrupt upon external event ICU 3/5 inputs are shared with OCU 6/7 outputs			
8/16-bit Programmable Pulse Generator (6 channels)	Supports 8-bit and 16-bit operation modes Twelve 8-bit reload counters Twelve 8-bit reload registers for L pulse width Twelve 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ or 102.4 $\mu$ s at $f_{osc}$ = 5 MHz ( $f_{sys}$ = System clock frequency, $f_{osc}$ = Oscillation clock frequency)			
CAN Interface (up to 5 channels)	2 channels		5 channels	
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full-bit compare/Full-bit mask/Two partial bit masks Supports up to 1 Mbps MB90F394H, MB90V390H, MB90V390HA : Do not use CAN message buffer RAM and clock modulator at the same time.			
Stepping Motor Controller (6 channels)	Four high current outputs with controlled slew rate for each channel Synchronized two 8-bit PWM's for each channel			
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive			
Sound Generator	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM frequency : 62.5 kHz, 31.2 kHz, 15.6 kHz, 7.8 kHz at System clock = 16 MHz Tone frequency : $PWM\ frequency/2$ (reload value + 1)			

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# MB90390 Series

(Continued)

Part Number Parameter	MB90394HA	MB90F394H MB90F394HA	MB90V390H	MB90V390HA/ MB90V390HB
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal Port-wise programmable as CMOS Hysteresis or automotive Hysteresis inputs (default)			
Clock Modulator	Spread spectrum clock modulator for reducing electromagnetic emissions. Frequency and Phase Modulation modes. MB90F394H : Do not use frequency modulation. MB90F394H, MB90V390H, MB90V390HA : Do not use CAN message buffer RAM and clock modulator at the same time.			
Flash Memory	—	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years*3 Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage	—	—

\*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.  
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

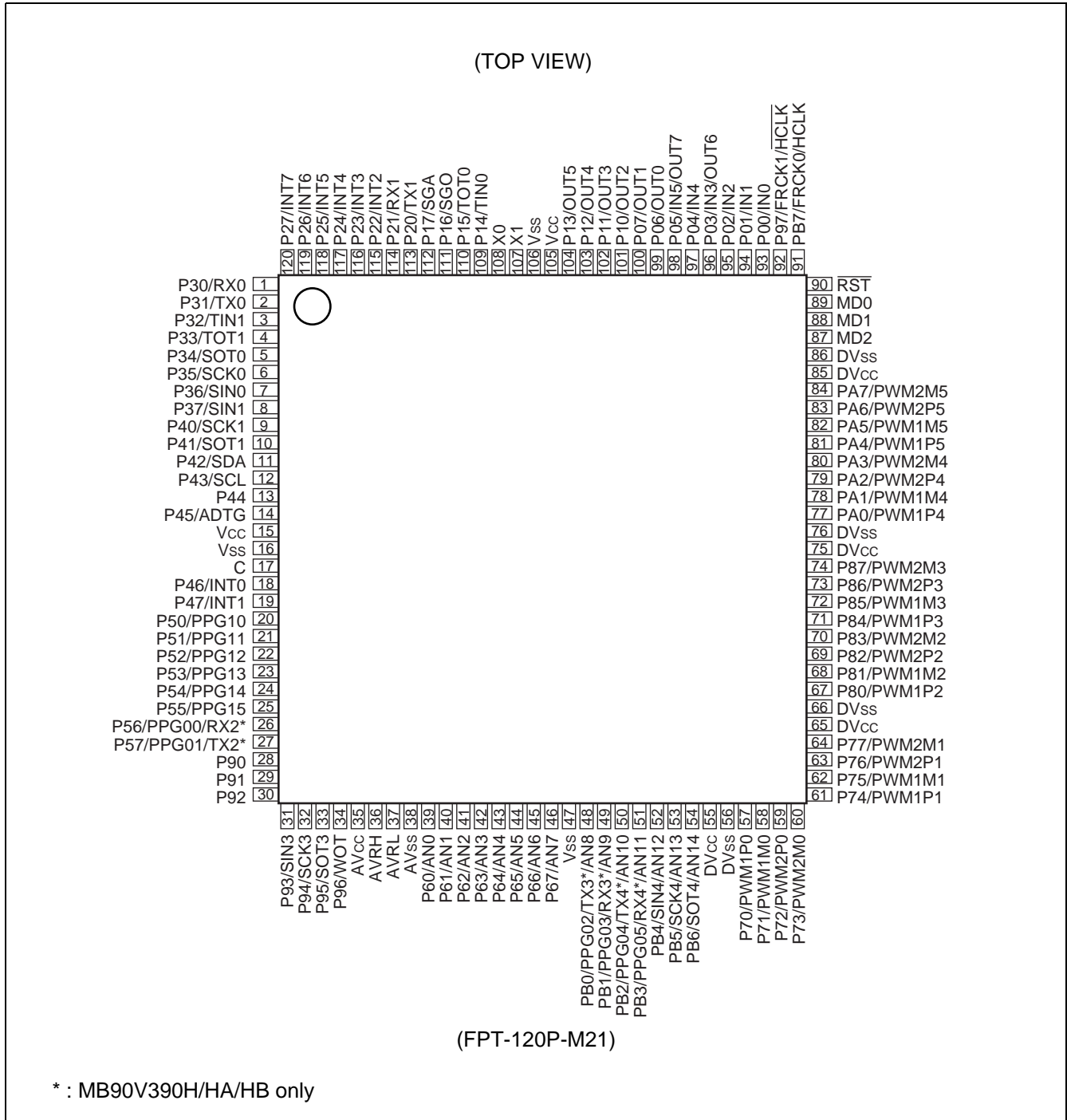
\*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

\*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

# MB90390 Series

## PIN ASSIGNMENTS

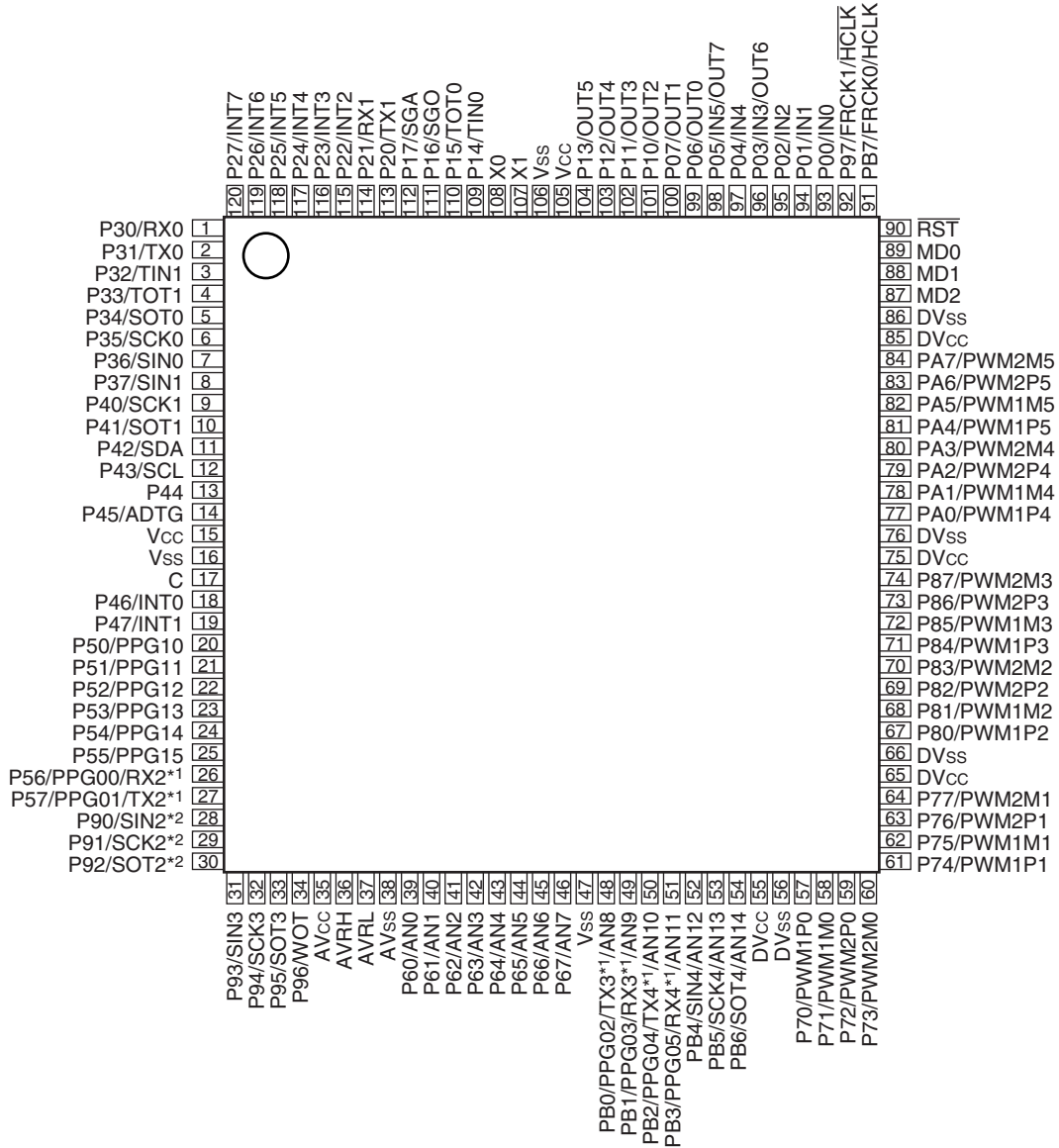
- MB90V390H



# MB90390 Series

- MB90V390HA/MB90V390HB

(TOP VIEW)



(FPT-120P-M21)

\*1 : MB90V390H/HA/HB only

\*2 : MB90V390HA/HB only





## ■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type*	Function
107	X1	A	Oscillation output
108	X0		Oscillation input
90	$\overline{RST}$	B	Reset input
93 to 95	P00 to P02	D	General purpose I/O
	IN0 to IN2		Inputs for the Input Captures 0 to 2
96	P03	D	General purpose I/O
	IN3		Input for the Input Capture 3
	OUT6		Output for the Output Compare 6
97	P04	D	General purpose I/O
	IN4		Input for the Input Capture 4
98	P05	D	General purpose I/O
	IN5		Input for the Input Capture 5
	OUT7		Output for the Output Compare 7
99 to 104	P06, P07, P10 to P13	D	General purpose I/O
	OUT0 to OUT5		Outputs for the Output Compares 0 to 5
109	P14	D	General purpose I/O
	TIN0		TIN0 input for the 16-bit Reload Timer 0
110	P15	D	General purpose I/O
	TOT0		TOT0 output for the 16-bit Reload Timer 0
111	P16	D	General purpose I/O
	SGO		SGO output for the Sound Generator
112	P17	D	General purpose I/O
	SGA		SGA output for the Sound Generator
113	P20	D	General purpose I/O
	TX1		TX output for CAN Interface 1
114	P21	D	General purpose I/O
	RX1		RX input for CAN Interface 1
115 to 120	P22 to P27	D	General purpose I/O
	INT2 to INT7		External interrupt inputs for INT2 to INT7
1	P30	D	General purpose I/O
	RX0		RX input for CAN Interface 0
2	P31	D	General purpose I/O
	TX0		TX output for CAN Interface 0

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# MB90390 Series

Pin no.	Pin name	Circuit type*	Function
3	P32	D	General purpose I/O
	TIN1		TIN1 input for the 16-bit Reload Timer 1
4	P33	D	General purpose I/O
	TOT1		TOT1 output for the 16-bit Reload Timer 1
5	P34	D	General purpose I/O
	SOT0		SOT output for UART 0
6	P35	D	General purpose I/O
	SCK0		SCK I/O for UART 0
7	P36	D	General purpose I/O
	SIN0		SIN input for UART 0
8	P37	D	General purpose I/O
	SIN1		SIN input for UART 1
9	P40	D	General purpose I/O
	SCK1		SCK I/O for UART 1
10	P41	D	General purpose I/O
	SOT1		SOT output for UART 1
11	P42	D	General purpose I/O
	SDA		Serial data for I <sup>2</sup> C interface (except MB90F394H(A))
12	P43	D	General purpose I/O
	SCL		Serial clock for I <sup>2</sup> C interface (except MB90F394H(A))
13	P44	D	General purpose I/O
14	P45	D	General purpose I/O
	ADTG		External trigger input of the A/D Converter
18, 19	P46, P47	D	General purpose I/O
	INT0, INT1		External interrupt inputs for INT0 to INT1
20 to 25	P50 to P55	D	General purpose I/O
	PPG10 to PPG15		Outputs for the Programmable Pulse Generators 10 to 15
26	P56	D	General purpose I/O
	PPG00		Output for the Programmable Pulse Generator 0
	RX2		RX input for CAN Interface 2 (only MB90V390H/HA/HB)
27	P57	D	General purpose I/O
	PPG01		Output for the Programmable Pulse Generator 1
	TX2		TX output for CAN Interface 2 (only MB90V390H/HA/HB)
28	P90	D	General purpose I/O
	SIN2		SIN input for UART 2 (only MB90V390HA/HB)

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# MB90390 Series

Pin no.	Pin name	Circuit type*	Function
29	P91	D	General purpose I/O
	SCK2		SCK input/output for UART 2 (only MB90V390HA/HB)
30	P92	D	General purpose I/O
	SOT2		SOT output for UART 2 (only MB90V390HA/HB)
31	P93	D	General purpose I/O
	SIN3		SIN input for UART 3 (LIN/SCI)
32	P94	D	General purpose I/O
	SCK3		SCK input/output for UART 3 (LIN/SCI)
33	P95	D	General purpose I/O
	SOT3		SOT output for UART 3 (LIN/SCI)
34	P96	D	General purpose I/O
	WOT		WOT output for the Watch Timer
39 to 46	P60 to P67	E	General purpose I/O
	AN0 to AN7		Inputs for the A/D Converter
48	PB0	E	General purpose I/O
	PPG02		Output for the Programmable Pulse Generator 2
	TX3		TX output for CAN Interface 3 (only MB90V390H/HA/HB)
	AN8		Input for the A/D Converter
49	PB1	E	General purpose I/O
	PPG03		Output for the Programmable Pulse Generator 3
	RX3		RX input for CAN Interface 3 (only MB90V390H/HA/HB)
	AN9		Input for the A/D Converter
50	PB2	E	General purpose I/O
	PPG04		Output for the Programmable Pulse Generator 4
	TX4		TX output for CAN Interface 4 (only MB90V390H/HA/HB)
	AN10		Input for the A/D Converter
51	PB3	E	General purpose I/O
	PPG05		Output for the Programmable Pulse Generator 5
	RX4		RX input for CAN Interface 4 (only MB90V390H/HA/HB)
	AN11		Input for the A/D Converter
52	PB4	E	General purpose I/O
	SIN4		SIN input for the Serial I/O
	AN12		Input for the A/D Converter

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# MB90390 Series

Pin no.	Pin name	Circuit type*	Function
53	PB5	E	General purpose I/O
	SCK4		SCK input/output for the Serial I/O
	AN13		Input for the A/D Converter
54	PB6	E	General purpose I/O
	SOT4		SOT output for the Serial I/O
	AN14		Input for the A/D Converter
57 to 60	P70 to P73	F	General purpose I/O
	PWM1P0 PWM1M0 PWM2P0 PWM2M0		Output for Stepping Motor Controller channel 0
61 to 64	P74 to P77	F	General purpose I/O
	PWM1P1 PWM1M1 PWM2P1 PWM2M1		Output for Stepping Motor Controller channel 1
67 to 70	P80 to P83	F	General purpose I/O
	PWM1P2 PWM1M2 PWM2P2 PWM2M2		Output for Stepping Motor Controller channel 2
71 to 74	P84 to P87	F	General purpose I/O
	PWM1P3 PWM1M3 PWM2P3 PWM2M3		Output for Stepping Motor Controller channel 3
77 to 80	PA0 to PA3	F	General purpose I/O
	PWM1P4 PWM1M4 PWM2P4 PWM2M4		Output for Stepping Motor Controller channel 4
81 to 84	PA4 to PA7	F	General purpose I/O
	PWM1P5 PWM1M5 PWM2P5 PWM2M5		Output for Stepping Motor Controller channel 5
91	PB7	D	General purpose I/O
	FRCK0		FRCK0 input for the 16-bit I/O Timer 0
	HCLK		Oscillation Clock output

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# MB90390 Series

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Pin no.	Pin name	Circuit type*	Function
92	P97	D	General purpose I/O
	FRCK1		FRCK1 input for the 16-bit I/O Timer 1
	$\overline{\text{HCLK}}$		Inverted Oscillation Clock output
55 65 75 85	DVcc	—	Dedicated power supply pins for the high current output buffers (Pin No. 57 to 84)
56 66 76 86	DVss	—	Dedicated ground pins for the high current output buffers (Pin No. 57 to 84)
35	AVcc	—	Dedicated power supply pin (5 V) for the A/D converter
36	AVRH	—	Dedicated pos. reference voltage pin for the A/D converter
37	AVRL	—	Dedicated neg. reference voltage pin for the A/D converter
38	AVss	—	Dedicated power supply pin (0 V) for the A/D converter
88, 89	MD1, MD0	C	These are input pins used to designate the operating mode. They should be connected directly to Vcc or Vss.
87	MD2	G	This is an input pin used to designate the operating mode. It should be connected directly to Vcc or Vss.
15 105	Vcc	—	These are power supply (5 V) input pins
16 47 106	Vss	—	These are power supply (0 V) input pins
17	C	—	This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 $\mu\text{F}$ (MB90394HA/MB90F394H(A)/MB90V390H)/0.22 $\mu\text{F}$ (MB90V390HA/HB) ceramic capacitor.

\* : Refer to "■ I/O CIRCUIT TYPE" for I/O circuit type.

# MB90390 Series

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<p>Oscillation feedback resistor : 1 M<math>\Omega</math> approx.</p>
B		<ul style="list-style-type: none"> <li>• CMOS Hysteresis input with pull-up Resistor : 50 k<math>\Omega</math> approx.</li> </ul>
C		<ul style="list-style-type: none"> <li>• EVA/ROM device : CMOS Hysteresis input</li> <li>• Flash device : CMOS input.</li> </ul>
D		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS Hysteresis input</li> <li>• Automotive Hysteresis input</li> </ul> <p>Note : The input characteristic may be different for different pins/devices. Refer to <math>V_{IHs}</math> in "■ ELECTRICAL CHARACTERISTICS 3.DC Characteristics"</p>

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Type	Circuit	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS Hysteresis input</li> <li>• Automotive Hysteresis input</li> <li>• Analog input</li> </ul> <p>Note : The input characteristic may be different for different pins/devices. Refer to <math>V_{IHS}</math> in "■ ELECTRICAL CHARACTERISTICS 3.DC Characteristics"</p>
F		<ul style="list-style-type: none"> <li>• CMOS high current output</li> <li>• CMOS Hysteresis input</li> <li>• Automotive Hysteresis input</li> </ul>
G		<ul style="list-style-type: none"> <li>• EVA/ROM device : CMOS Hysteresis input with pull-down Resistor : 50 kΩ approx.</li> <li>• Flash device : CMOS input without pull-down.</li> </ul>

## ■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins ( $V_{CC}/V_{SS}$ )
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter if A/D Converter is unused.
- Notes on Energization
- Caution on Operations during PLL Clock Mode

### 1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AV_{RH}$ ) exceed the digital power-supply voltage.

### 2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified  $V_{CC}$  supply voltage operating range. Therefore, the  $V_{CC}$  supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that  $V_{CC}$  ripple variations (peak-to-peak values) at commercial frequencies (50/60 Hz) fall below 10% of the standard  $V_{CC}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

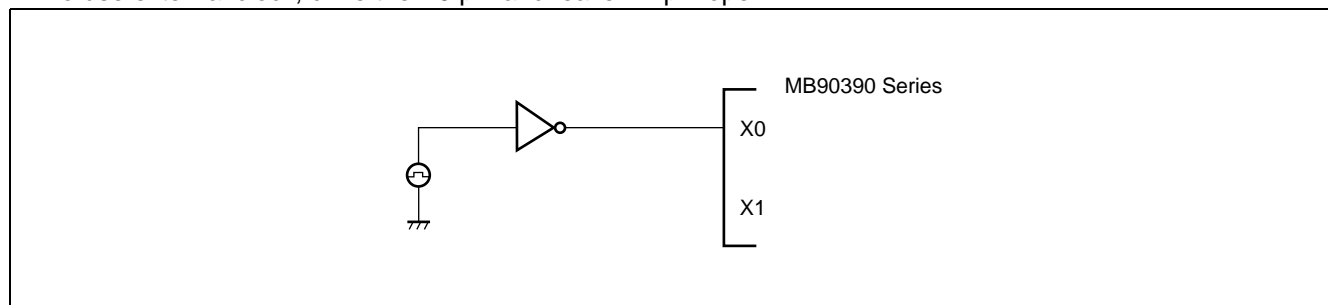
### 3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k $\Omega$  .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### 4. Using external clock

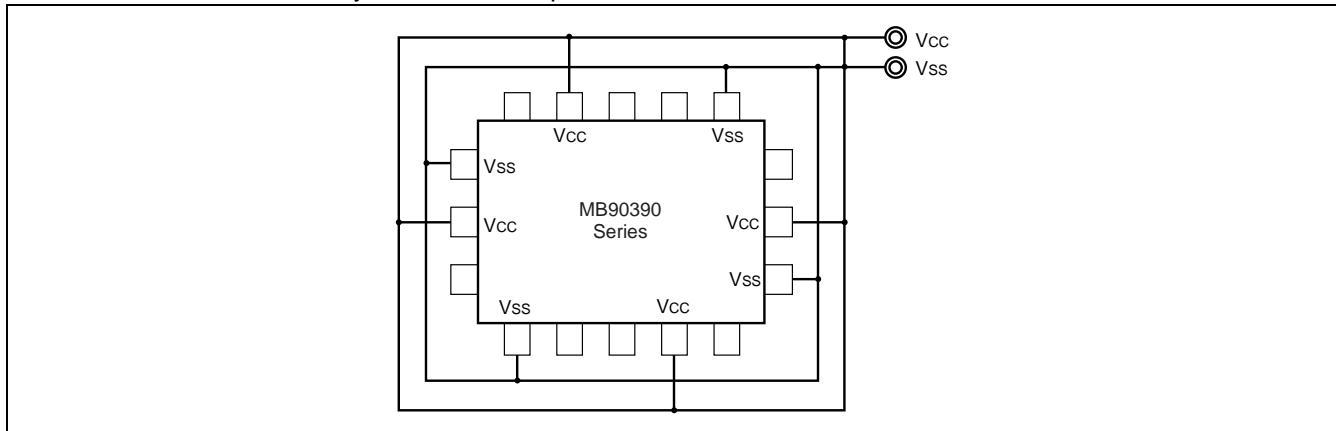
To use external clock, drive the X0 pin and leave X1 pin open.





## 5. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.  
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally.
- Connect  $V_{CC}$  and  $V_{SS}$  to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about  $0.1 \mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



## 6. Pull-up/down resistors

The MB90390 Series does not support internal pull-up/down resistors. Use external components where needed.

## 7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

## 8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ( $AV_{CC}$ ,  $AV_{RH}$ ,  $AV_{RL}$ ) and analog inputs ( $AN0$  to  $AN14$ ) after turning-on the digital power supply ( $V_{CC}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed  $AV_{RH}$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 9. Connection of Unused Pins of A/D Converter if A/D Converter is unused

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$ .

## 10. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at  $50$  or more  $\mu\text{s}$  ( $0.2 \text{ V}$  to  $2.7 \text{ V}$ ).

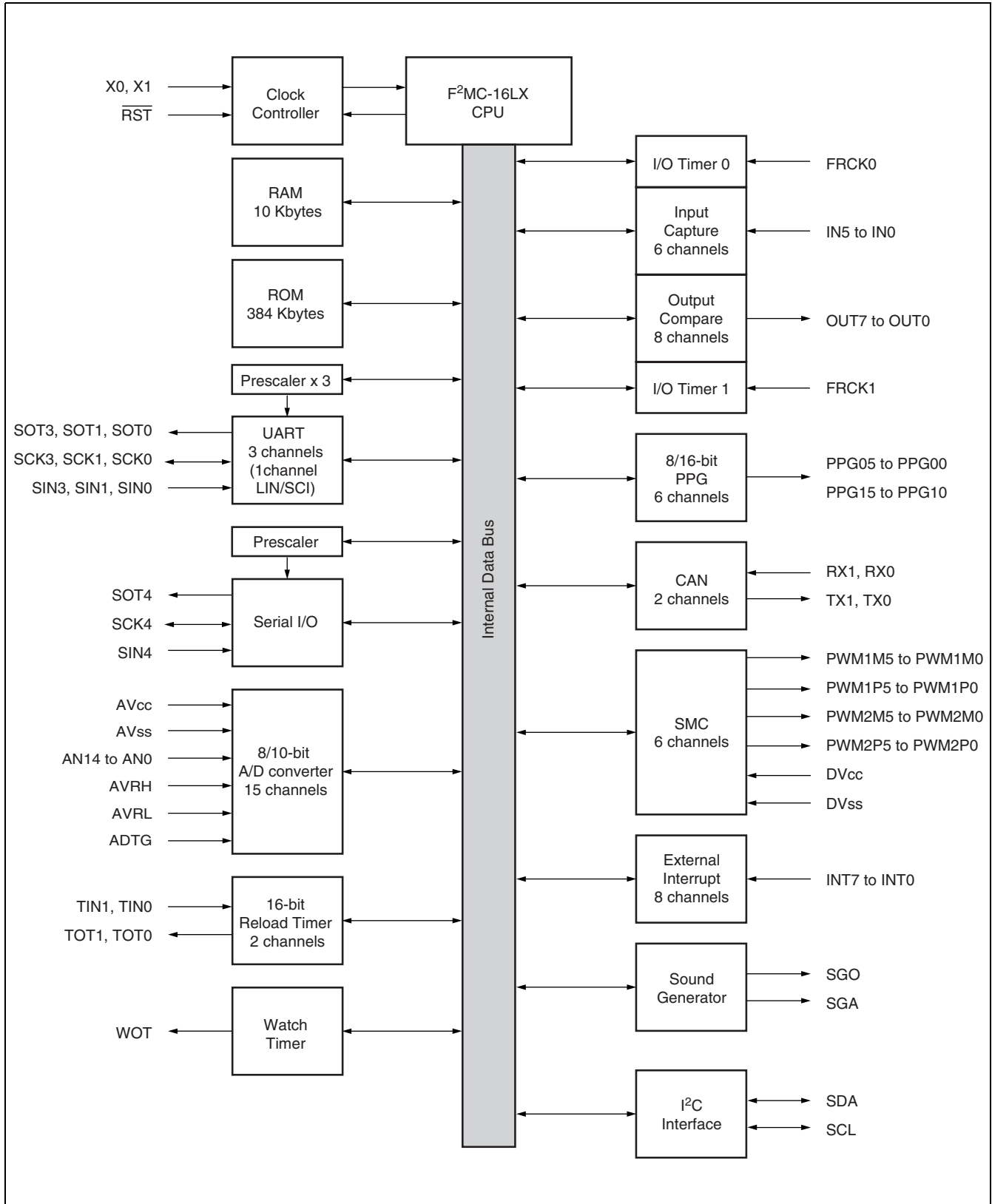
## 11. Notes on During Operation of PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

# MB90390 Series

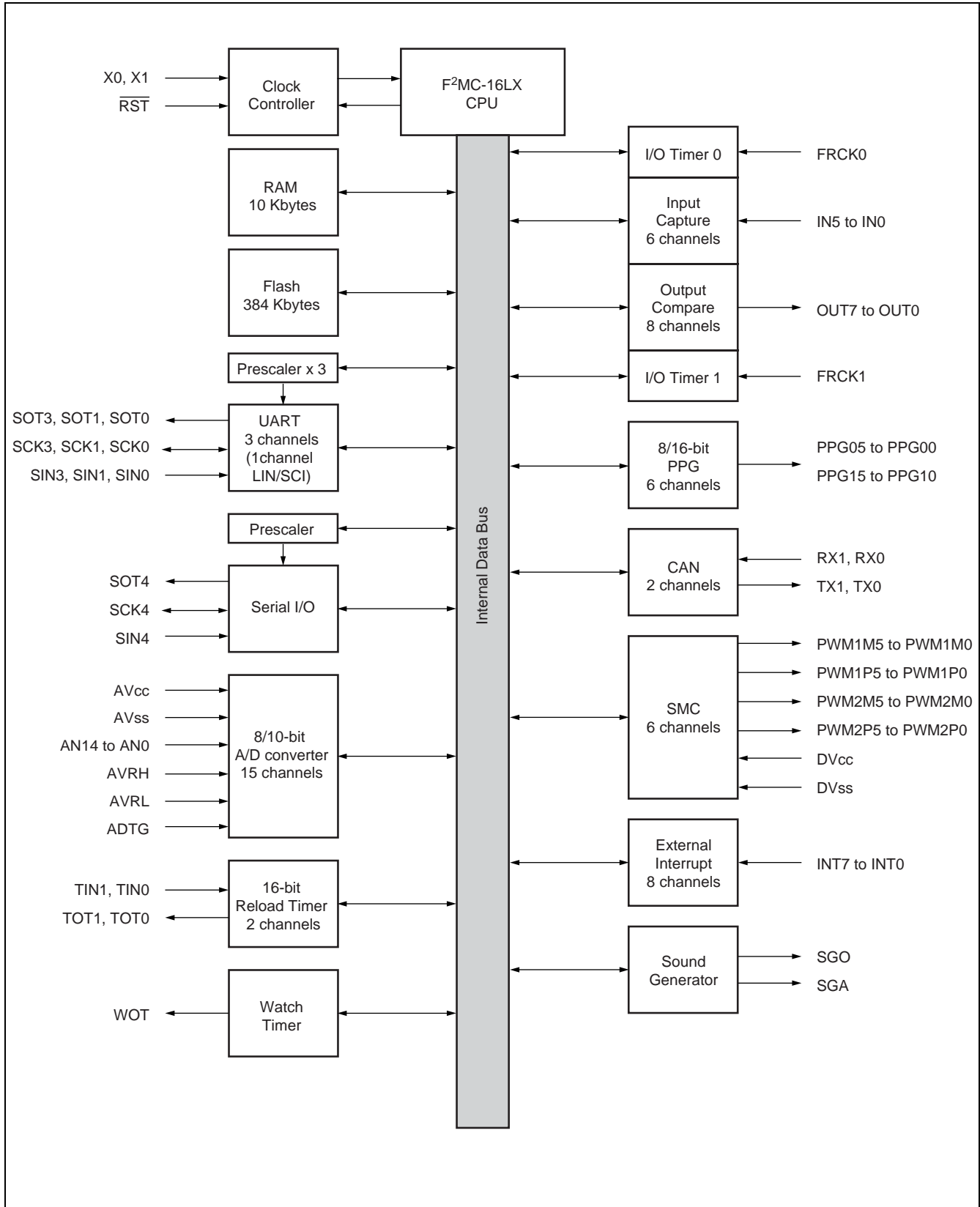
## ■ BLOCK DIAGRAMS

### • MB90394HA



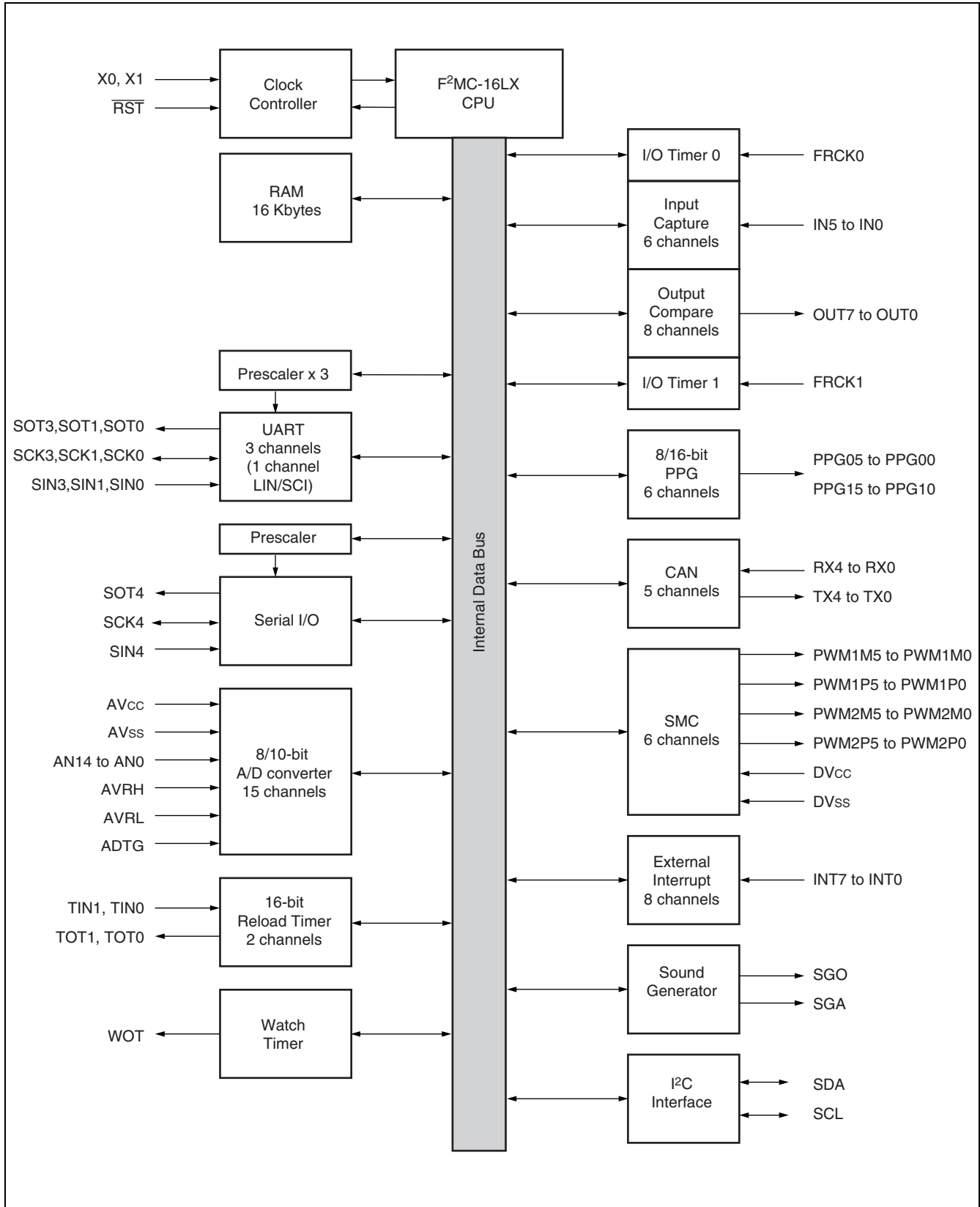
# MB90390 Series

## • MB90F394H/MB90F394HA



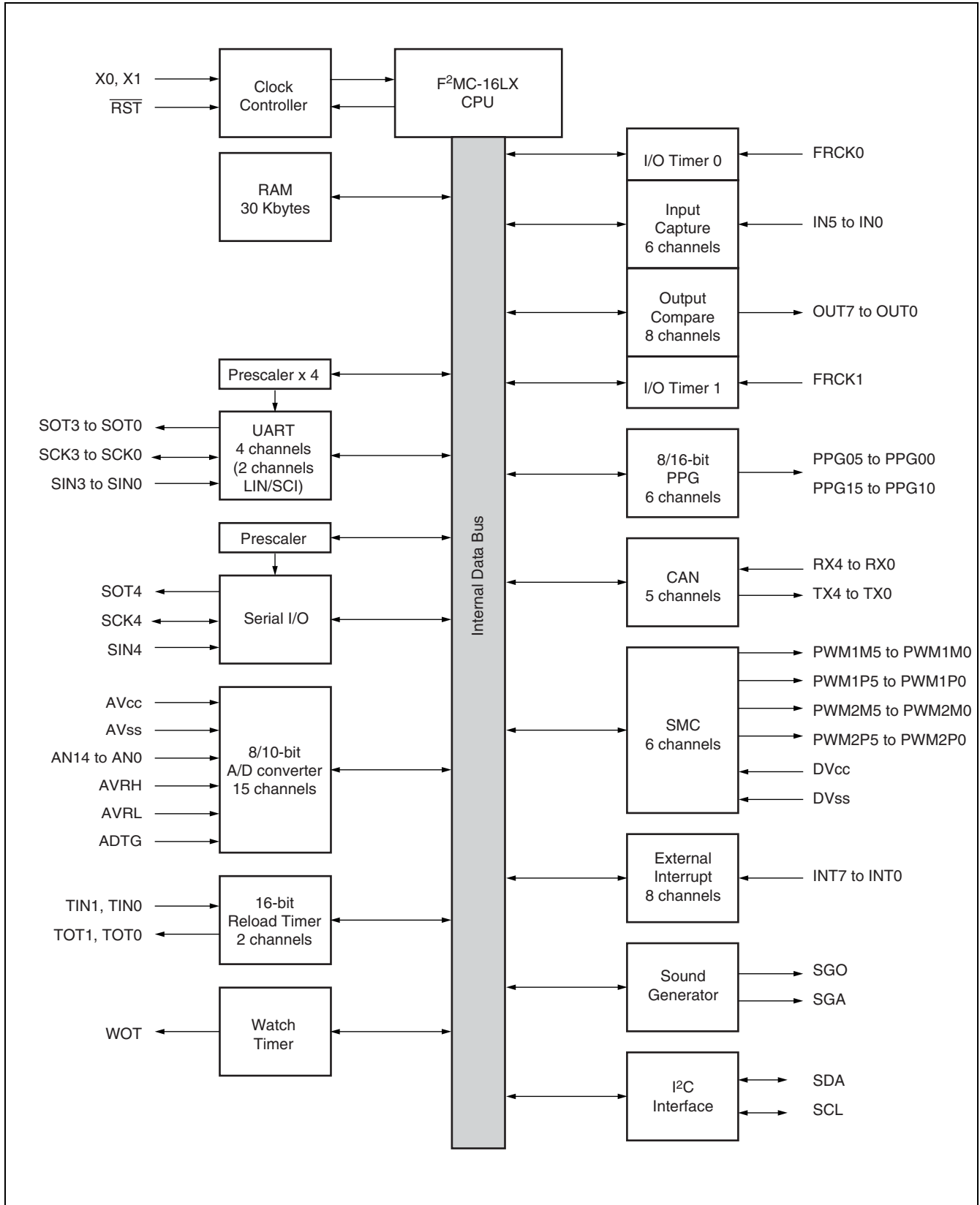
# MB90390 Series

## • MB90V390H



# MB90390 Series

## • MB90V390HA/MB90V390HB



# MB90390 Series

## MEMORY MAP

MB90394HA/ F394H(A)		MB90V390HA/HB		MB90V390H	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)
FF0000H		FF0000H		FF0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)
FE0000H		FE0000H		FE0000H	
FDFFFFH	ROM (FD bank)	FDFFFFH	ROM (FD bank)	FDFFFFH	ROM (FD bank)
FD0000H		FD0000H		FD0000H	
FCFFFFH		FCFFFFH	ROM (FC bank)	FCFFFFH	ROM (FC bank)
FC0000H		FC0000H		FC0000H	
FBFFFFH	ROM (FB bank)	FBFFFFH	ROM (FB bank)	FBFFFFH	ROM (FB bank)
FB0000H		FB0000H		FB0000H	
FAFFFFH	ROM (FA bank)	FAFFFFH	ROM (FA bank)	FAFFFFH	ROM (FA bank)
FA0000H		FA0000H		FA0000H	
F9FFFFH	ROM (F9 bank)	F9FFFFH	ROM (F9 bank)	F9FFFFH	ROM (F9 bank)
F90000H		F90000H		F90000H	
		F8FFFFH	ROM (F8 bank)	F8FFFFH	ROM (F8 bank)
		F80000H		F80000H	
		8017FFH			
		800000H	RAM 6 Kbytes		
00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)
004000H		008000H		008000H	
or		0070FFH			
008000H		004100H	RAM 12 Kbytes	0050FFH	RAM 4 Kbytes
				004100H	
003FFFH		003FFFH		003FFFH	
	Periperal		Periperal		Periperal
003500H		003500H		003500H	
0028FFH		0030FFH		0030FFH	
	RAM 10 Kbytes		RAM 12 Kbytes		RAM 12 Kbytes
000100H		000100H		000100H	
0000BFH		0000BFH		0000BFH	
000000H	Periperal	000000H	Periperal	000000H	Periperal

Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.  
 For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.  
 The ROM area in bank FF exceeds 32/48 Kbytes, and its entire image cannot be shown in bank 00.  
 The image between FF4000H/FF8000H and FFFFFFFH is visible in bank 00, while the image between FF0000H and FF3FFFH/FF7FFFH is visible only in bank FF.  
 In MB90V390H/HA/HB, the image for only ROM data between FF8000H to FFFFFFFH is visible in bank 00.  
 As for MB90F394H(A) and MB90394HA, it is possible to set the FF bank area which looks the 00 bank image in the ROM mirror function select register (ROMM) .

## ■ I/O MAP

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
00H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX <sub>B</sub>
01H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX <sub>B</sub>
02H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX <sub>B</sub>
03H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX <sub>B</sub>
04H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX <sub>B</sub>
05H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX <sub>B</sub>
06H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX <sub>B</sub>
07H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX <sub>B</sub>
08H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX <sub>B</sub>
09H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX <sub>B</sub>
0AH	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX <sub>B</sub>
0BH	Port B Data Register	PDRB	R/W	Port B	XXXXXXXX <sub>B</sub>
0CH	Analog Input Enable 0	ADER0	R/W	Port 6, A/D	1111111 <sub>B</sub>
0DH	Analog Input Enable 1/ ADC Select	ADER1	R/W	Port B, A/D	0111111 <sub>B</sub>
0EH	Input Level Select Register	ILSR	R/W	Ports	0000000 <sub>B</sub>
0FH	Input Level Select Register	ILSR	R/W	Ports	0000000 <sub>B</sub>
10H	Port 0 Direction Register	DDR0	R/W	Port 0	0000000 <sub>B</sub>
11H	Port 1 Direction Register	DDR1	R/W	Port 1	0000000 <sub>B</sub>
12H	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 <sub>B</sub>
13H	Port 3 Direction Register	DDR3	R/W	Port 3	0000000 <sub>B</sub>
14H	Port 4 Direction Register	DDR4	R/W	Port 4	0000000 <sub>B</sub>
15H	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 <sub>B</sub>
16H	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 <sub>B</sub>
17H	Port 7 Direction Register	DDR7	R/W	Port 7	0000000 <sub>B</sub>
18H	Port 8 Direction Register	DDR8	R/W	Port 8	0000000 <sub>B</sub>
19H	Port 9 Direction Register	DDR9	R/W	Port 9	0000000 <sub>B</sub>
1AH	Port A Direction Register	DDRA	R/W	Port A	0000000 <sub>B</sub>
1BH	Port B Direction Register	DDRB	R/W	Port B	0000000 <sub>B</sub>
1CH to 1FH	Reserved				
20H	Serial Mode Control 0	UMC0	R/W	UART0	0000100 <sub>B</sub>
21H	Status 0	USR0	R/W		00010000 <sub>B</sub>
22H	Input/Output Data 0	UIDR0/ UODR0	R/W		XXXXXXXX <sub>B</sub>
23H	Rate and Data 0	URD0	R/W		0000000X <sub>B</sub>

(Continued)

# MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
24 <sub>H</sub>	Serial Mode Control 1	UMC1	R/W	UART1	00000100 <sub>B</sub>
25 <sub>H</sub>	Status 1	USR1	R/W		00010000 <sub>B</sub>
26 <sub>H</sub>	Input/Output Data 1	UIDR1/ UODR1	R/W		XXXXXXXX <sub>B</sub>
27 <sub>H</sub>	Rate and Data 1	URD1	R/W		0000000X <sub>B</sub>
28 <sub>H</sub> to 2B <sub>H</sub>	Reserved				
2C <sub>H</sub>	Serial Mode Control 4	SMCS4	R/W	Serial I/O	XXXX0000 <sub>B</sub>
2D <sub>H</sub>	Serial Mode Control 4	SMCS4	R/W		00000010 <sub>B</sub>
2E <sub>H</sub>	Serial Data 4	SDR4	R/W		XXXXXXXX <sub>B</sub>
2F <sub>H</sub>	Serial I/O Prescaler/Edge Selector 4	CDCR4	R/W		0X0X0000 <sub>B</sub>
30 <sub>H</sub>	External Interrupt Enable	ENIR	R/W	External Interrupt	00000000 <sub>B</sub>
31 <sub>H</sub>	External Interrupt Request	EIRR	R/W		XXXXXXXX <sub>B</sub>
32 <sub>H</sub>	External Interrupt Level	ELVR	R/W		00000000 <sub>B</sub>
33 <sub>H</sub>	External Interrupt Level	ELVR	R/W		00000000 <sub>B</sub>
34 <sub>H</sub>	A/D Control Status 0	ADCS0	R/W	A/D Converter	00000000 <sub>B</sub>
35 <sub>H</sub>	A/D Control Status 1	ADCS1	R/W		00000000 <sub>B</sub>
36 <sub>H</sub>	A/D Data 0	ADCR0	R		XXXXXXXX <sub>B</sub>
37 <sub>H</sub>	A/D Data 1	ADCR1	R/W		000010XX <sub>B</sub>
38 <sub>H</sub>	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0X000XX1 <sub>B</sub>
39 <sub>H</sub>	PPG1 Operation Mode Control Register	PPGC1	R/W		0X000001 <sub>B</sub>
3A <sub>H</sub>	PPG0 and PPG1 Clock Select Register	PPG01	R/W		000000XX <sub>B</sub>
3B <sub>H</sub>	Address Detection Control Register 1	PACSR1	R/W	Address Match Detection Function 1	00000000 <sub>B</sub>
3C <sub>H</sub>	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0X000XX1 <sub>B</sub>
3D <sub>H</sub>	PPG3 Operation Mode Control Register	PPGC3	R/W		0X000001 <sub>B</sub>
3E <sub>H</sub>	PPG2 and PPG3 Clock Select Register	PPG23	R/W		000000XX <sub>B</sub>
3F <sub>H</sub>	Clock Output Enable Register	CKOE	R/W	Clock Output	XXXXXX00 <sub>B</sub>
40 <sub>H</sub>	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0X000XX1 <sub>B</sub>
41 <sub>H</sub>	PPG5 Operation Mode Control Register	PPGC5	R/W		0X000001 <sub>B</sub>
42 <sub>H</sub>	PPG4 and PPG5 Clock Select Register	PPG45	R/W		000000XX <sub>B</sub>
43 <sub>H</sub>	Reserved				
44 <sub>H</sub>	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1 <sub>B</sub>
45 <sub>H</sub>	PPG7 Operation Mode Control Register	PPGC7	R/W		0X000001 <sub>B</sub>
46 <sub>H</sub>	PPG6 and PPG7 Clock Select Register	PPG67	R/W		000000XX <sub>B</sub>

(Continued)



# MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1 <sub>B</sub>
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0X000001 <sub>B</sub>
4AH	PPG8 and PPG9 Clock Select Register	PPG89	R/W		000000XX <sub>B</sub>
4BH	Reserved				
4CH	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0X000XX1 <sub>B</sub>
4DH	PPGB Operation Mode Control Register	PPGCB	R/W		0X000001 <sub>B</sub>
4EH	PPGA and PPGB Clock Select Register	PPGAB	R/W		000000XX <sub>B</sub>
4FH	Reserved				
50H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 <sub>B</sub>
51H	Timer Control Status 0	TMCSR0	R/W		XXXX0000 <sub>B</sub>
52H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 <sub>B</sub>
53H	Timer Control Status 1	TMCSR1	R/W		XXXX0000 <sub>B</sub>
54H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 <sub>B</sub>
55H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 <sub>B</sub>
56H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 <sub>B</sub>
57H	Reserved				
58H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 <sub>B</sub>
59H	Output Compare Control Status 1	OCS1	R/W		0XX00000 <sub>B</sub>
5AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 <sub>B</sub>
5BH	Output Compare Control Status 3	OCS3	R/W		0XX00000 <sub>B</sub>
5CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 <sub>B</sub>
5DH	Output Compare Control Status 5	OCS5	R/W		0XX00000 <sub>B</sub>
5EH	Sound Control	SGCR	R/W	Sound Generator	00000000 <sub>B</sub>
5FH	Sound Control	SGCR	R/W		0XXXXXX0 <sub>B</sub>
60H	Watch Timer Control	WTCR	R/W	Watch Timer	000XX000 <sub>B</sub>
61H	Watch Timer Control	WTCR	R/W		00000000 <sub>B</sub>
62H	PWM Control 0	PWC0	R/W	Stepping Motor Controller 0	00000XX0 <sub>B</sub>
63H	Reserved				
64H	PWM Control 1	PWC1	R/W	Stepping Motor Controller 1	00000XX0 <sub>B</sub>
65H	Reserved				
66H	PWM Control 2	PWC2	R/W	Stepping Motor Controller 2	00000XX0 <sub>B</sub>
67H	Reserved				

(Continued)

# MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
68 <sub>H</sub>	PWM Control 3	PWC3	R/W	Stepping Motor Controller 3	00000XX0 <sub>B</sub>
69 <sub>H</sub>	Reserved				
6A <sub>H</sub>	PWM Control 4	PWC4	R/W	Stepping Motor Controller 4	00000XX0 <sub>B</sub>
6B <sub>H</sub>	Reserved				
6C <sub>H</sub>	PWM Control 5	PWC5	R/W	Stepping Motor Controller 5	00000XX0 <sub>B</sub>
6D <sub>H</sub>	Reserved				
6E <sub>H</sub>	Reserved				
6F <sub>H</sub>	ROM Mirror	ROMM	W	ROM Mirror	XXXXXXXX1 <sub>B</sub>
70 <sub>H</sub> to 8F <sub>H</sub>	Reserved for CAN Interface 0/1. Refer to “■ CAN CONTROLLERS”				
90 <sub>H</sub> to 9D <sub>H</sub>	Reserved				
9E <sub>H</sub>	Address Detection Control Register 0	PACSR0	R/W	Address Match Detection Function 0	00000000 <sub>B</sub>
9F <sub>H</sub>	Delayed Interrupt/Release	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 <sub>B</sub>
A0 <sub>H</sub>	Low-power Mode	LPMCR	R/W	Low Power Controller	00011000 <sub>B</sub>
A1 <sub>H</sub>	Clock Selector	CKSCR	R/W	Low Power Controller	11111100 <sub>B</sub>
A2 <sub>H</sub> to A7 <sub>H</sub>	Reserved				
A8 <sub>H</sub>	Watchdog Control	WDTC	R/W	Watchdog Timer	XXXXX111 <sub>B</sub>
A9 <sub>H</sub>	Time Base Timer Control	TBTC	R/W	Time Base Timer	1XX00100 <sub>B</sub>
AA <sub>H</sub> to AD <sub>H</sub>	Reserved				
AE <sub>H</sub>	Flash Control Status (Flash devices only. Otherwise reserved)	FMCS	R/W	Flash Memory	000X0XX0 <sub>B</sub>
AF <sub>H</sub>	Reserved				
B0 <sub>H</sub>	Interrupt Control Register 00	ICR00	R/W	Interrupt Controller	00000111 <sub>B</sub>
B1 <sub>H</sub>	Interrupt Control Register 01	ICR01	R/W		00000111 <sub>B</sub>
B2 <sub>H</sub>	Interrupt Control Register 02	ICR02	R/W		00000111 <sub>B</sub>
B3 <sub>H</sub>	Interrupt Control Register 03	ICR03	R/W		00000111 <sub>B</sub>
B4 <sub>H</sub>	Interrupt Control Register 04	ICR04	R/W		00000111 <sub>B</sub>
B5 <sub>H</sub>	Interrupt Control Register 05	ICR05	R/W		00000111 <sub>B</sub>
B6 <sub>H</sub>	Interrupt Control Register 06	ICR06	R/W		00000111 <sub>B</sub>
B7 <sub>H</sub>	Interrupt Control Register 07	ICR07	R/W		00000111 <sub>B</sub>
B8 <sub>H</sub>	Interrupt Control Register 08	ICR08	R/W		00000111 <sub>B</sub>
B9 <sub>H</sub>	Interrupt Control Register 09	ICR09	R/W		00000111 <sub>B</sub>

(Continued)

# MB90390 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
BA <sub>H</sub>	Interrupt Control Register 10	ICR10	R/W	Interrupt Controller	00000111 <sub>B</sub>
BB <sub>H</sub>	Interrupt Control Register 11	ICR11	R/W		00000111 <sub>B</sub>
BC <sub>H</sub>	Interrupt Control Register 12	ICR12	R/W		00000111 <sub>B</sub>
BD <sub>H</sub>	Interrupt Control Register 13	ICR13	R/W		00000111 <sub>B</sub>
BE <sub>H</sub>	Interrupt Control Register 14	ICR14	R/W		00000111 <sub>B</sub>
BF <sub>H</sub>	Interrupt Control Register 15	ICR15	R/W		00000111 <sub>B</sub>
C0 <sub>H</sub> to FF <sub>H</sub>	Reserved				
3500 <sub>H</sub>	Reload L	PRL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX <sub>B</sub>
3501 <sub>H</sub>	Reload H	PRLH0	R/W		XXXXXXXX <sub>B</sub>
3502 <sub>H</sub>	Reload L	PRL1	R/W		XXXXXXXX <sub>B</sub>
3503 <sub>H</sub>	Reload H	PRLH1	R/W		XXXXXXXX <sub>B</sub>
3504 <sub>H</sub>	Reload L	PRL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX <sub>B</sub>
3505 <sub>H</sub>	Reload H	PRLH2	R/W		XXXXXXXX <sub>B</sub>
3506 <sub>H</sub>	Reload L	PRL3	R/W		XXXXXXXX <sub>B</sub>
3507 <sub>H</sub>	Reload H	PRLH3	R/W		XXXXXXXX <sub>B</sub>
3508 <sub>H</sub>	Reload L	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX <sub>B</sub>
3509 <sub>H</sub>	Reload H	PRLH4	R/W		XXXXXXXX <sub>B</sub>
350A <sub>H</sub>	Reload L	PRL5	R/W		XXXXXXXX <sub>B</sub>
350B <sub>H</sub>	Reload H	PRLH5	R/W		XXXXXXXX <sub>B</sub>
350C <sub>H</sub>	Reload L	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX <sub>B</sub>
350D <sub>H</sub>	Reload H	PRLH6	R/W		XXXXXXXX <sub>B</sub>
350E <sub>H</sub>	Reload L	PRL7	R/W		XXXXXXXX <sub>B</sub>
350F <sub>H</sub>	Reload H	PRLH7	R/W		XXXXXXXX <sub>B</sub>
3510 <sub>H</sub>	Reload L	PRL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX <sub>B</sub>
3511 <sub>H</sub>	Reload H	PRLH8	R/W		XXXXXXXX <sub>B</sub>
3512 <sub>H</sub>	Reload L	PRL9	R/W		XXXXXXXX <sub>B</sub>
3513 <sub>H</sub>	Reload H	PRLH9	R/W		XXXXXXXX <sub>B</sub>
3514 <sub>H</sub>	Reload L	PRLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX <sub>B</sub>
3515 <sub>H</sub>	Reload H	PRLHA	R/W		XXXXXXXX <sub>B</sub>
3516 <sub>H</sub>	Reload L	PRLB	R/W		XXXXXXXX <sub>B</sub>
3517 <sub>H</sub>	Reload H	PRLHB	R/W		XXXXXXXX <sub>B</sub>
3518 <sub>H</sub>	Serial Mode Register	SMR3	R/W	UART3 (LIN/SCI)	00000000 <sub>B</sub>
3519 <sub>H</sub>	Serial Control Register	SCR3	R/W		00000000 <sub>B</sub>
351A <sub>H</sub>	Reception/Transmission Data Register	RDR3/ TDR3	R/W		00000000 <sub>B</sub>

(Continued)

# MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
351B <sub>H</sub>	Serial Status Register	SSR3	R/W	UART3 (LIN/SCI)	00001000 <sub>B</sub>
351C <sub>H</sub>	Extended Communication Control Reg.	ECCR3	R/W		000000XX <sub>B</sub>
351D <sub>H</sub>	Extended Status/Control Register	ESCR3	R/W		00000X00 <sub>B</sub>
351E <sub>H</sub>	Baud Rate Register 0	BGR03	R/W		00000000 <sub>B</sub>
351F <sub>H</sub>	Baud Rate Register 1	BGR13	R/W		00000000 <sub>B</sub>
3520 <sub>H</sub>	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX <sub>B</sub>
3521 <sub>H</sub>	Input Capture 0	IPCP0	R		XXXXXXXX <sub>B</sub>
3522 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX <sub>B</sub>
3523 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX <sub>B</sub>
3524 <sub>H</sub>	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX <sub>B</sub>
3525 <sub>H</sub>	Input Capture 2	IPCP2	R		XXXXXXXX <sub>B</sub>
3526 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX <sub>B</sub>
3527 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX <sub>B</sub>
3528 <sub>H</sub>	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX <sub>B</sub>
3529 <sub>H</sub>	Input Capture 4	IPCP4	R		XXXXXXXX <sub>B</sub>
352A <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX <sub>B</sub>
352B <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX <sub>B</sub>
352C <sub>H</sub>	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000 <sub>B</sub>
352D <sub>H</sub>	Timer Data 0	TCDT0	R/W		00000000 <sub>B</sub>
352E <sub>H</sub>	Timer Control 0	TCCS0	R/W		00000000 <sub>B</sub>
352F <sub>H</sub>	Timer Control 0	TCCS0	R/W		0XXXXXXXX <sub>B</sub>
3530 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX <sub>B</sub>
3531 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXX <sub>B</sub>
3532 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
3533 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
3534 <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX <sub>B</sub>
3535 <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXX <sub>B</sub>
3536 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
3537 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
3538 <sub>H</sub>	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX <sub>B</sub>
3539 <sub>H</sub>	Output Compare 4	OCCP4	R/W		XXXXXXXX <sub>B</sub>
353A <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX <sub>B</sub>
353B <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX <sub>B</sub>

(Continued)

# MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
353C <sub>H</sub>	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000 <sub>B</sub>
353D <sub>H</sub>	Timer Data 1	TCDT1	R/W		00000000 <sub>B</sub>
353E <sub>H</sub>	Timer Control 1	TCCS1	R/W		00000000 <sub>B</sub>
353F <sub>H</sub>	Timer Control 1	TCCS1	R/W		0XXXXXXXX <sub>B</sub>
3540 <sub>H</sub>	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX <sub>B</sub>
3541 <sub>H</sub>	Timer 0/Reload 0	TMR0/ TMRLR0	R/W		XXXXXXXX <sub>B</sub>
3542 <sub>H</sub>	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX <sub>B</sub>
3543 <sub>H</sub>	Timer 1/Reload 1	TMR1/ TMRLR1	R/W		XXXXXXXX <sub>B</sub>
3544 <sub>H</sub> , 3545 <sub>H</sub>	Reserved				
3546 <sub>H</sub>	Frequency Data	SGFR	R/W	Sound Generator	XXXXXXXX <sub>B</sub>
3547 <sub>H</sub>	Amplitude Data	SGAR	R/W		XXXXXXXX <sub>B</sub>
3548 <sub>H</sub>	Decrement Grade	SGDR	R/W		XXXXXXXX <sub>B</sub>
3549 <sub>H</sub>	Tone Count	SGTR	R/W		XXXXXXXX <sub>B</sub>
354A <sub>H</sub>	Sub-second Data	WTBR	R/W	Watch Timer	XXXXXXXX <sub>B</sub>
354B <sub>H</sub>	Sub-second Data	WTBR	R/W		XXXXXXXX <sub>B</sub>
354C <sub>H</sub>	Sub-second Data	WTBR	R/W		XXXXXXXX <sub>B</sub>
354D <sub>H</sub>	Second Data	WTSR	R/W		XX000000 <sub>B</sub>
354E <sub>H</sub>	Minute Data	WTMR	R/W		XX000000 <sub>B</sub>
354F <sub>H</sub>	Hour Data	WTHR	R/W		XXX00000 <sub>B</sub>
3550 <sub>H</sub>	PWM1 Compare 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX <sub>B</sub>
3551 <sub>H</sub>	PWM2 Compare 0	PWC20	R/W		XXXXXXXX <sub>B</sub>
3552 <sub>H</sub>	PWM1 Select 0	PWS10	R/W		00000000 <sub>B</sub>
3553 <sub>H</sub>	PWM2 Select 0	PWS20	R/W		X0000000 <sub>B</sub>
3554 <sub>H</sub>	PWM1 Compare 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX <sub>B</sub>
3555 <sub>H</sub>	PWM2 Compare 1	PWC21	R/W		XXXXXXXX <sub>B</sub>
3556 <sub>H</sub>	PWM1 Select 1	PWS11	R/W		00000000 <sub>B</sub>
3557 <sub>H</sub>	PWM2 Select 1	PWS21	R/W		X0000000 <sub>B</sub>
3558 <sub>H</sub>	PWM1 Compare 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX <sub>B</sub>
3559 <sub>H</sub>	PWM2 Compare 2	PWC22	R/W		XXXXXXXX <sub>B</sub>
355A <sub>H</sub>	PWM1 Select 2	PWS12	R/W		00000000 <sub>B</sub>
355B <sub>H</sub>	PWM2 Select 2	PWS22	R/W		X0000000 <sub>B</sub>

(Continued)

# MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value	
355C <sub>H</sub>	PWM1 Compare 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX <sub>B</sub>	
355D <sub>H</sub>	PWM2 Compare 3	PWC23	R/W		XXXXXXXX <sub>B</sub>	
355E <sub>H</sub>	PWM1 Select 3	PWS13	R/W		00000000 <sub>B</sub>	
355F <sub>H</sub>	PWM2 Select 3	PWS23	R/W		X0000000 <sub>B</sub>	
3560 <sub>H</sub>	PWM1 Compare 4	PWC14	R/W	Stepping Motor Controller 4	XXXXXXXX <sub>B</sub>	
3561 <sub>H</sub>	PWM2 Compare 4	PWC24	R/W		XXXXXXXX <sub>B</sub>	
3562 <sub>H</sub>	PWM1 Select 4	PWS14	R/W		00000000 <sub>B</sub>	
3563 <sub>H</sub>	PWM2 Select 4	PWS24	R/W		X0000000 <sub>B</sub>	
3564 <sub>H</sub>	PWM1 Compare 5	PWC15	R/W	Stepping Motor Controller 5	XXXXXXXX <sub>B</sub>	
3565 <sub>H</sub>	PWM2 Compare 5	PWC25	R/W		XXXXXXXX <sub>B</sub>	
3566 <sub>H</sub>	PWM1 Select 5	PWS15	R/W		00000000 <sub>B</sub>	
3567 <sub>H</sub>	PWM2 Select 5	PWS25	R/W		X0000000 <sub>B</sub>	
3568 <sub>H</sub>	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 <sub>B</sub>	
3569 <sub>H</sub>	Output Compare Control Status 7	OCS7	R/W		XX000000 <sub>B</sub>	
356A <sub>H</sub>	Output Compare 6	OCCP6	R/W		XXXXXXXX <sub>B</sub>	
356B <sub>H</sub>	Output Compare 6	OCCP6	R/W		XXXXXXXX <sub>B</sub>	
356C <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX <sub>B</sub>	
356D <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX <sub>B</sub>	
356E <sub>H</sub>	CAN Direct Mode Register	CDMR	R/W		CAN Clock Sync	XXXXXXXX0 <sub>B</sub>
356F <sub>H</sub>	CAN RX/TX redirect register	CANSWR	R/W		CAN 0/1/2/3	XXXX0000 <sub>B</sub>
3570 <sub>H</sub> to 359F <sub>H</sub>	Reserved for CAN Interface 2/3/4. Refer to "■ CAN CONTROLLERS"					
35A0 <sub>H</sub>	I <sup>2</sup> C Bus Status Register	IBSR	R	I <sup>2</sup> C Interface* <sup>4</sup>	00000000 <sub>B</sub>	
35A1 <sub>H</sub>	I <sup>2</sup> C Bus Control Register	IBCR	R/W		00000000 <sub>B</sub>	
35A2 <sub>H</sub>	I <sup>2</sup> C Ten Bit Slave Address Register	ITBAL	R/W		00000000 <sub>B</sub>	
35A3 <sub>H</sub>		ITBAH	R/W		XXXXXX00 <sub>B</sub>	
35A4 <sub>H</sub>	I <sup>2</sup> C Ten Bit Address Mask Register	ITMKL	R/W		11111111 <sub>B</sub>	
35A5 <sub>H</sub>		ITMKH	R/W		00XXXX11 <sub>B</sub>	
35A6 <sub>H</sub>	I <sup>2</sup> C Seven Bit Slave Address Register	ISBA	R/W		X0000000 <sub>B</sub>	
35A7 <sub>H</sub>	I <sup>2</sup> C Seven Bit Address Mask Register	ISMK	R/W		01111111 <sub>B</sub>	
35A8 <sub>H</sub>	I <sup>2</sup> C Data Register	IDAR	R/W		00000000 <sub>B</sub>	
35A9 <sub>H</sub>	I <sup>2</sup> C Noise Filter Configuration Register* <sup>2</sup>	INFCR	R/W		XXXXXX01 <sub>B</sub>	
35AA <sub>H</sub>	Reserved					
35AB <sub>H</sub>	I <sup>2</sup> C Clock Control Register	ICCR	R/W		I <sup>2</sup> C Interface* <sup>4</sup>	X0011111 <sub>B</sub>
35AC <sub>H</sub> to 35BF <sub>H</sub>	Reserved					
35C0 <sub>H</sub>	Parameter Register Low Byte	CMPRL	R/W	Clock Modulator	11111101 <sub>B</sub>	

(Continued)

# MB90390 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
35C1 <sub>H</sub>	Parameter Register High Byte	CMPRH	R/W	Clock Modulator	XX000010 <sub>B</sub>
35C2 <sub>H</sub>	Clock Modulator Control Register	CMCR	R/W		00010000 <sub>B</sub>
35C3 <sub>H</sub> to 35C8 <sub>H</sub>	Reserved				
35C9 <sub>H</sub>	Input Capture Edge 0/1	ICE01	R/W	Input Capture 0/1	XXXXX0XX <sub>B</sub>
35CA <sub>H</sub>	Input Capture Edge 2/3*3	ICE23	R	Input Capture 2/3	XXXXXXXX <sub>B</sub>
35CB <sub>H</sub>	Input Capture Edge 4/5	ICE45	R/W	Input Capture 4/5	XXXXX0XX <sub>B</sub>
35CC <sub>H</sub> to 35CE <sub>H</sub>	Reserved				
35CF <sub>H</sub>	PLL and special configuration control resister	PSCCR	W	PLL	XXXX0000 <sub>B</sub>
35D0 <sub>H</sub> to 35D7 <sub>H</sub>	Reserved				
35D8 <sub>H</sub>	Serial Mode Register	SMR2	R/W	UART2*1 (LIN/SCI)	00000000 <sub>B</sub>
35D9 <sub>H</sub>	Serial Control Register	SCR2	R/W		00000000 <sub>B</sub>
35DA <sub>H</sub>	Reception/Transmission Data Register	RDR2/ TDR2	R/W		00000000 <sub>B</sub>
35DB <sub>H</sub>	Serial Status Register	SSR2	R/W		00001000 <sub>B</sub>
35DC <sub>H</sub>	Extended Communication Control Register	ECCR2	R/W		000000XX <sub>B</sub>
35DD <sub>H</sub>	Extended Status/Control Register	ESCR2	R/W		00000X00 <sub>B</sub>
35DE <sub>H</sub>	Baud Rate Register 0	BGR02	R/W		00000000 <sub>B</sub>
35DF <sub>H</sub>	Baud Rate Register 1	BGR12	R/W		00000000 <sub>B</sub>
35E0 <sub>H</sub>	Detection Address Setting Register 0 (Low-order)	PADR0	R/W	Address Match Detection Function 0	XXXXXXXX <sub>B</sub>
35E1 <sub>H</sub>	Detection Address Setting Register 0 (Middle-order)	PADR0	R/W		XXXXXXXX <sub>B</sub>
35E2 <sub>H</sub>	Detection Address Setting Register 0 (High-order)	PADR0	R/W		XXXXXXXX <sub>B</sub>
35E3 <sub>H</sub>	Detection Address Setting Register 1 (Low-order)	PADR1	R/W		XXXXXXXX <sub>B</sub>
35E4 <sub>H</sub>	Detection Address Setting Register 1 (Middle-order)	PADR1	R/W		XXXXXXXX <sub>B</sub>
35E5 <sub>H</sub>	Detection Address Setting Register 1 (High-order)	PADR1	R/W		XXXXXXXX <sub>B</sub>
35E6 <sub>H</sub> to 35EF <sub>H</sub>	Reserved				
35F0 <sub>H</sub>	Detection Address Setting Register 3 (Low-order)	PADR3	R/W	Address Match Detection Function 1	XXXXXXXX <sub>B</sub>
35F1 <sub>H</sub>	Detection Address Setting Register 3 (Middle-order)	PADR3	R/W		XXXXXXXX <sub>B</sub>

(Continued)

# MB90390 Series

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
35F2 <sub>H</sub>	Detection Address Setting Register 3 (High-order)	PADR3	R/W	Address Match Detection Function 1	XXXXXXXX <sub>B</sub>
35F3 <sub>H</sub>	Detection Address Setting Register 4 (Low-order)	PADR4	R/W		XXXXXXXX <sub>B</sub>
35F4 <sub>H</sub>	Detection Address Setting Register 4 (Middle-order)	PADR4	R/W		XXXXXXXX <sub>B</sub>
35F5 <sub>H</sub>	Detection Address Setting Register 4 (High-order)	PADR4	R/W		XXXXXXXX <sub>B</sub>
35F6 <sub>H</sub>	Detection Address Setting Register 5 (Low-order)	PADR5	R/W		XXXXXXXX <sub>B</sub>
35F7 <sub>H</sub>	Detection Address Setting Register 5 (Middle-order)	PADR5	R/W		XXXXXXXX <sub>B</sub>
35F8 <sub>H</sub>	Detection Address Setting Register 5 (High-order)	PADR5	R/W		XXXXXXXX <sub>B</sub>
35F9 <sub>H</sub> to 35FF <sub>H</sub>	Reserved				
3600 <sub>H</sub> to 37FF <sub>H</sub>	Reserved for CAN Interface 0. Refer to “■ CAN CONTROLLERS”				
3800 <sub>H</sub> to 39FF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
3A00 <sub>H</sub> to 3BFF <sub>H</sub>	Reserved for CAN Interface 2. Refer to “■ CAN CONTROLLERS”				
3C00 <sub>H</sub> to 3DFF <sub>H</sub>	Reserved for CAN Interface 3. Refer to “■ CAN CONTROLLERS”				
3E00 <sub>H</sub> to 3FFF <sub>H</sub>	Reserved for CAN Interface 4. Refer to “■ CAN CONTROLLERS”				

\*1 : UART2 (LIN/SCI) is only available in MB90V390HA/HB.

\*2 : I<sup>2</sup>C Noise Filter Configuration Register is only available in the devices MB90V390HA/HB, MB90394HA.

\*3 : Input Capture Edge 2/3 register is different in MB90V390HA/HB, the access is “R/W” and initial value is “XXXXX0XX<sub>B</sub>”.

\*4 : I<sup>2</sup>C Interface is not available in MB90F394H(A).



- Explanation on read/write
  - R/W : Readable and writable
  - R : Read only
  - W : Write only
- Explanation on initial values
  - 0 : Initial value is "0".
  - 1 : Initial value is "1".
  - X : Initial value is undefined.

Note : Any write access to reserved addresses in I/O map should not be performed. A read access to reserved address results in reading "X".

# MB90390 Series

## ■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance mask register 0/acceptance mask register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

**List of Control Registers (1)**

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
000070 <sub>H</sub>	000080 <sub>H</sub>	003570 <sub>H</sub>	003580 <sub>H</sub>	003590 <sub>H</sub>	Message buffer valid register	BVALR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000071 <sub>H</sub>	000081 <sub>H</sub>	003571 <sub>H</sub>	003581 <sub>H</sub>	003591 <sub>H</sub>				
000072 <sub>H</sub>	000082 <sub>H</sub>	003572 <sub>H</sub>	003582 <sub>H</sub>	003592 <sub>H</sub>	Transmit request register	TREQR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000073 <sub>H</sub>	000083 <sub>H</sub>	003573 <sub>H</sub>	003583 <sub>H</sub>	003593 <sub>H</sub>				
000074 <sub>H</sub>	000084 <sub>H</sub>	003574 <sub>H</sub>	003584 <sub>H</sub>	003594 <sub>H</sub>	Transmit cancel register	TCANR	W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000075 <sub>H</sub>	000085 <sub>H</sub>	003575 <sub>H</sub>	003585 <sub>H</sub>	003595 <sub>H</sub>				
000076 <sub>H</sub>	000086 <sub>H</sub>	003576 <sub>H</sub>	003586 <sub>H</sub>	003596 <sub>H</sub>	Transmit complete register	TCR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000077 <sub>H</sub>	000087 <sub>H</sub>	003577 <sub>H</sub>	003587 <sub>H</sub>	003597 <sub>H</sub>				
000078 <sub>H</sub>	000088 <sub>H</sub>	003578 <sub>H</sub>	003588 <sub>H</sub>	003598 <sub>H</sub>	Receive complete register	RCR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000079 <sub>H</sub>	000089 <sub>H</sub>	003579 <sub>H</sub>	003589 <sub>H</sub>	003599 <sub>H</sub>				
00007A <sub>H</sub>	00008A <sub>H</sub>	00357A <sub>H</sub>	00358A <sub>H</sub>	00359A <sub>H</sub>	Remote request receiving register	RRTRR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00007B <sub>H</sub>	00008B <sub>H</sub>	00357B <sub>H</sub>	00358B <sub>H</sub>	00359B <sub>H</sub>				
00007C <sub>H</sub>	00008C <sub>H</sub>	00357C <sub>H</sub>	00358C <sub>H</sub>	00359C <sub>H</sub>	Receive overrun register	ROVRR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00007D <sub>H</sub>	00008D <sub>H</sub>	00357D <sub>H</sub>	00358D <sub>H</sub>	00359D <sub>H</sub>				
00007E <sub>H</sub>	00008E <sub>H</sub>	00357E <sub>H</sub>	00358E <sub>H</sub>	00359E <sub>H</sub>	Receive interrupt enable register	RIER	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00007F <sub>H</sub>	00008F <sub>H</sub>	00357F <sub>H</sub>	00358F <sub>H</sub>	00359F <sub>H</sub>				

List of Control Registers (2)

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003700 <sub>H</sub>	003900 <sub>H</sub>	003B00 <sub>H</sub>	003D00 <sub>H</sub>	003F00 <sub>H</sub>	Control status register	CSR	R/W, R	00XXX000 <sub>B</sub> 0XXXX0X1 <sub>B</sub>
003701 <sub>H</sub>	003901 <sub>H</sub>	003B01 <sub>H</sub>	003D01 <sub>H</sub>	003F01 <sub>H</sub>				
003702 <sub>H</sub>	003902 <sub>H</sub>	003B02 <sub>H</sub>	003D02 <sub>H</sub>	003F02 <sub>H</sub>	Last event indicator register	LEIR	R/W	XXXXXXXX <sub>B</sub> 000X0000 <sub>B</sub>
003703 <sub>H</sub>	003903 <sub>H</sub>	003B03 <sub>H</sub>	003D03 <sub>H</sub>	003F03 <sub>H</sub>				
003704 <sub>H</sub>	003904 <sub>H</sub>	003B04 <sub>H</sub>	003D04 <sub>H</sub>	003F04 <sub>H</sub>	Receive/transmit error counter	RTEC	R	00000000 <sub>B</sub> 00000000 <sub>B</sub>
003705 <sub>H</sub>	003905 <sub>H</sub>	003B05 <sub>H</sub>	003D05 <sub>H</sub>	003F05 <sub>H</sub>				
003706 <sub>H</sub>	003906 <sub>H</sub>	003B06 <sub>H</sub>	003D06 <sub>H</sub>	003F06 <sub>H</sub>	Bit timing register	BTR	R/W	X1111111 <sub>B</sub> 11111111 <sub>B</sub>
003707 <sub>H</sub>	003907 <sub>H</sub>	003B07 <sub>H</sub>	003D07 <sub>H</sub>	003F07 <sub>H</sub>				
003708 <sub>H</sub>	003908 <sub>H</sub>	003B08 <sub>H</sub>	003D08 <sub>H</sub>	003F08 <sub>H</sub>	IDE register	IDER	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003709 <sub>H</sub>	003909 <sub>H</sub>	003B09 <sub>H</sub>	003D09 <sub>H</sub>	003F09 <sub>H</sub>				
00370A <sub>H</sub>	00390A <sub>H</sub>	003B0A <sub>H</sub>	003D0A <sub>H</sub>	003F0A <sub>H</sub>	Transmit RTR register	TRTRR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00370B <sub>H</sub>	00390B <sub>H</sub>	003B0B <sub>H</sub>	003D0B <sub>H</sub>	003F0B <sub>H</sub>				
00370C <sub>H</sub>	00390C <sub>H</sub>	003B0C <sub>H</sub>	003D0C <sub>H</sub>	003F0C <sub>H</sub>	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00370D <sub>H</sub>	00390D <sub>H</sub>	003B0D <sub>H</sub>	003D0D <sub>H</sub>	003F0D <sub>H</sub>				
00370E <sub>H</sub>	00390E <sub>H</sub>	003B0E <sub>H</sub>	003D0E <sub>H</sub>	003F0E <sub>H</sub>	Transmit interrupt enable register	TIER	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00370F <sub>H</sub>	00390F <sub>H</sub>	003B0F <sub>H</sub>	003D0F <sub>H</sub>	003F0F <sub>H</sub>				
003710 <sub>H</sub>	003910 <sub>H</sub>	003B10 <sub>H</sub>	003D10 <sub>H</sub>	003F10 <sub>H</sub>	Acceptance mask select register	AMSR	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003711 <sub>H</sub>	003911 <sub>H</sub>	003B11 <sub>H</sub>	003D11 <sub>H</sub>	003F11 <sub>H</sub>				
003712 <sub>H</sub>	003912 <sub>H</sub>	003B12 <sub>H</sub>	003D12 <sub>H</sub>	003F12 <sub>H</sub>				
003713 <sub>H</sub>	003913 <sub>H</sub>	003B13 <sub>H</sub>	003D13 <sub>H</sub>	003F13 <sub>H</sub>				
003714 <sub>H</sub>	003914 <sub>H</sub>	003B14 <sub>H</sub>	003D14 <sub>H</sub>	003F14 <sub>H</sub>	Acceptance mask register 0	AMR0	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003715 <sub>H</sub>	003915 <sub>H</sub>	003B15 <sub>H</sub>	003D15 <sub>H</sub>	003F15 <sub>H</sub>				
003716 <sub>H</sub>	003916 <sub>H</sub>	003B16 <sub>H</sub>	003D16 <sub>H</sub>	003F16 <sub>H</sub>				
003717 <sub>H</sub>	003917 <sub>H</sub>	003B17 <sub>H</sub>	003D17 <sub>H</sub>	003F17 <sub>H</sub>				
003718 <sub>H</sub>	003918 <sub>H</sub>	003B18 <sub>H</sub>	003D18 <sub>H</sub>	003F18 <sub>H</sub>	Acceptance mask register 1	AMR1	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003719 <sub>H</sub>	003919 <sub>H</sub>	003B19 <sub>H</sub>	003D19 <sub>H</sub>	003F19 <sub>H</sub>				
00371A <sub>H</sub>	00391A <sub>H</sub>	003B1A <sub>H</sub>	003D1A <sub>H</sub>	003F1A <sub>H</sub>				
00371B <sub>H</sub>	00391B <sub>H</sub>	003B1B <sub>H</sub>	003D1B <sub>H</sub>	003F1B <sub>H</sub>				

# MB90390 Series

List of Message Buffers (ID Registers) (1)

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003600 <sub>H</sub> to 00361F <sub>H</sub>	003800 <sub>H</sub> to 00381F <sub>H</sub>	003A00 <sub>H</sub> to 003A1F <sub>H</sub>	003C00 <sub>H</sub> to 003C1F <sub>H</sub>	003E00 <sub>H</sub> to 003E1F <sub>H</sub>	General- purpose RAM	—	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003620 <sub>H</sub>	003820 <sub>H</sub>	003A20 <sub>H</sub>	003C20 <sub>H</sub>	003E20 <sub>H</sub>	ID register 0	IDR0	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003621 <sub>H</sub>	003821 <sub>H</sub>	003A21 <sub>H</sub>	003C21 <sub>H</sub>	003E21 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003622 <sub>H</sub>	003822 <sub>H</sub>	003A22 <sub>H</sub>	003C22 <sub>H</sub>	003E22 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003623 <sub>H</sub>	003823 <sub>H</sub>	003A23 <sub>H</sub>	003C23 <sub>H</sub>	003E23 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003624 <sub>H</sub>	003824 <sub>H</sub>	003A24 <sub>H</sub>	003C24 <sub>H</sub>	003E24 <sub>H</sub>	ID register 1	IDR1	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003625 <sub>H</sub>	003825 <sub>H</sub>	003A25 <sub>H</sub>	003C25 <sub>H</sub>	003E25 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003626 <sub>H</sub>	003826 <sub>H</sub>	003A26 <sub>H</sub>	003C26 <sub>H</sub>	003E26 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003627 <sub>H</sub>	003827 <sub>H</sub>	003A27 <sub>H</sub>	003C27 <sub>H</sub>	003E27 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003628 <sub>H</sub>	003828 <sub>H</sub>	003A28 <sub>H</sub>	003C28 <sub>H</sub>	003E28 <sub>H</sub>	ID register 2	IDR2	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003629 <sub>H</sub>	003829 <sub>H</sub>	003A29 <sub>H</sub>	003C29 <sub>H</sub>	003E29 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00362A <sub>H</sub>	00382A <sub>H</sub>	003A2A <sub>H</sub>	003C2A <sub>H</sub>	003E2A <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00362B <sub>H</sub>	00382B <sub>H</sub>	003A2B <sub>H</sub>	003C2B <sub>H</sub>	003E2B <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00362C <sub>H</sub>	00382C <sub>H</sub>	003A2C <sub>H</sub>	003C2C <sub>H</sub>	003E2C <sub>H</sub>	ID register 3	IDR3	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00362D <sub>H</sub>	00382D <sub>H</sub>	003A2D <sub>H</sub>	003C2D <sub>H</sub>	003E2D <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00362E <sub>H</sub>	00382E <sub>H</sub>	003A2E <sub>H</sub>	003C2E <sub>H</sub>	003E2E <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00362F <sub>H</sub>	00382F <sub>H</sub>	003A2F <sub>H</sub>	003C2F <sub>H</sub>	003E2F <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003630 <sub>H</sub>	003830 <sub>H</sub>	003A30 <sub>H</sub>	003C30 <sub>H</sub>	003E30 <sub>H</sub>	ID register 4	IDR4	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003631 <sub>H</sub>	003831 <sub>H</sub>	003A31 <sub>H</sub>	003C31 <sub>H</sub>	003E31 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003632 <sub>H</sub>	003832 <sub>H</sub>	003A32 <sub>H</sub>	003C32 <sub>H</sub>	003E32 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003633 <sub>H</sub>	003833 <sub>H</sub>	003A33 <sub>H</sub>	003C33 <sub>H</sub>	003E33 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003634 <sub>H</sub>	003834 <sub>H</sub>	003A34 <sub>H</sub>	003C34 <sub>H</sub>	003E34 <sub>H</sub>	ID register 5	IDR5	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003635 <sub>H</sub>	003835 <sub>H</sub>	003A35 <sub>H</sub>	003C35 <sub>H</sub>	003E35 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003636 <sub>H</sub>	003836 <sub>H</sub>	003A36 <sub>H</sub>	003C36 <sub>H</sub>	003E36 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003637 <sub>H</sub>	003837 <sub>H</sub>	003A37 <sub>H</sub>	003C37 <sub>H</sub>	003E37 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003638 <sub>H</sub>	003838 <sub>H</sub>	003A38 <sub>H</sub>	003C38 <sub>H</sub>	003E38 <sub>H</sub>	ID register 6	IDR6	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
003639 <sub>H</sub>	003839 <sub>H</sub>	003A39 <sub>H</sub>	003C39 <sub>H</sub>	003E39 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00363A <sub>H</sub>	00383A <sub>H</sub>	003A3A <sub>H</sub>	003C3A <sub>H</sub>	003E3A <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00363B <sub>H</sub>	00383B <sub>H</sub>	003A3B <sub>H</sub>	003C3B <sub>H</sub>	003E3B <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00363C <sub>H</sub>	00383C <sub>H</sub>	003A3C <sub>H</sub>	003C3C <sub>H</sub>	003E3C <sub>H</sub>	ID register 7	IDR7	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00363D <sub>H</sub>	00383D <sub>H</sub>	003A3D <sub>H</sub>	003C3D <sub>H</sub>	003E3D <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00363E <sub>H</sub>	00383E <sub>H</sub>	003A3E <sub>H</sub>	003C3E <sub>H</sub>	003E3E <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
00363F <sub>H</sub>	00383F <sub>H</sub>	003A3F <sub>H</sub>	003C3F <sub>H</sub>	003E3F <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>

List of Message Buffers (ID Registers) (2)

Address		Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003640 <sub>H</sub>	003840 <sub>H</sub>	003A40 <sub>H</sub>	003C40 <sub>H</sub>	003E40 <sub>H</sub>	ID register 8	IDR8	R/W	XXXXXXXX <sub>B</sub>
003641 <sub>H</sub>	003841 <sub>H</sub>	003A41 <sub>H</sub>	003C41 <sub>H</sub>	003E41 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003642 <sub>H</sub>	003842 <sub>H</sub>	003A42 <sub>H</sub>	003C42 <sub>H</sub>	003E42 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003643 <sub>H</sub>	003843 <sub>H</sub>	003A43 <sub>H</sub>	003C43 <sub>H</sub>	003E43 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003644 <sub>H</sub>	003844 <sub>H</sub>	003A44 <sub>H</sub>	003C44 <sub>H</sub>	003E44 <sub>H</sub>	ID register 9	IDR9	R/W	XXXXXXXX <sub>B</sub>
003645 <sub>H</sub>	003845 <sub>H</sub>	003A45 <sub>H</sub>	003C45 <sub>H</sub>	003E45 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003646 <sub>H</sub>	003846 <sub>H</sub>	003A46 <sub>H</sub>	003C46 <sub>H</sub>	003E46 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003647 <sub>H</sub>	003847 <sub>H</sub>	003A47 <sub>H</sub>	003C47 <sub>H</sub>	003E47 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003648 <sub>H</sub>	003848 <sub>H</sub>	003A48 <sub>H</sub>	003C48 <sub>H</sub>	003E48 <sub>H</sub>	ID register 10	IDR10	R/W	XXXXXXXX <sub>B</sub>
003649 <sub>H</sub>	003849 <sub>H</sub>	003A49 <sub>H</sub>	003C49 <sub>H</sub>	003E49 <sub>H</sub>				XXXXXXXX <sub>B</sub>
00364A <sub>H</sub>	00384A <sub>H</sub>	003A4A <sub>H</sub>	003C4A <sub>H</sub>	003E4A <sub>H</sub>				XXXXXXXX <sub>B</sub>
00364B <sub>H</sub>	00384B <sub>H</sub>	003A4B <sub>H</sub>	003C4B <sub>H</sub>	003E4B <sub>H</sub>				XXXXXXXX <sub>B</sub>
00364C <sub>H</sub>	00384C <sub>H</sub>	003A4C <sub>H</sub>	003C4C <sub>H</sub>	003E4C <sub>H</sub>	ID register 11	IDR11	R/W	XXXXXXXX <sub>B</sub>
00364D <sub>H</sub>	00384D <sub>H</sub>	003A4D <sub>H</sub>	003C4D <sub>H</sub>	003E4D <sub>H</sub>				XXXXXXXX <sub>B</sub>
00364E <sub>H</sub>	00384E <sub>H</sub>	003A4E <sub>H</sub>	003C4E <sub>H</sub>	003E4E <sub>H</sub>				XXXXXXXX <sub>B</sub>
00364F <sub>H</sub>	00384F <sub>H</sub>	003A4F <sub>H</sub>	003C4F <sub>H</sub>	003E4F <sub>H</sub>				XXXXXXXX <sub>B</sub>
003650 <sub>H</sub>	003850 <sub>H</sub>	003A50 <sub>H</sub>	003C50 <sub>H</sub>	003E50 <sub>H</sub>	ID register 12	IDR12	R/W	XXXXXXXX <sub>B</sub>
003651 <sub>H</sub>	003851 <sub>H</sub>	003A51 <sub>H</sub>	003C51 <sub>H</sub>	003E51 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003652 <sub>H</sub>	003852 <sub>H</sub>	003A52 <sub>H</sub>	003C52 <sub>H</sub>	003E52 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003653 <sub>H</sub>	003853 <sub>H</sub>	003A53 <sub>H</sub>	003C53 <sub>H</sub>	003E53 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003654 <sub>H</sub>	003854 <sub>H</sub>	003A54 <sub>H</sub>	003C54 <sub>H</sub>	003E54 <sub>H</sub>	ID register 13	IDR13	R/W	XXXXXXXX <sub>B</sub>
003655 <sub>H</sub>	003855 <sub>H</sub>	003A55 <sub>H</sub>	003C55 <sub>H</sub>	003E55 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003656 <sub>H</sub>	003856 <sub>H</sub>	003A56 <sub>H</sub>	003C56 <sub>H</sub>	003E56 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003657 <sub>H</sub>	003857 <sub>H</sub>	003A57 <sub>H</sub>	003C57 <sub>H</sub>	003E57 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003658 <sub>H</sub>	003858 <sub>H</sub>	003A58 <sub>H</sub>	003C58 <sub>H</sub>	003E58 <sub>H</sub>	ID register 14	IDR14	R/W	XXXXXXXX <sub>B</sub>
003659 <sub>H</sub>	003859 <sub>H</sub>	003A59 <sub>H</sub>	003C59 <sub>H</sub>	003E59 <sub>H</sub>				XXXXXXXX <sub>B</sub>
00365A <sub>H</sub>	00385A <sub>H</sub>	003A5A <sub>H</sub>	003C5A <sub>H</sub>	003E5A <sub>H</sub>				XXXXXXXX <sub>B</sub>
00365B <sub>H</sub>	00385B <sub>H</sub>	003A5B <sub>H</sub>	003C5B <sub>H</sub>	003E5B <sub>H</sub>				XXXXXXXX <sub>B</sub>
00365C <sub>H</sub>	00385C <sub>H</sub>	003A5C <sub>H</sub>	003C5C <sub>H</sub>	003E5C <sub>H</sub>	ID register 15	IDR7	R/W	XXXXXXXX <sub>B</sub>
00365D <sub>H</sub>	00385D <sub>H</sub>	003A5D <sub>H</sub>	003C5D <sub>H</sub>	003E5D <sub>H</sub>				XXXXXXXX <sub>B</sub>
00365E <sub>H</sub>	00385E <sub>H</sub>	003A5E <sub>H</sub>	003C5E <sub>H</sub>	003E5E <sub>H</sub>				XXXXXXXX <sub>B</sub>
00365F <sub>H</sub>	00385F <sub>H</sub>	003A5F <sub>H</sub>	003C5F <sub>H</sub>	003E5F <sub>H</sub>				XXXXXXXX <sub>B</sub>

# MB90390 Series

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003660 <sub>H</sub>	003860 <sub>H</sub>	003A60 <sub>H</sub>	003C60 <sub>H</sub>	003E60 <sub>H</sub>	DLC register 0	DLCR0	R/W	XXXXXXXX <sub>B</sub>
003661 <sub>H</sub>	003861 <sub>H</sub>	003A61 <sub>H</sub>	003C61 <sub>H</sub>	003E61 <sub>H</sub>				
003662 <sub>H</sub>	003862 <sub>H</sub>	003A62 <sub>H</sub>	003C62 <sub>H</sub>	003E62 <sub>H</sub>	DLC register 1	DLCR1	R/W	XXXXXXXX <sub>B</sub>
003663 <sub>H</sub>	003863 <sub>H</sub>	003A63 <sub>H</sub>	003C63 <sub>H</sub>	003E63 <sub>H</sub>				
003664 <sub>H</sub>	003864 <sub>H</sub>	003A64 <sub>H</sub>	003C64 <sub>H</sub>	003E64 <sub>H</sub>	DLC register 2	DLCR2	R/W	XXXXXXXX <sub>B</sub>
003665 <sub>H</sub>	003865 <sub>H</sub>	003A65 <sub>H</sub>	003C65 <sub>H</sub>	003E65 <sub>H</sub>				
003666 <sub>H</sub>	003866 <sub>H</sub>	003A66 <sub>H</sub>	003C66 <sub>H</sub>	003E66 <sub>H</sub>	DLC register 3	DLCR3	R/W	XXXXXXXX <sub>B</sub>
003667 <sub>H</sub>	003867 <sub>H</sub>	003A67 <sub>H</sub>	003C67 <sub>H</sub>	003E67 <sub>H</sub>				
003668 <sub>H</sub>	003868 <sub>H</sub>	003A68 <sub>H</sub>	003C68 <sub>H</sub>	003E68 <sub>H</sub>	DLC register 4	DLCR4	R/W	XXXXXXXX <sub>B</sub>
003669 <sub>H</sub>	003869 <sub>H</sub>	003A69 <sub>H</sub>	003C69 <sub>H</sub>	003E69 <sub>H</sub>				
00366A <sub>H</sub>	00386A <sub>H</sub>	003A6A <sub>H</sub>	003C6A <sub>H</sub>	003E6A <sub>H</sub>	DLC register 5	DLCR5	R/W	XXXXXXXX <sub>B</sub>
00366B <sub>H</sub>	00386B <sub>H</sub>	003A6B <sub>H</sub>	003C6B <sub>H</sub>	003E6B <sub>H</sub>				
00366C <sub>H</sub>	00386C <sub>H</sub>	003A6C <sub>H</sub>	003C6C <sub>H</sub>	003E6C <sub>H</sub>	DLC register 6	DLCR6	R/W	XXXXXXXX <sub>B</sub>
00366D <sub>H</sub>	00386D <sub>H</sub>	003A6D <sub>H</sub>	003C6D <sub>H</sub>	003E6D <sub>H</sub>				
00366E <sub>H</sub>	00386E <sub>H</sub>	003A6E <sub>H</sub>	003C6E <sub>H</sub>	003E6E <sub>H</sub>	DLC register 7	DLCR7	R/W	XXXXXXXX <sub>B</sub>
00366F <sub>H</sub>	00386F <sub>H</sub>	003A6F <sub>H</sub>	003C6F <sub>H</sub>	003E6F <sub>H</sub>				
003670 <sub>H</sub>	003870 <sub>H</sub>	003A70 <sub>H</sub>	003C70 <sub>H</sub>	003E70 <sub>H</sub>	DLC register 8	DLCR8	R/W	XXXXXXXX <sub>B</sub>
003671 <sub>H</sub>	003871 <sub>H</sub>	003A71 <sub>H</sub>	003C71 <sub>H</sub>	003E71 <sub>H</sub>				
003672 <sub>H</sub>	003872 <sub>H</sub>	003A72 <sub>H</sub>	003C72 <sub>H</sub>	003E72 <sub>H</sub>	DLC register 9	DLCR9	R/W	XXXXXXXX <sub>B</sub>
003673 <sub>H</sub>	003873 <sub>H</sub>	003A73 <sub>H</sub>	003C73 <sub>H</sub>	003E73 <sub>H</sub>				
003674 <sub>H</sub>	003874 <sub>H</sub>	003A74 <sub>H</sub>	003C74 <sub>H</sub>	003E74 <sub>H</sub>	DLC register 10	DLCR10	R/W	XXXXXXXX <sub>B</sub>
003675 <sub>H</sub>	003875 <sub>H</sub>	003A75 <sub>H</sub>	003C75 <sub>H</sub>	003E75 <sub>H</sub>				
003676 <sub>H</sub>	003876 <sub>H</sub>	003A76 <sub>H</sub>	003C76 <sub>H</sub>	003E76 <sub>H</sub>	DLC register 11	DLCR11	R/W	XXXXXXXX <sub>B</sub>
003677 <sub>H</sub>	003877 <sub>H</sub>	003A77 <sub>H</sub>	003C77 <sub>H</sub>	003E77 <sub>H</sub>				
003678 <sub>H</sub>	003878 <sub>H</sub>	003A78 <sub>H</sub>	003C78 <sub>H</sub>	003E78 <sub>H</sub>	DLC register 12	DLCR12	R/W	XXXXXXXX <sub>B</sub>
003679 <sub>H</sub>	003879 <sub>H</sub>	003A79 <sub>H</sub>	003C79 <sub>H</sub>	003E79 <sub>H</sub>				
00367A <sub>H</sub>	00387A <sub>H</sub>	003A7A <sub>H</sub>	003C7A <sub>H</sub>	003E7A <sub>H</sub>	DLC register 13	DLCR13	R/W	XXXXXXXX <sub>B</sub>
00367B <sub>H</sub>	00387B <sub>H</sub>	003A7B <sub>H</sub>	003C7B <sub>H</sub>	003E7B <sub>H</sub>				
00367C <sub>H</sub>	00387C <sub>H</sub>	003A7C <sub>H</sub>	003C7C <sub>H</sub>	003E7C <sub>H</sub>	DLC register 14	DLCR14	R/W	XXXXXXXX <sub>B</sub>
00367D <sub>H</sub>	00387D <sub>H</sub>	003A7D <sub>H</sub>	003C7D <sub>H</sub>	003E7D <sub>H</sub>				
00367E <sub>H</sub>	00387E <sub>H</sub>	003A7E <sub>H</sub>	003C7E <sub>H</sub>	003E7E <sub>H</sub>	DLC register 15	DLCR15	R/W	XXXXXXXX <sub>B</sub>
00367F <sub>H</sub>	00387F <sub>H</sub>	003A7F <sub>H</sub>	003C7F <sub>H</sub>	003E7F <sub>H</sub>				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003680 <sub>H</sub> to 003687 <sub>H</sub>	003880 <sub>H</sub> to 003887 <sub>H</sub>	003A80 <sub>H</sub> to 003A87 <sub>H</sub>	003C80 <sub>H</sub> to 003C87 <sub>H</sub>	003E80 <sub>H</sub> to 003E87 <sub>H</sub>	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003688 <sub>H</sub> to 00368F <sub>H</sub>	003888 <sub>H</sub> to 00388F <sub>H</sub>	003A88 <sub>H</sub> to 003A8F <sub>H</sub>	003C88 <sub>H</sub> to 003C8F <sub>H</sub>	003E88 <sub>H</sub> to 003E8F <sub>H</sub>	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003690 <sub>H</sub> to 003697 <sub>H</sub>	003890 <sub>H</sub> to 003897 <sub>H</sub>	003A90 <sub>H</sub> to 003A97 <sub>H</sub>	003C90 <sub>H</sub> to 003C97 <sub>H</sub>	003E90 <sub>H</sub> to 003E97 <sub>H</sub>	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003698 <sub>H</sub> to 00369F <sub>H</sub>	003898 <sub>H</sub> to 00389F <sub>H</sub>	003A98 <sub>H</sub> to 003A9F <sub>H</sub>	003C98 <sub>H</sub> to 003C9F <sub>H</sub>	003E98 <sub>H</sub> to 003E9F <sub>H</sub>	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036A0 <sub>H</sub> to 0036A7 <sub>H</sub>	0038A0 <sub>H</sub> to 0038A7 <sub>H</sub>	003AA0 <sub>H</sub> to 003AA7 <sub>H</sub>	003CA0 <sub>H</sub> to 003CA7 <sub>H</sub>	003EA0 <sub>H</sub> to 003EA7 <sub>H</sub>	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036A8 <sub>H</sub> to 0036AF <sub>H</sub>	0038A8 <sub>H</sub> to 0038AF <sub>H</sub>	003AA8 <sub>H</sub> to 003AAF <sub>H</sub>	003CA8 <sub>H</sub> to 003CAF <sub>H</sub>	003EA8 <sub>H</sub> to 003EAF <sub>H</sub>	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036B0 <sub>H</sub> to 0036B7 <sub>H</sub>	0038B0 <sub>H</sub> to 0038B7 <sub>H</sub>	003AB0 <sub>H</sub> to 003AB7 <sub>H</sub>	003CB0 <sub>H</sub> to 003CB7 <sub>H</sub>	003EB0 <sub>H</sub> to 003EB7 <sub>H</sub>	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036B8 <sub>H</sub> to 0036BF <sub>H</sub>	0038B8 <sub>H</sub> to 0038BF <sub>H</sub>	003AB8 <sub>H</sub> to 003ABF <sub>H</sub>	003CB8 <sub>H</sub> to 003CBF <sub>H</sub>	003EB8 <sub>H</sub> to 003EBF <sub>H</sub>	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036C0 <sub>H</sub> to 0036C7 <sub>H</sub>	0038C0 <sub>H</sub> to 0038C7 <sub>H</sub>	003AC0 <sub>H</sub> to 003AC7 <sub>H</sub>	003CC0 <sub>H</sub> to 003CC7 <sub>H</sub>	003EC0 <sub>H</sub> to 003EC7 <sub>H</sub>	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036C8 <sub>H</sub> to 0036CF <sub>H</sub>	0038C8 <sub>H</sub> to 0038CF <sub>H</sub>	003AC8 <sub>H</sub> to 003ACF <sub>H</sub>	003CC8 <sub>H</sub> to 003CCF <sub>H</sub>	003EC8 <sub>H</sub> to 003ECF <sub>H</sub>	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036D0 <sub>H</sub> to 0036D7 <sub>H</sub>	0038D0 <sub>H</sub> to 0038D7 <sub>H</sub>	003AD0 <sub>H</sub> to 003AD7 <sub>H</sub>	003CD0 <sub>H</sub> to 003CD7 <sub>H</sub>	003ED0 <sub>H</sub> to 003ED7 <sub>H</sub>	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036D8 <sub>H</sub> to 0036DF <sub>H</sub>	0038D8 <sub>H</sub> to 0038DF <sub>H</sub>	003AD8 <sub>H</sub> to 003ADF <sub>H</sub>	003CD8 <sub>H</sub> to 003CDF <sub>H</sub>	003ED8 <sub>H</sub> to 003EDF <sub>H</sub>	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036E0 <sub>H</sub> to 0036E7 <sub>H</sub>	0038E0 <sub>H</sub> to 0038E7 <sub>H</sub>	003AE0 <sub>H</sub> to 003AE7 <sub>H</sub>	003CE0 <sub>H</sub> to 003CE7 <sub>H</sub>	003EE0 <sub>H</sub> to 003EE7 <sub>H</sub>	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036E8 <sub>H</sub> to 0036EF <sub>H</sub>	0038E8 <sub>H</sub> to 0038EF <sub>H</sub>	003AE8 <sub>H</sub> to 003AEF <sub>H</sub>	003CE8 <sub>H</sub> to 003CEF <sub>H</sub>	003EE8 <sub>H</sub> to 003EEF <sub>H</sub>	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>

# MB90390 Series

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
0036F0 <sub>H</sub> to 0036F7 <sub>H</sub>	0038F0 <sub>H</sub> to 0038F7 <sub>H</sub>	003AF0 <sub>H</sub> to 003AF7 <sub>H</sub>	003CF0 <sub>H</sub> to 003CF7 <sub>H</sub>	003EF0 <sub>H</sub> to 003EF7 <sub>H</sub>	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
0036F8 <sub>H</sub> to 0036FF <sub>H</sub>	0038F8 <sub>H</sub> to 0038FF <sub>H</sub>	003AF8 <sub>H</sub> to 003AFF <sub>H</sub>	003CF8 <sub>H</sub> to 003CFF <sub>H</sub>	003EF8 <sub>H</sub> to 003EFF <sub>H</sub>	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>



## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI <sup>2</sup> OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC <sub>H</sub>	—	—
INT9 instruction	N/A	#09	FFFFD8 <sub>H</sub>	—	—
Exception	N/A	#10	FFFFD4 <sub>H</sub>	—	—
Time Base Timer	N/A	#11	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
External Interrupt INT0 to INT7	○	#12	FFFFCC <sub>H</sub>		
CAN 0 RX	N/A	#13	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
CAN 0 TX/NS	N/A	#14	FFFFC4 <sub>H</sub>		
CAN 1 RX	N/A	#15	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
CAN 1 TX/NS	N/A	#16	FFFFBC <sub>H</sub>		
PPG 0/1 / (CAN 2 RX)	N/A	#17	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
PPG 2/3 / (CAN 2 TX/NS)	N/A	#18	FFFFB4 <sub>H</sub>		
PPG 4/5 / (CAN 3 RX)	N/A	#19	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
PPG 6/7 / (CAN 3 TX/NS)	N/A	#20	FFFFAC <sub>H</sub>		
PPG 8/9 / (CAN 4 RX)	N/A	#21	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
PPG A/B / (CAN 4 TX/NS)	N/A	#22	FFFFA4 <sub>H</sub>		
16-bit Reload Timer 0	○	#23	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
16-bit Reload Timer 1	○	#24	FFFF9C <sub>H</sub>		
Input Capture 0/1	○	#25	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
Output compare 0/1	○	#26	FFFF94 <sub>H</sub>		
Input Capture 2/3 / Output Compare 6	○	#27	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
Output Compare 2/3	○	#28	FFFF8C <sub>H</sub>		
Input Capture 4/5 / Output Compare 7	○	#29	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
Output Compare 4/5 /I <sup>2</sup> C	○	#30	FFFF84 <sub>H</sub>		
A/D Converter	○	#31	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
I/O Timer 0/1 / Watch Timer	N/A	#32	FFFF7C <sub>H</sub>		
Serial I/O	○	#33	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
Sound Generator	N/A	#34	FFFF74 <sub>H</sub>		
UART 0 RX	◎	#35	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
UART 0 TX	○	#36	FFFF6C <sub>H</sub>		
UART 1 RX	◎	#37	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
UART 1 TX	○	#38	FFFF64 <sub>H</sub>		

(Continued)

# MB90390 Series

(Continued)

Interrupt cause	EI <sup>2</sup> OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
(UART 2 RX) / UART 3 RX	○	#39	FFFF60 <sub>H</sub>	ICR14	0000BE <sub>H</sub>
(UART 2 TX) / UART 3 TX	○	#40	FFFF5C <sub>H</sub>		
Flash Memory	N/A	#41	FFFF58 <sub>H</sub>	ICR15	0000BF <sub>H</sub>
Delayed interrupt	N/A	#42	FFFF54 <sub>H</sub>		

○ : The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal.

○ : The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal. A stop request is available.

N/A : The interrupt request flag is not cleared by the EI<sup>2</sup>OS interrupt clear signal.

Note : For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI<sup>2</sup>OS interrupt clear signal.

At the end of EI<sup>2</sup>OS, the EI<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI<sup>2</sup>OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the EI<sup>2</sup>OS for this interrupt number.

If EI<sup>2</sup>OS is enabled, EI<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI<sup>2</sup>OS, the other interrupt should be disabled.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}^{*2}$
	$AV_{RH}$ , $AV_{RL}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}$ , $AV_{CC} \geq AV_{RL}$ , $AV_{RH} \geq AV_{RL}$
	$DV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} \geq DV_{CC}$
Input voltage*1	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	$I_{CLAMP}$	-4.0	+4.0	mA	*6
Total Maximum Clamp Current	$\sum  I_{CLAMP} $	—	40	mA	*6
“L” level maximum output current	$I_{OL1}$	—	15	mA	Normal outputs*4
“L” level average output current	$I_{OLAV1}$	—	4	mA	Normal outputs, average value
“L” level maximum output current	$I_{OL2}$	—	40	mA	High current outputs*5
“L” level average output current	$I_{OLAV2}$	—	30	mA	High current outputs, average value
“L” level maximum overall output current	$\sum I_{OL1}$	—	100	mA	Sum of all normal outputs
“L” level maximum overall output current	$\sum I_{OL2}$	—	330	mA	Sum of all high current outputs
“L” level average overall output current	$\sum I_{OLAV1}$	—	50	mA	Sum of all normal outputs, average value
“L” level average overall output current	$\sum I_{OLAV2}$	—	250	mA	Sum of all high current outputs, average value
“H” level maximum output current	$I_{OH1}$	—	-15	mA	Normal outputs*4
“H” level average output current	$I_{OHAV1}$	—	-4	mA	Normal outputs, average value
“H” level maximum output current	$I_{OH2}$	—	-40	mA	High current outputs*5
“H” level average output current	$I_{OHAV2}$	—	-30	mA	High current outputs, average value
“H” level maximum overall output current	$\sum I_{OH1}$	—	-100	mA	Sum of all normal outputs
“H” level maximum overall output current	$\sum I_{OH2}$	—	-330	mA	Sum of all high current outputs
“H” level average overall output current	$\sum I_{OHAV1}$	—	-50	mA	Sum of all normal outputs, average value
“H” level average overall output current	$\sum I_{OHAV2}$	—	-250	mA	Sum of all high current outputs, average value
Power consumption	$P_D$	—	800	mW	MB90F394H(A)/MB90394HA
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{STG}$	-55	+150	°C	

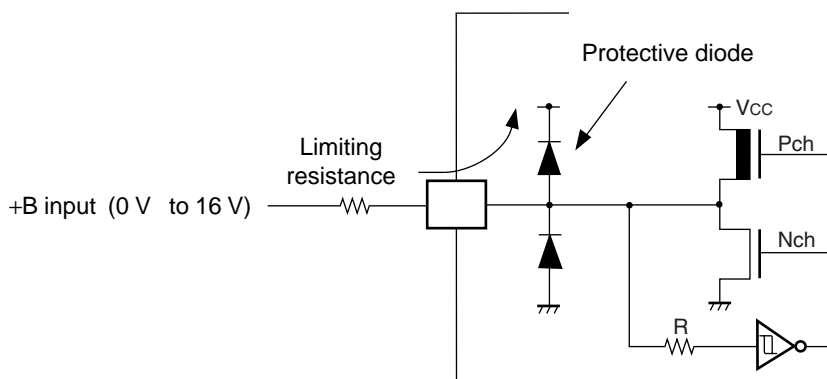
(Continued)

# MB90390 Series

(Continued)

- \*1 : The parameter is based on  $V_{SS} = AV_{SS} = DV_{SS} = 0.0 \text{ V}$ .
- \*2 : Set  $AV_{CC}$  and  $V_{CC}$  to the same voltage. Make sure that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  when the power is switched on.
- \*3 :  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3 \text{ V}$ .  $V_I$  should not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating. For ports P70 to P77, P80 to P87 and PA0 to PA7,  $V_I$  and  $V_O$  should not exceed  $DV_{CC} + 0.3 \text{ V}$ .
- \*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P90 to P97, PB0 to PB7
- \*5 : Applicable to pins : P70 to P77, P80 to P87, PA0 to PA7
- \*6 :
  - Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7
  - Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the +B input pin open.
  - Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
  - Sample recommended circuits:

• Input/output equivalent circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Conditions

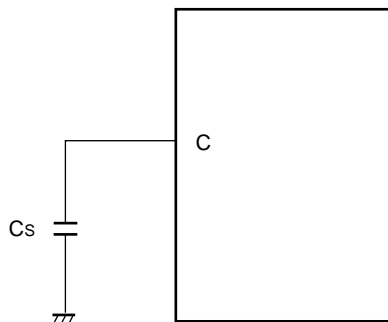
( $V_{SS} = AV_{SS} = DV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}$ , $AV_{CC}$	4.5	5.0	5.5	V	Under normal operation
		4.0	5.0	5.5	V	Under normal operation, when not using the A/D converter
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not programming or erasing Flash
		2.0	—	5.5	V	Retain RAM data in stop mode
Smoothing capacitor	$C_S$	0.1	—	1.0	$\mu\text{F}$	MB90F394H(A)/MB90394HA*
Operating temperature	$T_A$	-40	—	+85	$^{\circ}\text{C}$	

\* : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the  $V_{CC}$  pin (pin 15) , use a bypass capacitor that has a larger capacity than that of  $C_S$ . On the other  $V_{CC}$  pin (pin 105) , use a bypass capacitor of about 0.1  $\mu\text{F}$ .

Refer to the following figure for connection of smoothing capacitor  $C_S$ .

### • C Pin Connection Diagram



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB90390 Series

## 3. DC Characteristics

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	$V_{IHS}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS Hysteresis input levels are selected (except SIN and I <sup>2</sup> C pins of MB90394HA)
	$V_{IHS}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	MB90394HA : SIN (UART, SIO) and I <sup>2</sup> C input pins if CMOS Hysteresis levels are selected
	$V_{IHA}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if AUTOMOTIVE Hysteresis input levels are selected
	$V_{IHR}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input "L" voltage	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS Hysteresis input levels are selected (except SIN and I <sup>2</sup> C pins of MB90394HA)
	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	MB90394HA : SIN (UART, SIO) and I <sup>2</sup> C input pins if CMOS Hysteresis levels are selected
	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if AUTOMOTIVE Hysteresis input levels are selected
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output "H" voltage	$V_{OH1}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	

(Continued)

# MB90390 Series

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output "H" voltage	$V_{OH2}$	High current outputs	$DV_{CC} = 4.5\text{ V}$ , $I_{OH2} = -40.0\text{ mA}$	$DV_{CC} - 0.5$	—	—	V	$T_A = -40\text{ }^\circ\text{C}$
			$DV_{CC} = 4.5\text{ V}$ , $I_{OH2} = -30.0\text{ mA}$					$T_A = +25\text{ }^\circ\text{C}$
			$DV_{CC} = 4.5\text{ V}$ , $I_{OH2} = -30.0\text{ mA}$					$T_A = +85\text{ }^\circ\text{C}$
Output "L" voltage	$V_{OL1}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
Output "L" voltage	$V_{OL2}$	High current outputs	$DV_{CC} = 4.5\text{ V}$ , $I_{OL2} = 40.0\text{ mA}$	—	—	0.5	V	$T_A = -40\text{ }^\circ\text{C}$
			$DV_{CC} = 4.5\text{ V}$ , $I_{OL2} = 30.0\text{ mA}$					$T_A = +25\text{ }^\circ\text{C}$
			$DV_{CC} = 4.5\text{ V}$ , $I_{OL2} = 30.0\text{ mA}$					$T_A = +85\text{ }^\circ\text{C}$
Input leak current	$I_{IL}$	—	$V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_i < V_{CC}$	-5	—	+5	$\mu\text{A}$	
Power supply current*	$I_{CC}$	$V_{CC}$	$V_{CC} = 5.0\text{ V}$ , Internal frequency : 20 MHz, At normal operation.	—	50	70	mA	MB90394HA/ MB90F394H(A)
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At normal operation.	—	60	85	mA	MB90394HA/ MB90F394H(A)
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 20 MHz, At writing Flash memory.	—	65	85	mA	MB90F394H(A)
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 20 MHz, At erasing Flash memory.	—	70	90	mA	MB90F394H(A)
	$I_{CCS}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At Sleep mode.	—	27	36	mA	MB90394HA/ MB90F394H(A)

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# MB90390 Series

(Continued)

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I <sub>CTS</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency : 2 MHz, At Main Timebase timer mode	—	0.3	0.55	mA	MB90394HA/ MB90F394H(A)
	I <sub>CTSPLL6</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At PLL Timebase timer mode, external frequency = 4 MHz	—	5	7	mA	MB90394HA/ MB90F394H(A)
	I <sub>CCH</sub>		V <sub>CC</sub> = 5.0 V, At Stop mode, T <sub>A</sub> = +25°C	—	5	30	μA	MB90394HA/ MB90F394H(A)
Input capacitance	C <sub>IN</sub>	Other than C, AV <sub>CC</sub> , AV <sub>SS</sub> , AVRH, AVRL, V <sub>CC</sub> , V <sub>SS</sub> , DV <sub>CC</sub> , DV <sub>SS</sub> , P70 to P77, P80 to P87, PA0 to PA7	—	—	5	15	pF	
		P70 to P77, P80 to P87, PA0 to PA7	—	—	15	30	pF	

\* : The power supply current is measured with an external clock.



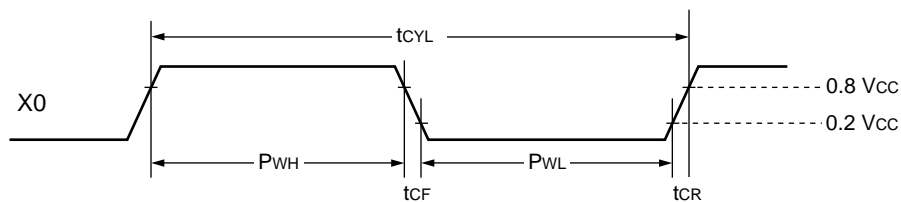
## 4. AC Characteristics

### (1) Clock Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$ )

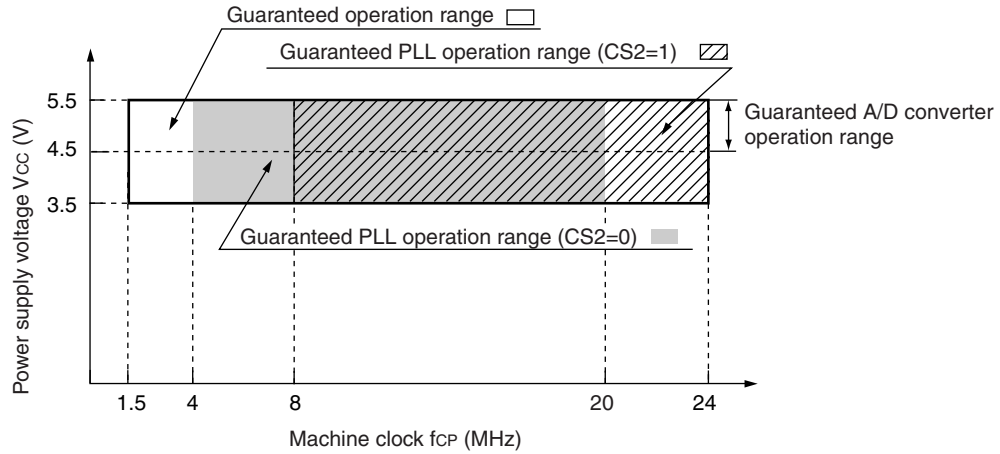
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_c$	X0, X1	3	—	8	MHz	When using a crystal oscillator or a ceramic oscillator
		X0	3	—	12	MHz	When using an external clock
Clock cycle time	$t_{CYL}$	X0, X1	125	—	333	ns	When using a crystal oscillator or a ceramic oscillator
		X0	83.33	—	333	ns	When using an external clock
Input clock pulse width	$P_{WH}$ , $P_{WL}$	X0	20	—	—	ns	Duty ratio is about 30% to 70%.
Input clock rise and fall time	$t_{CR}$ , $t_{CF}$	X0	—	—	5	ns	When using external clock
Machine clock frequency	$f_{CP}$	—	1.5	—	24	MHz	Except programming or erasing Flash memory. When using clock modulation, be sure that the maximum momentary frequency $F_{max}$ does not exceed 24 MHz. Refer to the Clock Modulator chapter of the Hardware Manual.
		—	1.5	—	20	MHz	When programming or erasing Flash memory. Be sure that the maximum momentary frequency $F_{max}$ does not exceed 20 MHz.
Machine clock cycle time	$t_{CP}$	—	41.67	—	666	ns	Except programming or erasing Flash memory.
		—	50	—	666	ns	When programming or erasing Flash memory.

#### • Clock Timing



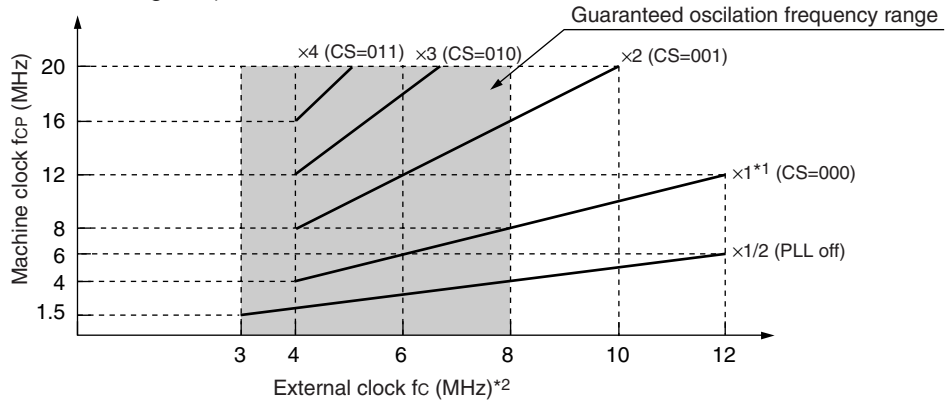
# MB90390 Series

- Guaranteed PLL operation range

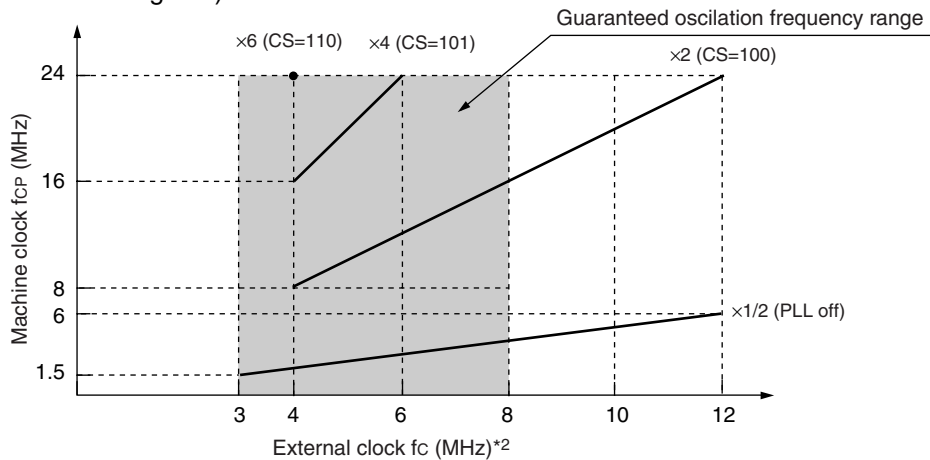


## Guaranteed operation range of MB90394HA/MB90F394H(A)

- CS2 (bit 0 in PSCCR register) = 0



- CS2 (bit 0 in PSCCR register) = 1



\*1 : PLL  $\times 1$  guaranteed operation range is from 4.0 MHz to 12 MHz.

\*2 : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 8 MHz

## External clock frequency and Machine clock frequency

## (2) Reset Standby Input

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	$t_{RSTL}$	$\overline{RST}$	$16 t_{CP}^{*1}$	—	ns	Under normal operation
			Oscillation time of oscillator <sup>*2</sup> $+ 100\ \mu\text{s} + 16 t_{CP}^{*1}$	—	ns	In Stop mode
			100	—	$\mu\text{s}$	In Time Base Timer mode

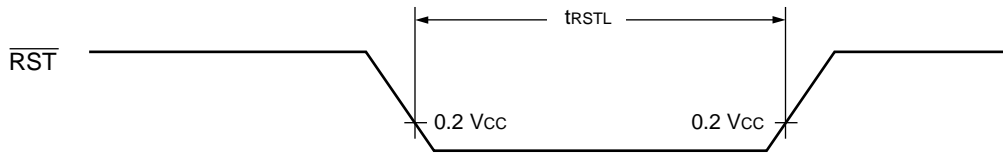
\*1 :  $t_{CP}$  is the machine clock cycle time. Refer to “(1) Clock timing”.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

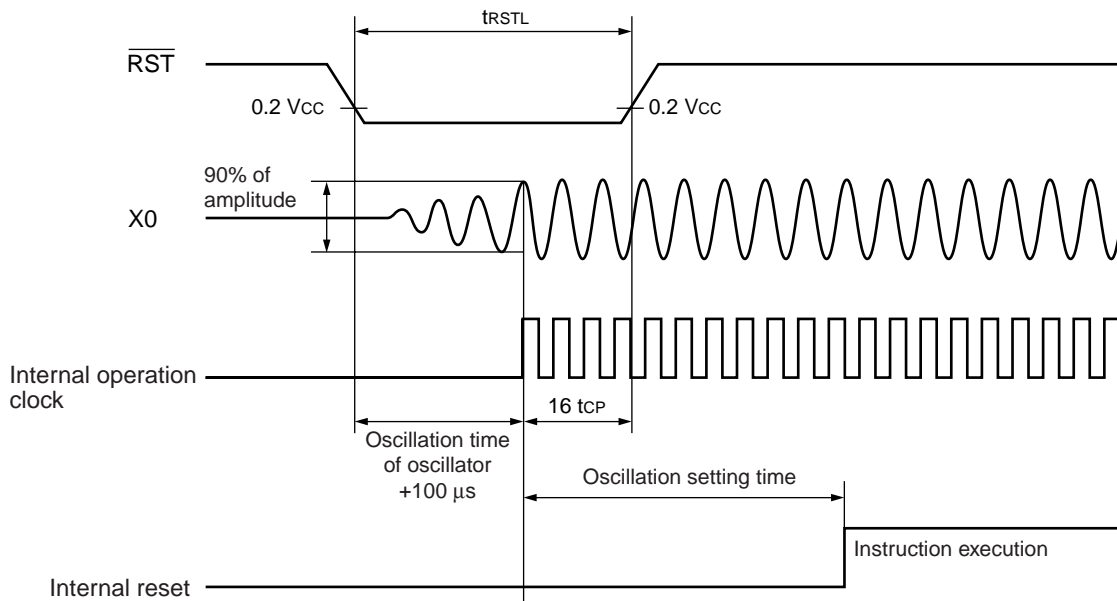
\*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.

In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. With an external clock, the oscillation time is 0 ms.

### • Under Normal Operation



### • In Stop Mode

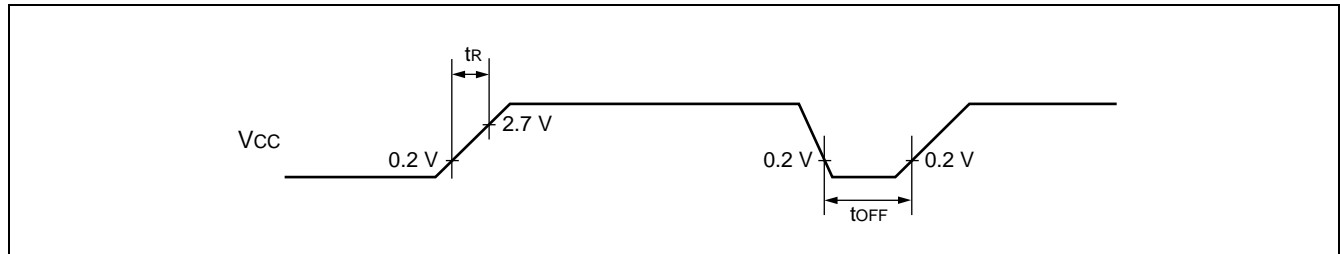


# MB90390 Series

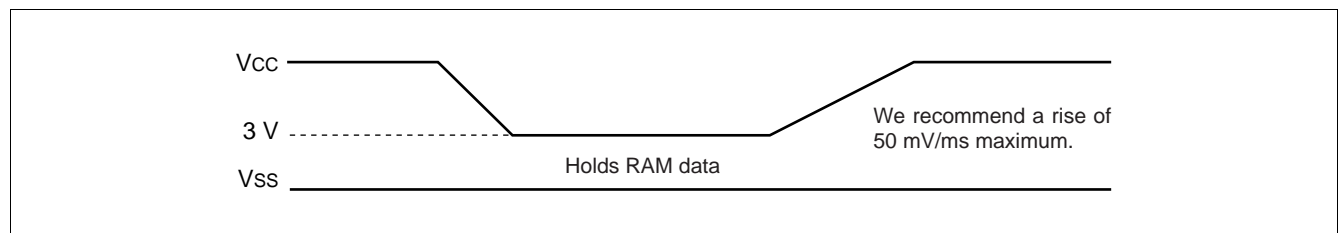
## (3) Power On Reset

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power off time	$t_{OFF}$	$V_{CC}$	—	1	—	ms	Wait time until power on



Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



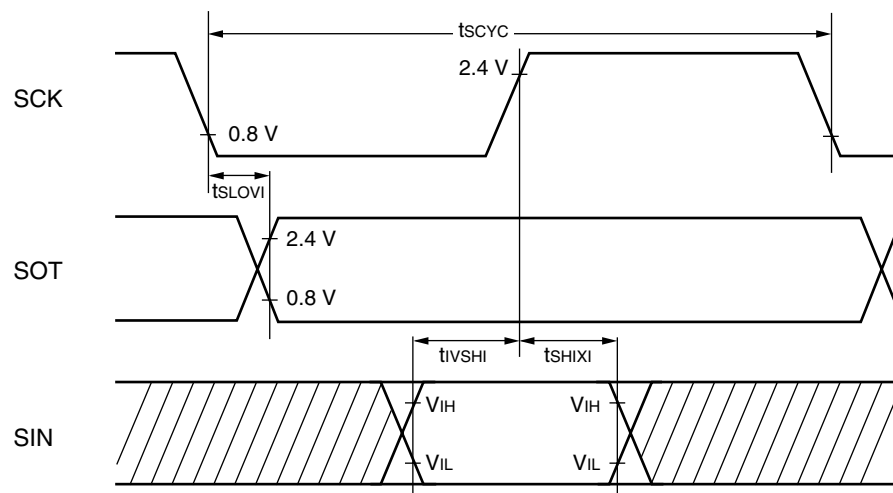
## (4) UART0/1 and Serial I/O Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK0, SCK1, SCK4	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$8\ t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK0, SCK1, SCK4, SOT0, SOT1, SOT4		-80	+80	ns	
Valid SIN → SCK ↑	$t_{VSHI}$	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		100	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIXI}$	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK0, SCK1, SCK4	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4\ t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	SCK0, SCK1, SCK4		$4\ t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCK0, SCK1, SCK4, SOT0, SOT1, SOT4		—	150	ns	
Valid SIN → SCK ↑	$t_{VSHI}$	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIXE}$	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	

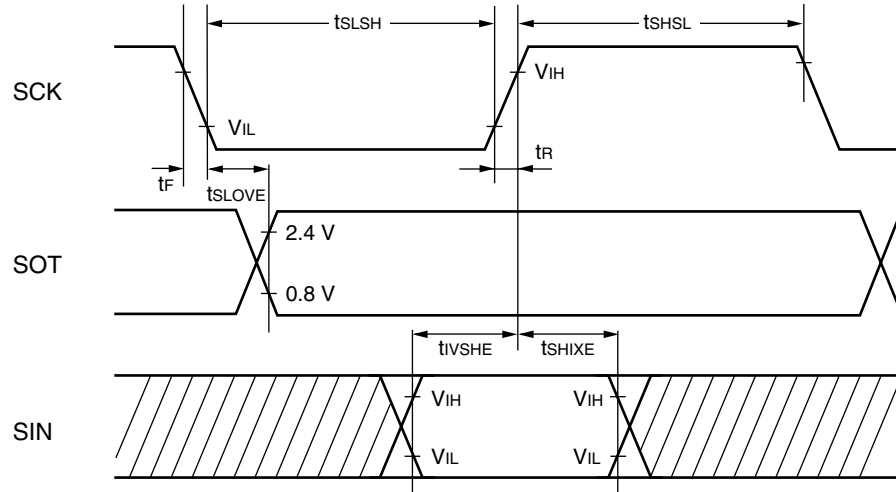
- Notes :
- Above rating is the case of CLK synchronized mode.
  - $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is the machine clock cycle time. Refer to "(1) Clock timing".

### • Internal Shift Clock Mode



# MB90390 Series

- External Shift Clock Mode



## (5) UART2/3 (LIN/SCI)

- Bit setting : ESCR2/3 : SCES = 0, ECCR2/3 : SCDE = 0

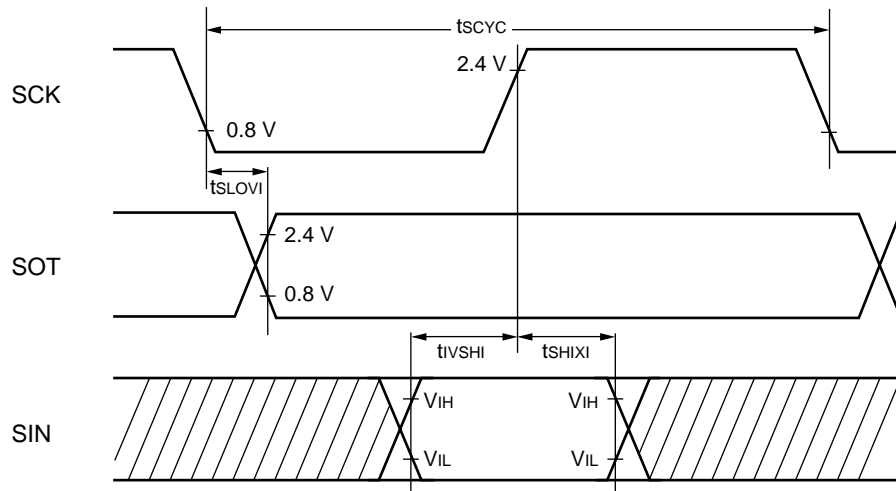
( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK2/3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK2/3, SOT2/3		-50	+50	ns
Valid SIN → SCK ↑	$t_{IVSHI}$	SCK2/3, SIN2/3		$t_{CP} + 80$	—	ns
SCK ↑ → Valid SIN hold time	$t_{SHIXI}$	SCK2/3, SIN2/3		0	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK2/3	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK2/3		$t_{CP} + 10$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCK2/3, SOT2/3		—	$2 t_{CP} + 60$	ns
Valid SIN → SCK ↑	$t_{IVSHE}$	SCK2/3, SIN2/3		30	—	ns
SCK ↑ → Valid SIN hold time	$t_{SHIXE}$	SCK2/3, SIN2/3		$t_{CP} + 30$	—	ns
SCK fall time	$t_F$	SCK2/3		—	10	ns
SCK rise time	$t_R$	SCK2/3		—	10	ns

Notes : •  $C_L$  is load capacity value of pins when testing.

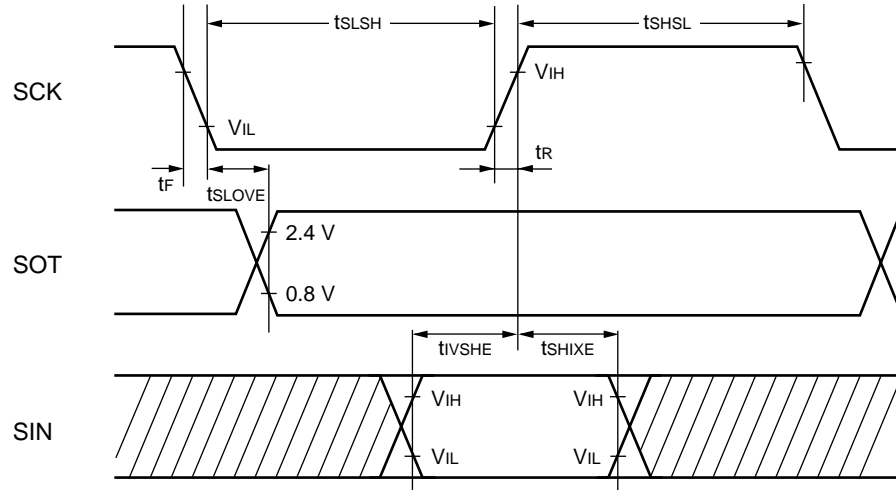
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB90390 series hardware manual".
- $t_{CP}$  is the machine clock cycle time. Refer to "(1) Clock timing".

### • Internal Shift Clock Mode



# MB90390 Series

## • External Shift Clock Mode



## • Bit setting : ESCR2/3 : SCES = 1, ECCR2/3 : SCDE = 0

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

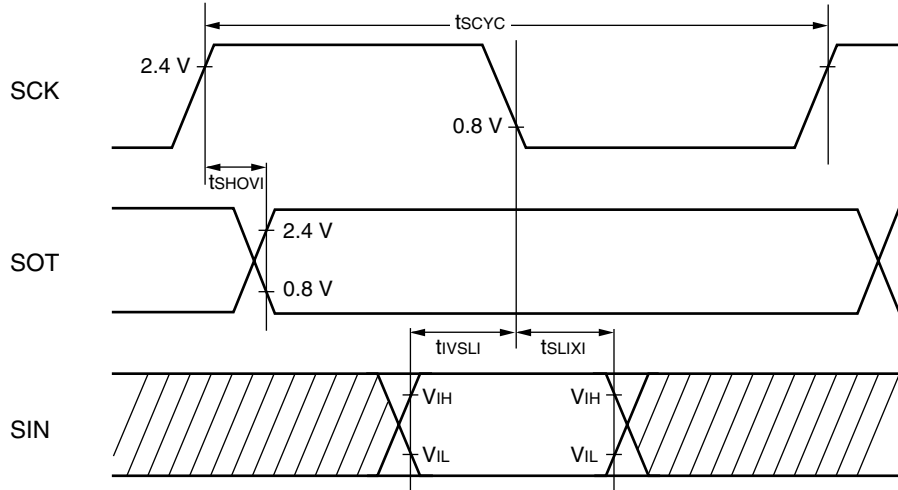
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK2/3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{CP}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK2/3, SOT2/3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK2/3, SIN2/3		$t_{CP}+80$	—	ns
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXI}$	SCK2/3, SIN2/3		0	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK2/3	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$3 t_{CP}-t_R$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK2/3		$t_{CP}+10$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCK2/3, SOT2/3		—	$2 t_{CP}+60$	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLE}$	SCK2/3, SIN2/3		30	—	ns
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXE}$	SCK2/3, SIN2/3		$t_{CP}+30$	—	ns
SCK fall time	$t_F$	SCK2/3		—	10	ns
SCK rise time	$t_R$	SCK2/3		—	10	ns

Notes : •  $C_L$  is load capacity value of pins when testing.

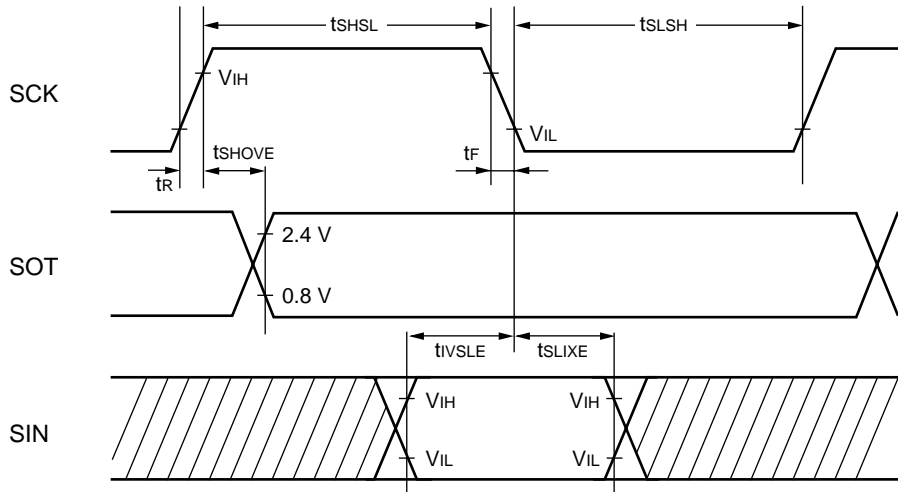
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB90390 series hardware manual".
- $t_{CP}$  is the machine clock cycle time. Refer to "(1) Clock timing".



• Internal Shift Clock Mode



• External Shift Clock Mode



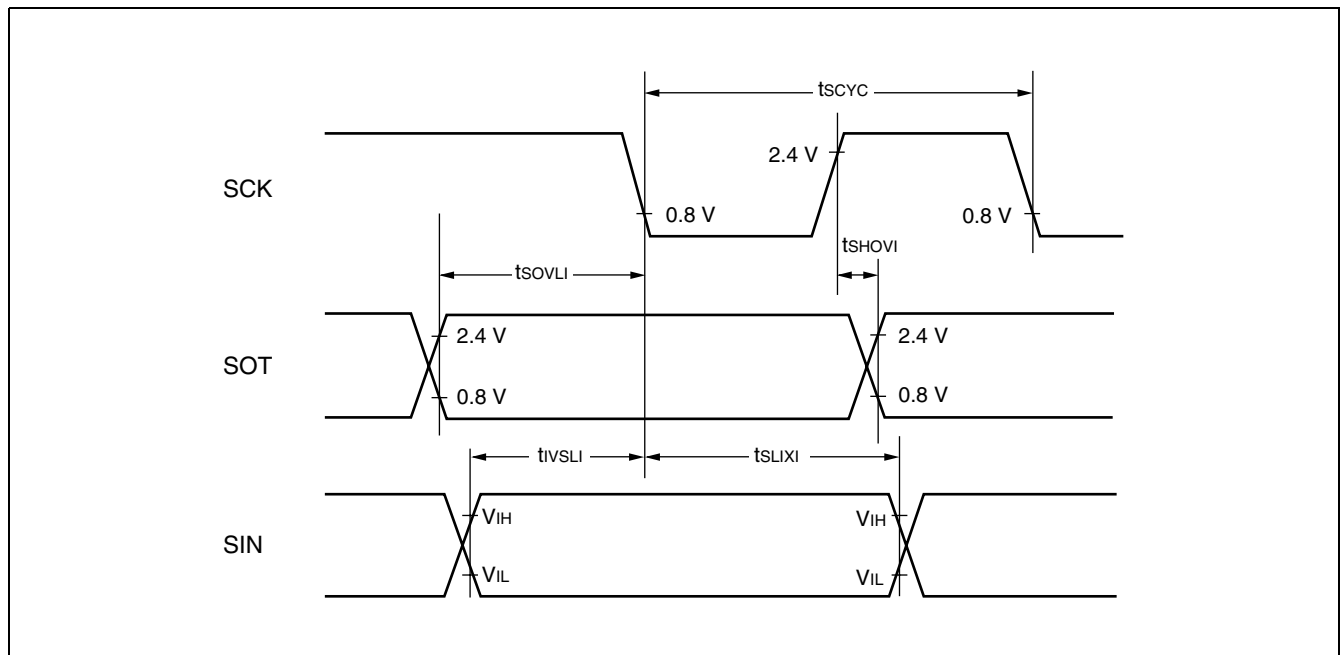
# MB90390 Series

- Bit setting : ESCR2/3 : SCES = 0, ECCR2/3 : SCDE = 1

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK2/3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{CP}$	—	ns	
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK2/3, SOT2/3		-50	+50	ns	MB90394HA, MB90V390HA/HB
				$t_{CP} - 60$	$t_{SCYC}/2 + 70 - t_{CP}$	ns	MB90F394H(A), MB90V390H
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK2/3, SIN2/3		$t_{CP} + 80$	—	ns	MB90394HA, MB90V390HA/HB
				$100 - t_{CP}$	—	ns	MB90F394H(A), MB90V390H
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXI}$	SCK2/3, SIN2/3		0	—	ns	MB90394HA, MB90V390HA/HB
				$t_{SCYC}/2$	—	ns	MB90F394H(A), MB90V390H
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK2/3, SOT2/3		$3 t_{CP} - 70$	—	ns	MB90394HA, MB90V390HA/HB
			$t_{CP} - 60$	—	ns	MB90F394H(A), MB90V390H	

- Notes :
- $C_L$  is load capacity value of pins when testing.
  - Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
  - $t_{CP}$  is the machine clock cycle time. Refer to “(1) Clock timing”.



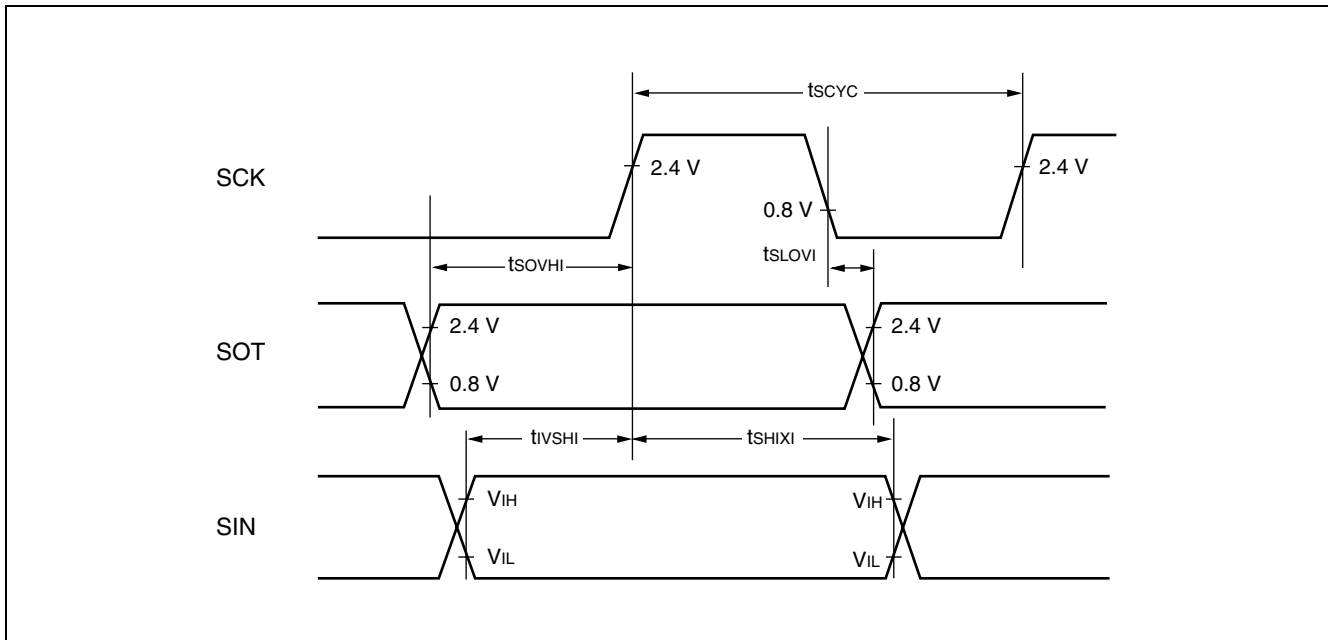
# MB90390 Series

- Bit setting : ESCR2/3 : SCES = 1, ECCR2/3 : SCDE = 1

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK2/3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{CP}$	—	ns	
SCK $\downarrow$ $\rightarrow$ SOT delay time	$t_{SLOVI}$	SCK2/3, SOT2/3		-50	+50	ns	MB90394HA, MB90V390HA/HB
				$t_{CP} - 60$	$t_{SCYC}/2 + 70 - t_{CP}$	ns	MB90F394H(A), MB90V390H
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSHI}$	SCK2/3, SIN2/3		$t_{CP} + 80$	—	ns	MB90394HA, MB90V390HA/HB
				$100 - t_{CP}$	—	ns	MB90F394H(A), MB90V390H
SCK $\uparrow$ $\rightarrow$ Valid SIN hold time	$t_{SHIXI}$	SCK2/3, SIN2/3		0	—	ns	MB90394HA, MB90V390HA/HB
				$t_{SCYC}/2$	—	ns	MB90F394H(A), MB90V390H
SOT $\rightarrow$ SCK $\uparrow$ delay time	$t_{SOVHI}$	SCK2/3, SOT2/3		$3t_{CP} - 70$	—	ns	MB90394HA, MB90V390HA/HB
			$t_{CP} - 60$	—	ns	MB90F394H(A), MB90V390H	

- Notes :
- $C_L$  is load capacity value of pins when testing.
  - Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
  - $t_{CP}$  is the machine clock cycle time. Refer to “ (1) Clock timing”.



# MB90390 Series

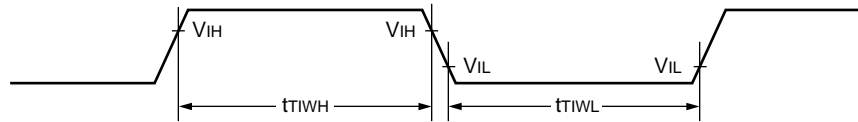
## (6) Timer Related Resource Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$	TIN0, TIN1	—	4 $t_{CP}$	—	ns	
	$t_{TIWL}$	IN0 to IN5					

Note :  $t_{CP}$  is the machine clock cycle time. Refer to “ (1) Clock timing”.

### • Timer Input Timing



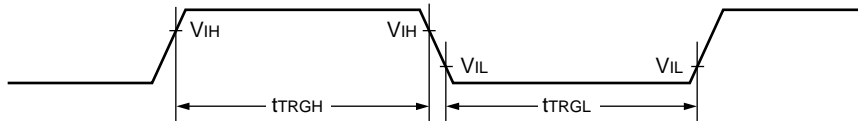
## (7) Trigger Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$	INT0 to INT7	—	200	—	ns	
	$t_{TRGL}$	ADTG	—	$t_{CP} + 200$	—	ns	

Note :  $t_{CP}$  is the machine clock cycle time. Refer to “ (1) Clock timing”.

### • Trigger Input Timing

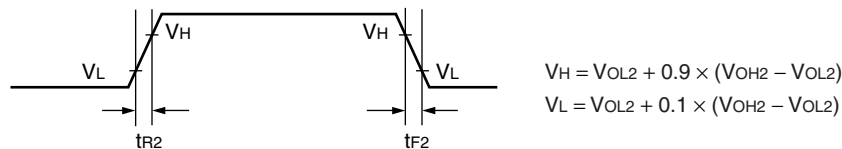


## (8) Slew Rate High Current Outputs

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{CC} = DV_{CC} = 3.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = DV_{SS} = 0\text{ V}$ )

Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	$t_{r2}$ $t_{f2}$	P70 to P77, P80 to P87, PA0 to PA7	—	15	—	—	ns	

### • Slew Rate Output Timing



## (9) I<sup>2</sup>C Timing

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>CC</sub> = 3.5 V to 5.5 V, V<sub>SS</sub> = 0 V)

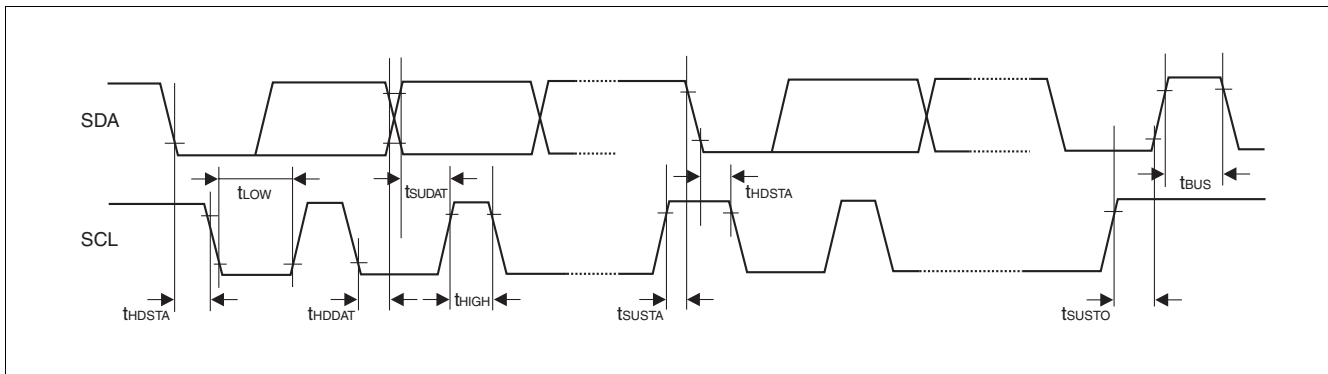
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	R = 1.3 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	—	0.6	—	μs
"L" width of the SCL clock	t <sub>LOW</sub>		4.7	—	1.3	—	μs
"H" width of the SCL clock	t <sub>HIGH</sub>		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45*2	0	0.9*3	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t <sub>BUS</sub>		4.7	—	1.3	—	μs

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : The maximum t<sub>HDDAT</sub> only has to be met if the device does not stretch the "L" width (t<sub>LOW</sub>) of the SCL signal.

\*3 : A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SUDAT</sub> ≥ 250 ns must then be met.

\*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



# MB90390 Series

## 5. A/D Converter

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$ ,  $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	$\pm 3.0$	LSB	
Nonlinearity error	—	—	—	—	$\pm 2.5$	LSB	
Differential nonlinearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero reading voltage	$V_{OT}$	AN0 to AN14	$\text{AVRL} - 1.5$	$\text{AVRL} + 0.5$	$\text{AVRL} + 2.5$	LSB	
Full scale reading voltage	$V_{FST}$	AN0 to AN14	$\text{AVRH} - 3.5$	$\text{AVRH} - 1.5$	$\text{AVRH} + 0.5$	LSB	
Compare time	—	—	3.3	—	16500	$\mu\text{s}$	
			—	$3.3 (= 66 t_{CP})$	—	$\mu\text{s}$	$f_{CP} = 20\text{ MHz}$
			—	$3.7 (= 88 t_{CP})$	—	$\mu\text{s}$	$f_{CP} = 24\text{ MHz}$
Sampling time	—	—	1.6	—	$\infty$	$\mu\text{s}$	
			—	$1.6 (= 32 t_{CP})$	—	$\mu\text{s}$	$f_{CP} = 20\text{ MHz}$
			—	$2 (= 48 t_{CP})$	—	$\mu\text{s}$	$f_{CP} = 24\text{ MHz}$
Analog port input current	$I_{AIN}$	AN0 to AN14	-1	—	+1	$\mu\text{A}$	
Analog input voltage range	$V_{AIN}$	AN0 to AN14	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	$\text{AV}_{CC}$	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	$I_A$	$\text{AV}_{CC}$	—	3.5	7.5	mA	
	$I_{AH}$	$\text{AV}_{CC}$	—	—	5	$\mu\text{A}$	*
Reference voltage current	$I_R$	AVRH	—	165	250	$\mu\text{A}$	
	$I_{RH}$	AVRH	—	—	5	$\mu\text{A}$	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

\* : When not operating A/D converter, this is the current ( $V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$ ) .

### Terminology

Conversion error : Absolute maximum conversion deviation with respect to the theoretical conversion line.

Nonlinearity : Relative maximum conversion deviation with respect to the theoretical conversion line connecting to the device unique zero reading voltage and full scale reading voltage.

Differential nonlinearity : Max conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.

Zero reading voltage : Input voltage which results in the minimum conversion value.

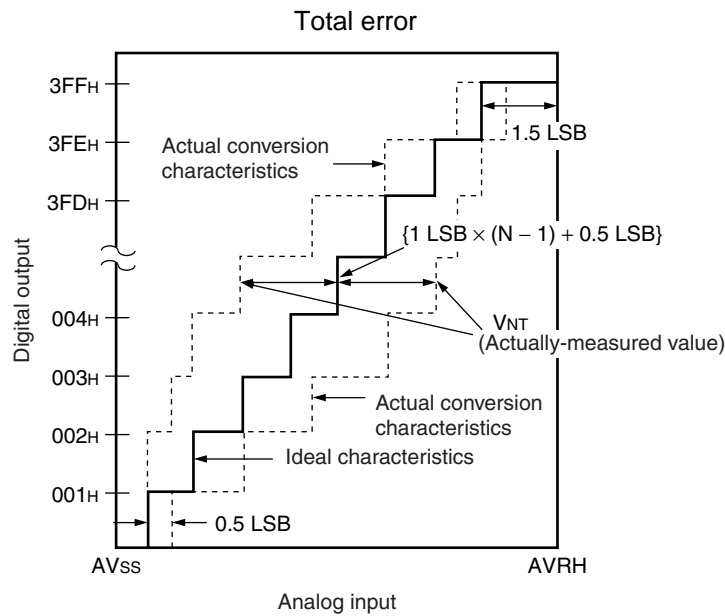
Full scale reading voltage : Input voltage which results in the maximum conversion value.

Notes : • The accuracy gets worse as  $\text{AVRH} - \text{AVRL}$  becomes smaller.

- $t_{CP}$  is the machine clock cycle time. Refer to “ (1) Clock timing” in “4. AC Characteristics”.

## 6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linear error : Deviation between a line across zero-transition line ( “00 0000 0000” ← → “00 0000 0001” ) and full-scale transition line ( “11 1111 1110” ← → “11 1111 1111” ) and actual conversion characteristics.
- Differential linear error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

N : A/D converter digital output value

$$V_{OT} (\text{Ideal value}) = AV_{SS} + 0.5 \text{ LSB [V]}$$

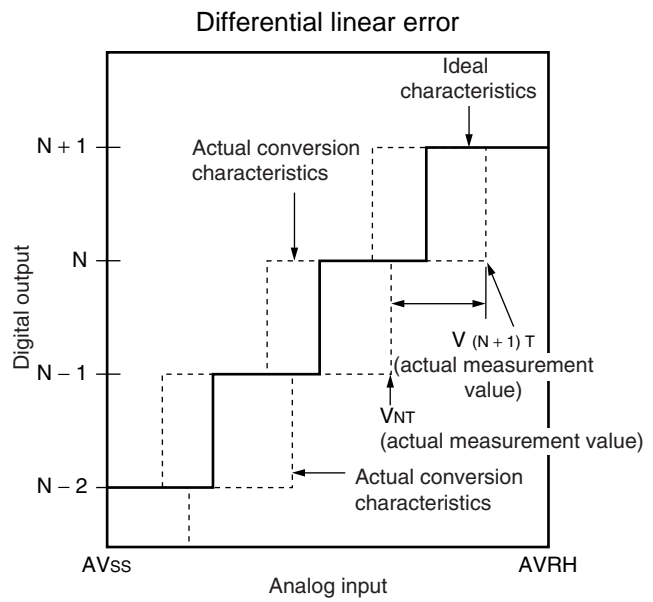
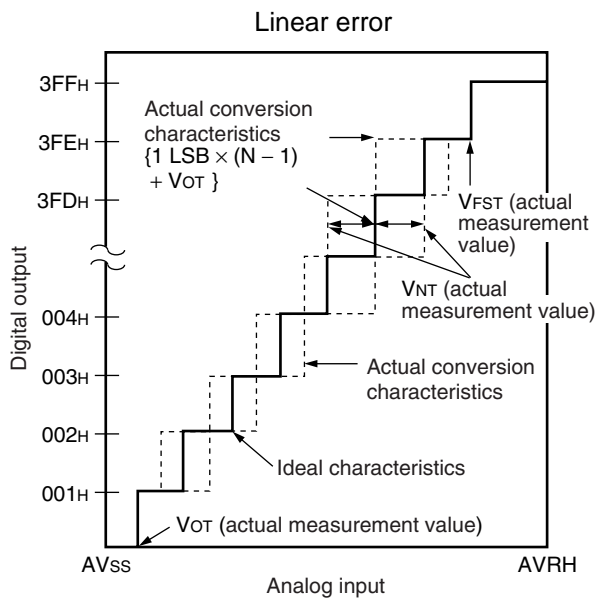
$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB [V]}$$

$V_{NT}$  : A voltage at which digital output transitions from (N - 1) to N.

(Continued)

# MB90390 Series

(Continued)



$$\text{Linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

$V_{OT}$  : Voltage at which digital output transits from "000H" to "001H."

$V_{FST}$  : Voltage at which digital output transits from "3FEH" to "3FFH."

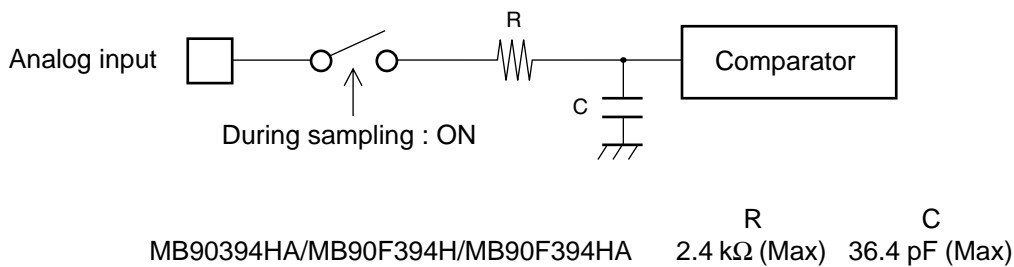


## 7. Notes on A/D Converter Section

### • About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

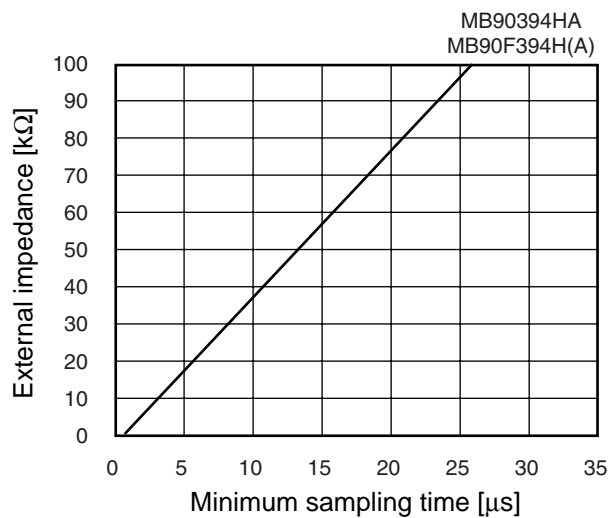
#### • Analog input circuit model



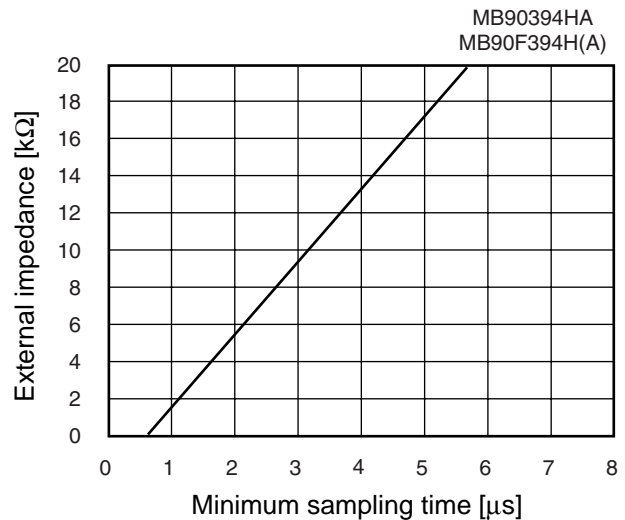
Note : The values are reference values.

#### • The relationship between the external impedance and minimum sampling time

(External impedance = 0 k $\Omega$  to 100 k $\Omega$ )



(External impedance = 0 k $\Omega$  to 20 k $\Omega$ )



#### • About the error

The accuracy gets worse as  $|AVRH - AVRL|$  becomes smaller.

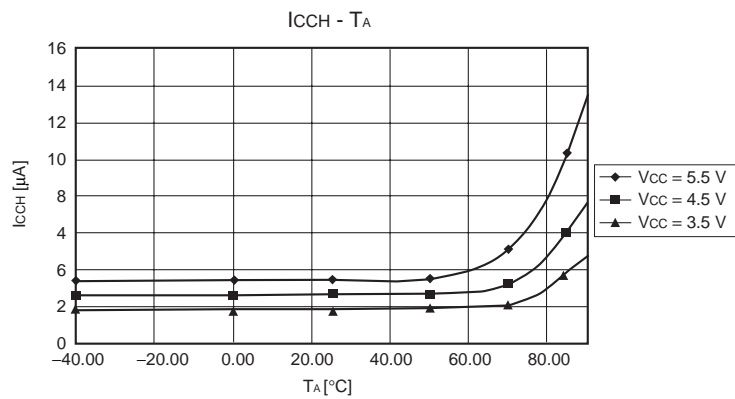
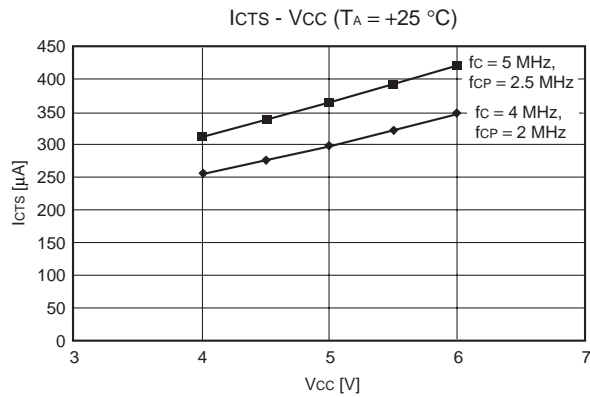
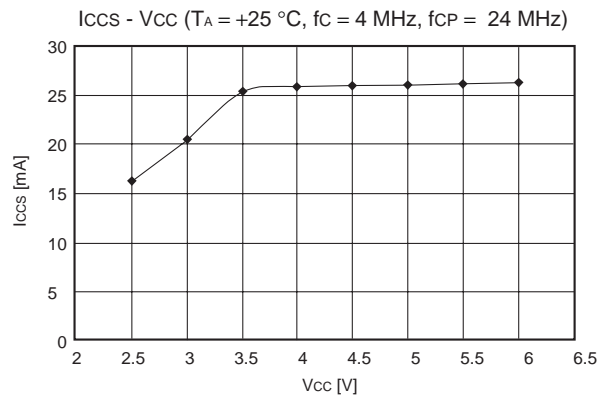
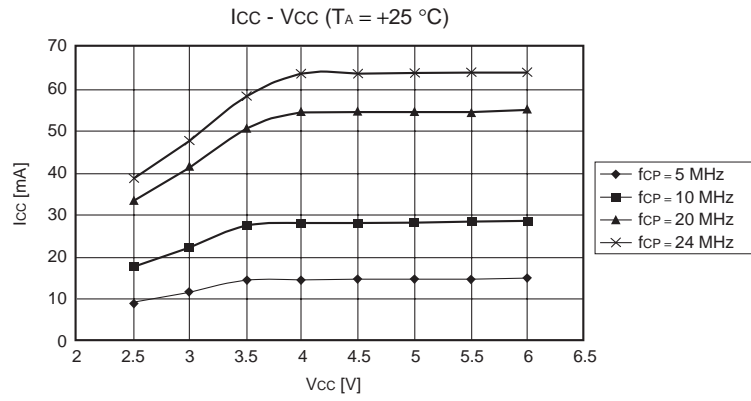
# MB90390 Series

## 8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T <sub>A</sub> = +25 °C V <sub>CC</sub> = 5.0 V	—	1	15	s	Excludes 00 <sub>H</sub> programming prior to erasure.
Chip erase time		—	9	—	s	MB90F394H, Excludes 00 <sub>H</sub> programming prior to erasure.
Word (16-bit width) programming time		—	16	3600	μs	Except for the over head time of the system.
Programs/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average T <sub>A</sub> = +85 °C	20	—	—	year	*

\* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

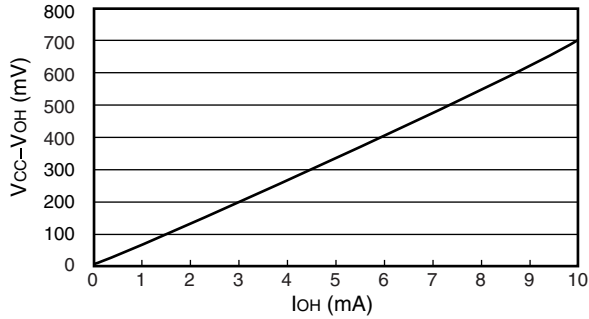
## EXAMPLE CHARACTERISTICS



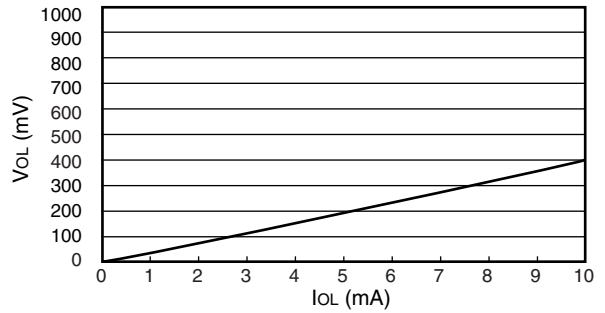
# MB90390 Series

• I/O characteristics

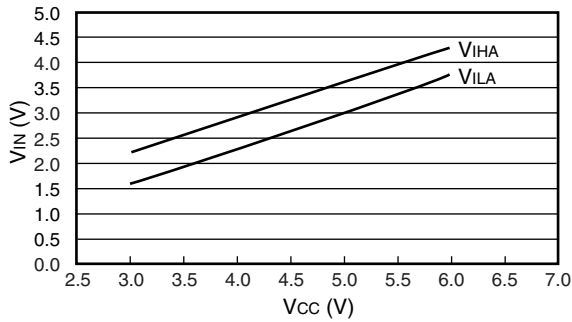
$(V_{CC}-V_{OH}) - I_{OH}$   
 $T_A = +25\text{ }^\circ\text{C}, V_{CC} = 4.5\text{ V}$



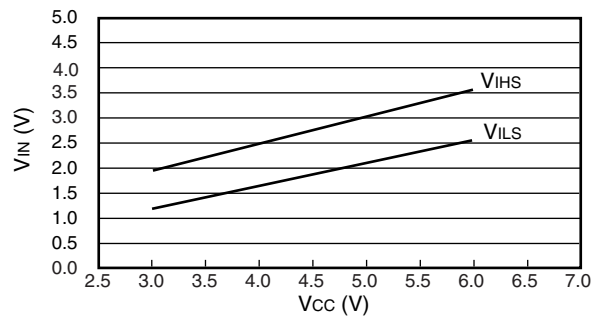
$V_{OL} - I_{OL}$   
 $T_A = +25\text{ }^\circ\text{C}, V_{CC} = 4.5\text{ V}$



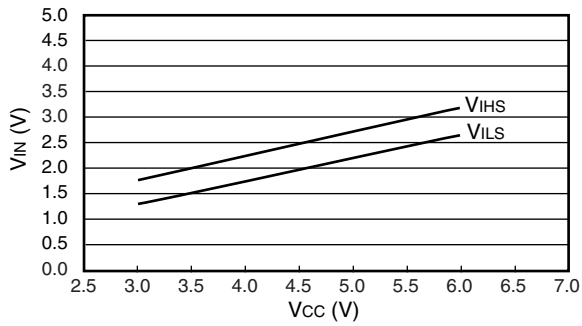
Automotive  $V_{IN} - V_{CC}$   
 $T_A = +25\text{ }^\circ\text{C}$



CMOS  $V_{IN} - V_{CC}$   
 Except UART-SIN pins and I<sup>2</sup>C pins of MB90394HA  
 $T_A = +25\text{ }^\circ\text{C}$



CMOS  $V_{IN} - V_{CC}$   
 UART-SIN pins and I<sup>2</sup>C pins of MB90394HA  
 $T_A = +25\text{ }^\circ\text{C}$

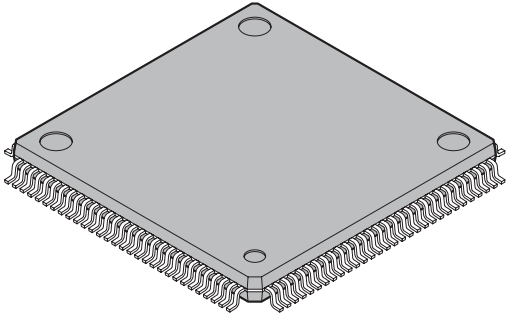


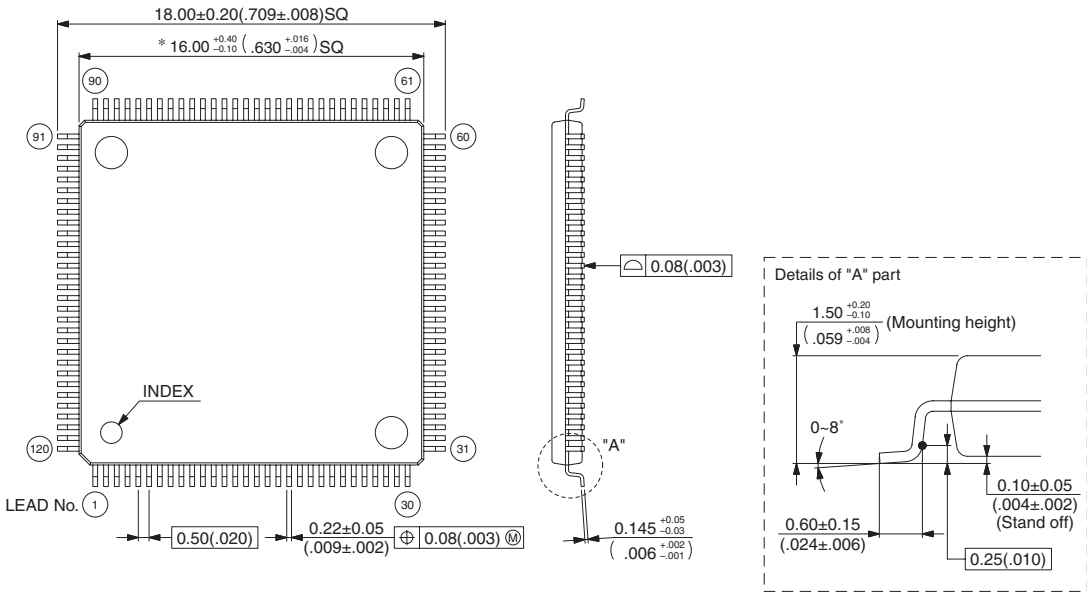
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F394HPMT	120-pin Plastic LQFP (FPT-120P-M21)	It is recommended to use MB90F394HA, because MB90F394H does not support frequency modulation, clock modulation and CAN message buffer RAM at the same time.
MB90F394HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90394HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90V390HACR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation It is recommended to use MB90V390HB, because MB90V390HA does not support clock modulation and CAN message buffer RAM at the same time.
MB90V390HBCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation
MB90V390HCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation It is recommended to use MB90V390HB, because MB90V390H does not support clock modulation and CAN message buffer RAM at the same time.

# MB90390 Series

## PACKAGE DIMENSION

<p>120-pin plastic LQFP</p>  <p>(FPT-120P-M21)</p>	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

<p>120-pin plastic LQFP (FPT-120P-M21)</p>  <p>18.00±0.20(.709±.008)SQ * 16.00<sup>+0.40</sup><sub>-0.10</sub> (.630<sup>+0.16</sup><sub>-.004</sub>)SQ</p> <p>INDEX</p> <p>LEAD No. 1</p> <p>0.50(.020)</p> <p>0.22±0.05 (.009±.002)</p> <p>0.08(.003)Ⓜ</p> <p>0.145<sup>+0.05</sup><sub>-.003</sub> (.006<sup>+0.002</sup><sub>-.001</sub>)</p> <p>0.08(.003)</p> <p>0-8°</p> <p>1.50<sup>+0.20</sup><sub>-0.10</sub> (.059<sup>+0.008</sup><sub>-.004</sub>) (Mounting height)</p> <p>0.60±0.15 (.024±.006)</p> <p>0.10±0.05 (.004±.002) (Stand off)</p> <p>0.25(.010)</p> <p>Details of "A" part</p>	<p>Note 1) * : These dimensions do not include resin protrusion. Resin protrusion is +0.25(.010) MAX(each side).</p> <p>Note 2) Pins width and pins thickness include plating thickness.</p> <p>Note 3) Pins width do not include tie bar cutting remainder.</p>
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Dimensions in mm (inches).  
Note: The values in parentheses are reference values.

# MB90390 Series

The information for microcontroller supports is shown in the following homepage.  
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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