



# Log-Taper, 100-Tap Digitally Programmable Potentiometer (DPP™)

## FEATURES

- 100-position, log-taper potentiometer
- Non-volatile EEPROM wiper storage
- 10nA ultra-low standby current
- Single-supply operation: 2.5V – 5.5V
- Increment Up/Down serial interface
- Resistance value: 32kΩ
- Available in 8-pin MSOP, TSSOP, SOIC and DIP packages

## APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Audio volume control
- Sensor adjustment
- Motor controls and feedback systems
- Programmable analog functions

For Ordering Information details, see page 11.

## DESCRIPTION

The CAT5116 is a log-taper single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers.

Ideal for automated adjustments on high volume production lines, DPP ICs are well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

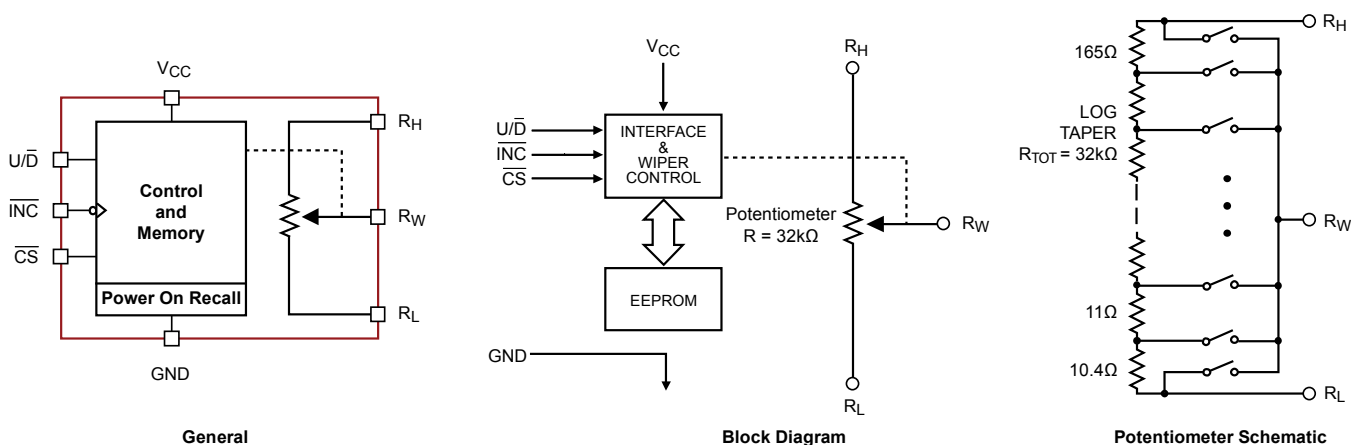
The CAT5116 contains a 100-tap series resistor array connected between two terminals  $R_H$  and  $R_L$ . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper,  $R_W$ .

The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting.

Wiper-control of the CAT5116 is accomplished with three input control pins,  $\overline{CS}$ ,  $\overline{U/D}$ , and  $\overline{INC}$ . The  $\overline{INC}$  input increments the wiper in the direction which is determined by the logic state of the  $\overline{U/D}$  input. The  $\overline{CS}$  input is used to select the device and also store the wiper position prior to power down.

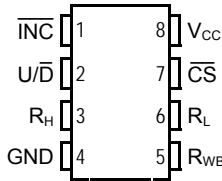
The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor.

## FUNCTIONAL DIAGRAM

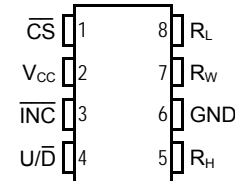


**PIN CONFIGURATION**

PDIP 8-Lead (L)  
SOIC 8 Lead (V)  
MSOP 8 Lead (Z)



TSSOP 8 Lead (Y)



**PIN DESCRIPTIONS**

| Name                           | Function                    |
|--------------------------------|-----------------------------|
| $\overline{\text{INC}}$        | Increment Control           |
| $\text{U}/\overline{\text{D}}$ | Up/Down Control             |
| $\text{R}_\text{H}$            | Potentiometer High Terminal |
| GND                            | Ground                      |
| $\text{R}_\text{W}$            | Buffered Wiper Terminal     |
| $\text{R}_\text{L}$            | Potentiometer Low Terminal  |
| $\overline{\text{CS}}$         | Chip Select                 |
| $\text{V}_\text{CC}$           | Supply Voltage              |

**PIN DESCRIPTION**

**$\overline{\text{INC}}$ :** Increment Control Input

The  $\overline{\text{INC}}$  input moves the wiper in the up or down direction determined by the condition of the  $\text{U}/\overline{\text{D}}$  input.

**$\text{U}/\overline{\text{D}}$ :** Up/Down Control Input

The  $\text{U}/\overline{\text{D}}$  input controls the direction of the wiper movement. When in a high state and  $\overline{\text{CS}}$  is low, any high-to-low transition on  $\overline{\text{INC}}$  will cause the wiper to move one increment toward the  $\text{R}_\text{H}$  terminal. When in a low state and  $\overline{\text{CS}}$  is low, any high-to-low transition on  $\overline{\text{INC}}$  will cause the wiper to move one increment towards the  $\text{R}_\text{L}$  terminal.

**$\text{R}_\text{H}$ :** High End Potentiometer Terminal

$\text{R}_\text{H}$  is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the  $\text{R}_\text{L}$  terminal. Voltage applied to the  $\text{R}_\text{H}$  terminal cannot exceed the supply voltage,  $\text{V}_\text{CC}$  or go below ground, GND.

**$\text{R}_\text{W}$ :** Wiper Potentiometer Terminal

$\text{R}_\text{W}$  is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs,  $\overline{\text{INC}}$ ,  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{CS}}$ . Voltage applied to the  $\text{R}_\text{W}$  terminal cannot exceed the supply voltage,  $\text{V}_\text{CC}$  or go below ground, GND.

**$\text{R}_\text{L}$ :** Low End Potentiometer Terminal

$\text{R}_\text{L}$  is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the  $\text{R}_\text{H}$  terminal. Voltage applied to the  $\text{R}_\text{L}$  terminal cannot exceed the supply voltage,  $\text{V}_\text{CC}$  or go below ground, GND.  $\text{R}_\text{L}$  and  $\text{R}_\text{H}$  are electrically interchangeable.

**$\overline{\text{CS}}$ :** Chip Select

The chip select input is used to activate the control input of the CAT5116 and is active low. When in a high state, activity on the  $\overline{\text{INC}}$  and  $\text{U}/\overline{\text{D}}$  inputs will not affect or change the position of the wiper.

**DEVICE OPERATION**

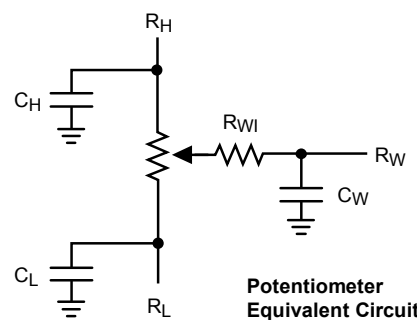
The CAT5116 operates like a digitally controlled potentiometer with  $\text{R}_\text{H}$  and  $\text{R}_\text{L}$  equivalent to the high and low terminals and  $\text{R}_\text{W}$  equivalent to the mechanical potentiometer's wiper. There are 100 tap positions including the resistor end points,  $\text{R}_\text{H}$  and  $\text{R}_\text{L}$ . There are 99 resistor elements connected in series between the  $\text{R}_\text{H}$  and  $\text{R}_\text{L}$  terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs,  $\overline{\text{INC}}$ ,  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{CS}}$ . These inputs control a seven-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the  $\overline{\text{INC}}$  and  $\overline{\text{CS}}$  inputs.

With  $\overline{\text{CS}}$  set LOW the CAT5116 is selected and will respond to the  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{INC}}$  inputs. HIGH to LOW transitions on  $\overline{\text{INC}}$  will increment or decrement the wiper (depending on the state of the  $\text{U}/\overline{\text{D}}$  input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever  $\overline{\text{CS}}$  transitions HIGH while the  $\overline{\text{INC}}$  input is also HIGH. When the CAT5116 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With  $\overline{\text{INC}}$  set low, the CAT5116 may be deselected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

## OPERATING MODES

| $\overline{INC}$ | $\overline{CS}$ | $U/\overline{D}$ | Operation                   |
|------------------|-----------------|------------------|-----------------------------|
| High to Low      | Low             | High             | Wiper toward H              |
| High to Low      | Low             | Low              | Wiper toward L              |
| High             | Low to High     | X                | Store Wiper Position        |
| Low              | Low to High     | X                | No Store, Return to Standby |
| X                | High            | X                | Standby                     |

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Parameters                        | Ratings                | Units |
|-----------------------------------|------------------------|-------|
| Supply Voltage<br>$V_{CC}$ to GND | -0.5 to +7V            | V     |
| Inputs                            |                        |       |
| $\overline{CS}$ to GND            | -0.5 to $V_{CC} + 0.5$ | V     |
| $\overline{INC}$ to GND           | -0.5 to $V_{CC} + 0.5$ | V     |
| $U/\overline{D}$ to GND           | -0.5 to $V_{CC} + 0.5$ | V     |
| $R_H$ to GND                      | -0.5 to $V_{CC} + 0.5$ | V     |
| $R_L$ to GND                      | -0.5 to $V_{CC} + 0.5$ | V     |
| $R_W$ to GND                      | -0.5 to $V_{CC} + 0.5$ | V     |

| Parameters   | Ratings    | Units |
|--|------------|-------|
| Operating Ambient Temperature<br>Industrial ('I' suffix) | -40 to +85 | °C    |
| Junction Temperature (10s)                               | +150       | °C    |
| Storage Temperature                                      | +150       | °C    |
| Lead Soldering (10s max)                                 | +300       | °C    |

## RELIABILITY CHARACTERISTICS

| Symbol             | Parameter          | Test Method                   | Min       | Typ | Max | Units  |
|--------------------|--------------------|-------------------------------|-----------|-----|-----|--------|
| $V_{ZAP}^{(2)}$    | ESD Susceptibility | MIL-STD-883, Test Method 3015 | 2000      |     |     | V      |
| $I_{LTH}^{(2)(3)}$ | Latch-Up           | JEDEC Standard 17             | 100       |     |     | mA     |
| $T_{DR}$           | Data Retention     | MIL-STD-883, Test Method 1008 | 100       |     |     | Years  |
| $N_{END}$          | Endurance          | MIL-STD-883, Test Method 1003 | 1,000,000 |     |     | Stores |

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +2.5V$  to  $+5.5V$  unless otherwise specified

## Power Supply

| Symbol          | Parameter                  | Conditions   | Min | Typ  | Max | Units   |
|-----------------|----------------------------|--|-----|------|-----|---------|
| $V_{CC}$        | Operating Voltage Range    |  | 2.5 | –    | 5.5 | V       |
| $I_{CC1}^{(4)}$ | Supply Current (Increment) | $V_{CC} = 5.5V, f = 1MHz, I_W = 0$   | –   | –    | 100 | $\mu A$ |
|                 |                            | $V_{CC} = 5.5V, f = 250kHz, I_W = 0$   | –   | –    | 50  | $\mu A$ |
| $I_{CC2}$       | Supply Current (Write)     | Programming, $V_{CC} = 5.5V$   |     |      | 1   | mA      |
|                 |                            | $V_{CC} = 3V$  |     |      | 500 | $\mu A$ |
| $I_{SB1}$       | Supply Current (Standby)   | $\overline{CS} = V_{CC} - 0.3V$<br>$U/\overline{D}, \overline{INC} = V_{CC} - 0.3V$ or GND | –   | 0.01 | 1   | $\mu A$ |

## Notes:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- (2) This parameter is tested initially and after a design or process change that affects the parameter.
- (3) Latch-up protection is provided for stresses up to 100mA on address and data pins from  $-1V$  to  $V_{CC} + 1V$
- (4)  $I_W$  = source or sink

**Logic Inputs**

| Symbol    | Parameter                     | Conditions                   | Min                 | Typ | Max                 | Units   |
|-----------|-------------------------------|------------------------------|---------------------|-----|---------------------|---------|
| $I_{IH}$  | Input Leakage Current         | $V_{IN} = V_{CC}$            | -                   | -   | 10                  | $\mu A$ |
| $I_{IL}$  | Input Leakage Current         | $V_{IN} = 0V$                | -                   | -   | -10                 | $\mu A$ |
| $V_{IH1}$ | TTL High Level Input Voltage  | $4.5V \leq V_{CC} \leq 5.5V$ | 2                   | -   | $V_{CC}$            | V       |
| $V_{IL1}$ | TTL Low Level Input Voltage   |                              | 0                   | -   | 0.8                 | V       |
| $V_{IH2}$ | CMOS High Level Input Voltage | $2.5V \leq V_{CC} \leq 5.5V$ | $V_{CC} \times 0.7$ | -   | $V_{CC} + 0.3$      | V       |
| $V_{IL2}$ | CMOS Low Level Input Voltage  |                              | -0.3                | -   | $V_{CC} \times 0.2$ | V       |

**Potentiometer Parameters**

| Symbol        | Parameter                  | Conditions                       | Min | Typ    | Max      | Units            |
|---------------|----------------------------|----------------------------------|-----|--------|----------|------------------|
| $R_{POT}$     | Potentiometer Resistance   |                                  |     | 32     |          | k $\Omega$       |
| $R_{TOL}$     | Pot. Resistance Tolerance  |                                  |     |        | $\pm 20$ | %                |
| $V_{RH}$      | Voltage on $R_H$ pin       |                                  | 0   |        | $V_{CC}$ | V                |
| $V_{RL}$      | Voltage on $R_L$ pin       |                                  | 0   |        | $V_{CC}$ | V                |
| $R_V^{(1)}$   | Relative Variation         |                                  |     |        | 0.05     |                  |
| $R_{WI}$      | Wiper Resistance           | $V_{CC} = 5V, I_W = 1mA$         |     | 200    | 400      | $\Omega$         |
|               |                            | $V_{CC} = 2.5V, I_W = 1mA$       |     | 400    | 1000     | $\Omega$         |
| $I_W$         | Wiper Current              |                                  |     |        | 1        | mA               |
| $TC_{RPOT}$   | TC of Pot Resistance       |                                  |     | 300    |          | ppm/ $^{\circ}C$ |
| $TC_{RATIO}$  | Ratiometric TC             |                                  |     |        | 20       | ppm/ $^{\circ}C$ |
| $V_N$         | Noise                      | 100kHz / 1kHz                    |     | 8/24   |          | nV/ $\sqrt{Hz}$  |
| $C_H/C_L/C_W$ | Potentiometer Capacitances |                                  |     | 8/8/25 |          | pF               |
| fc            | Frequency Response         | Passive Attenuator, 10k $\Omega$ |     | 1.7    |          | MHz              |

**Note:**

(1) Relative variation is a measure of the error in step size between taps =  $\log(V_{W(N)}) - \log(V_{W(N-1)}) = 0.045 \pm 0.003$ .

## AC CONDITIONS OF TEST

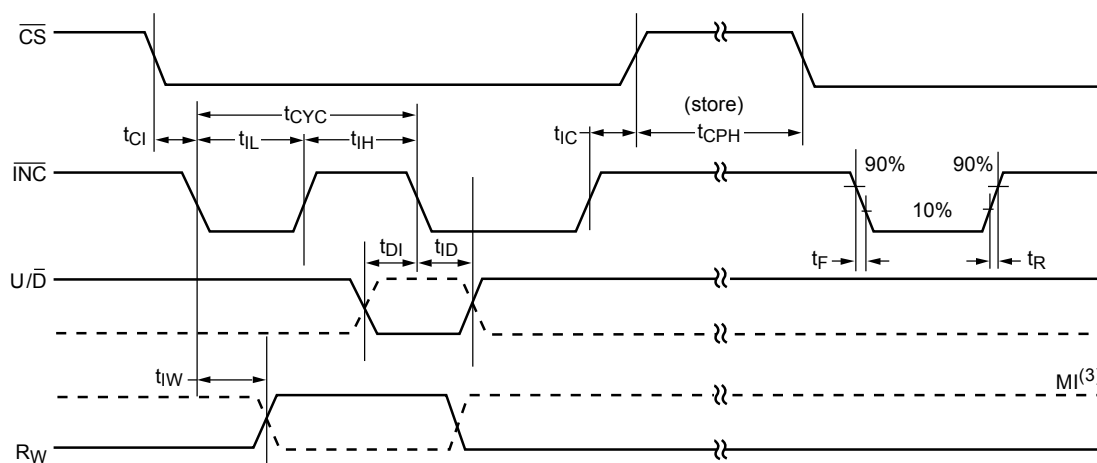
|                           |                              |
|---------------------------|------------------------------|
| $V_{CC}$ Range            | $2.5V \leq V_{CC} \leq 5.5V$ |
| Input Pulse Levels        | $0.2V_{CC}$ to $0.7V_{CC}$   |
| Input Rise and Fall Times | 10ns                         |
| Input Reference Levels    | $0.5V_{CC}$                  |

## AC OPERATING CHARACTERISTICS

$V_{CC} = +2.5V$  to  $+5.5V$ ,  $V_H = V_{CC}$ ,  $V_L = 0V$ , unless otherwise specified

| Symbol           | Parameter   | Min | Typ <sup>(1)</sup> | Max | Units   |
|------------------|---|-----|--------------------|-----|---------|
| $t_{CI}$         | $\overline{CS}$ to $\overline{INC}$ Setup             | 100 | –                  | –   | ns      |
| $t_{DI}$         | $U/\overline{D}$ to $\overline{INC}$ Setup            | 50  | –                  | –   | ns      |
| $t_{ID}$         | $U/\overline{D}$ to $\overline{INC}$ Hold             | 100 | –                  | –   | ns      |
| $t_{iL}$         | $\overline{INC}$ LOW Period                           | 250 | –                  | –   | ns      |
| $t_{iH}$         | $\overline{INC}$ HIGH Period                          | 250 | –                  | –   | ns      |
| $t_{iC}$         | $\overline{INC}$ Inactive to $\overline{CS}$ Inactive | 1   | –                  | –   | $\mu s$ |
| $t_{CPH1}$       | $\overline{CS}$ Deselect Time (NO STORE)              | 100 | –                  | –   | ns      |
| $t_{CPH2}$       | $\overline{CS}$ Deselect Time (STORE)                 | 10  | –                  | –   | ms      |
| $t_{iW}$         | $\overline{INC}$ to $V_{OUT}$ Change                  | –   | 1                  | 5   | $\mu s$ |
| $t_{CYC}$        | $\overline{INC}$ Cycle Time                           | 1   | –                  | –   | $\mu s$ |
| $t_R, t_F^{(2)}$ | $\overline{INC}$ Input Rise and Fall Time             | –   | –                  | 500 | $\mu s$ |
| $t_{PU}^{(2)}$   | Power-up to Wiper Stable                              | –   | –                  | 1   | ms      |
| $t_{WR}$         | Store Cycle   | –   | 5                  | 10  | ms      |

## A.C. TIMING



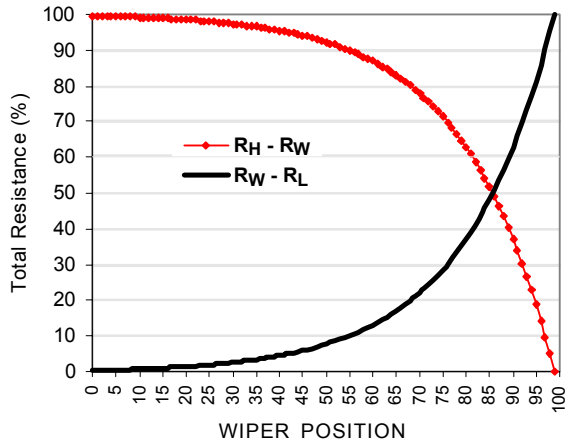
## Notes:

- (1) Typical values are for  $T_A = 25^\circ C$  and nominal supply voltage.
- (2) This parameter is periodically sampled and not 100% tested.
- (3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

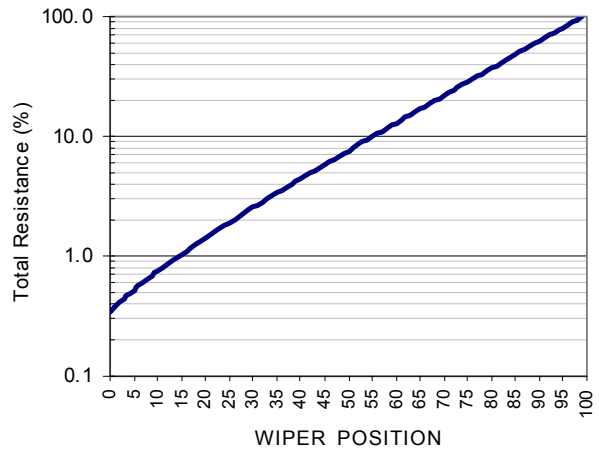
### TYPICAL CHARACTERISTICS

$V_{CC} = 5V$ ,  $T_{AMB} = 25^{\circ}C$ , unless otherwise specified

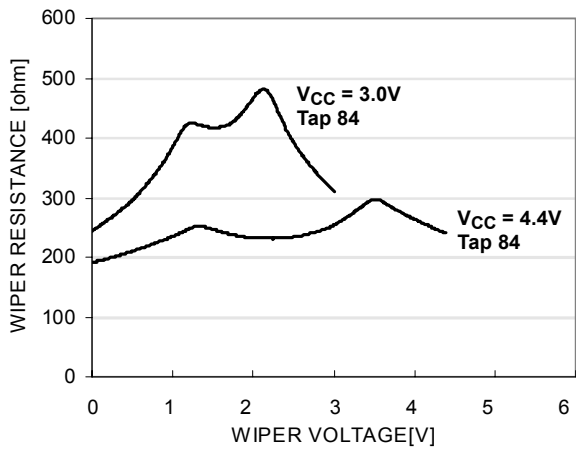
Wiper-Low/High Resistances vs. Wiper Position



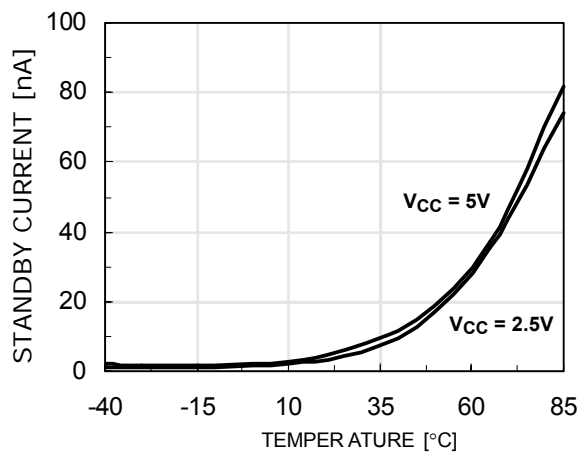
Wiper-Low Resistance vs. Wiper Position (log scale)



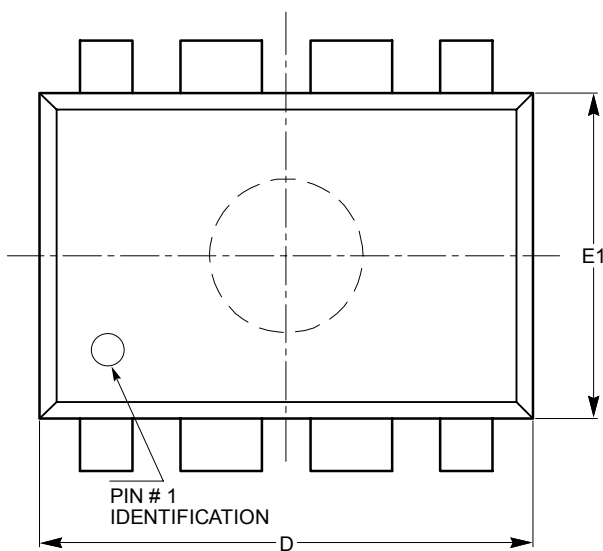
Wiper Resistance vs. Wiper Voltage



Standby Supply Current vs. Temperature

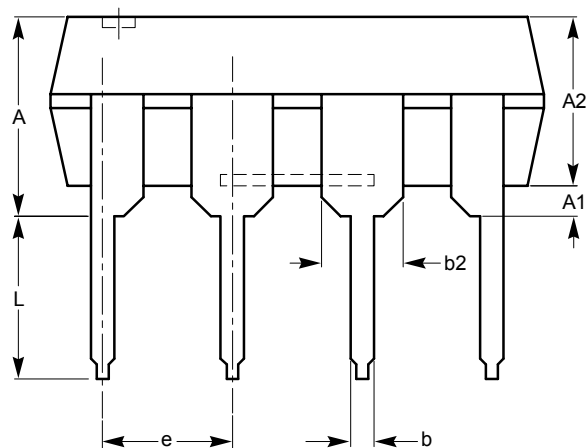


## PACKAGE OUTLINE DRAWINGS

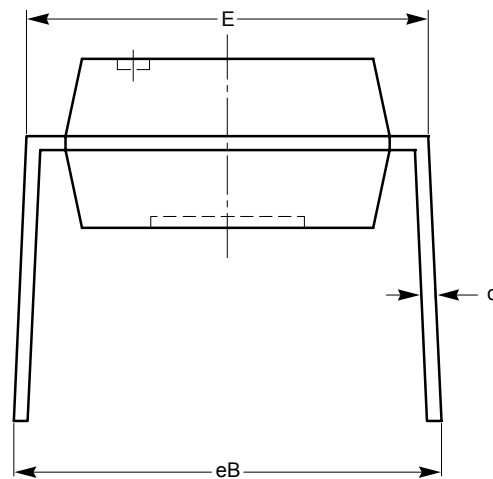
PDIP 8-Lead 300mils (L) <sup>(1)(2)</sup>

TOP VIEW

| SYMBOL | MIN      | NOM  | MAX   |
|--------|----------|------|-------|
| A      |          |      | 5.33  |
| A1     | 0.38     |      |       |
| A2     | 2.92     | 3.30 | 4.95  |
| b      | 0.36     | 0.46 | 0.56  |
| b2     | 1.14     | 1.52 | 1.78  |
| c      | 0.20     | 0.25 | 0.36  |
| D      | 9.02     | 9.27 | 10.16 |
| E      | 7.62     | 7.87 | 8.25  |
| e      | 2.54 BSC |      |       |
| E1     | 6.10     | 6.35 | 7.11  |
| eB     | 7.87     |      | 10.92 |
| L      | 2.92     | 3.30 | 3.80  |



SIDE VIEW



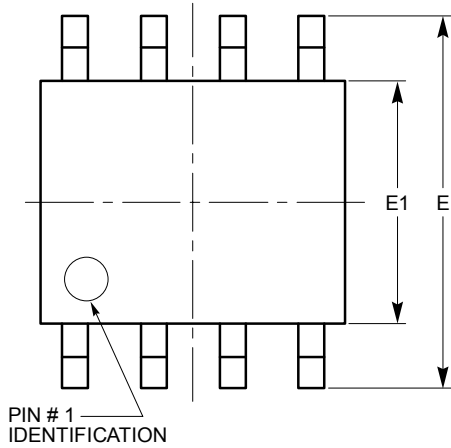
END VIEW

For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeand reel.pdf>.

**Notes:**

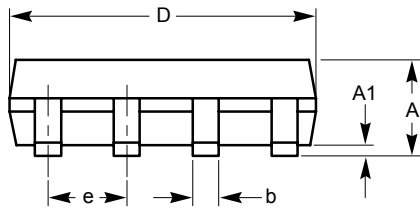
- (1) All dimensions are in millimeters.  
 (2) Complies with JEDEC standard MS-001.

SOIC 8-Lead 150mils (V) <sup>(1)(2)</sup>

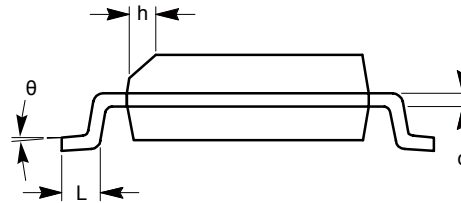


TOP VIEW

| SYMBOL   | MIN      | NOM | MAX  |
|----------|----------|-----|------|
| A        | 1.35     |     | 1.75 |
| A1       | 0.10     |     | 0.25 |
| b        | 0.33     |     | 0.51 |
| c        | 0.19     |     | 0.25 |
| D        | 4.80     |     | 5.00 |
| E        | 5.80     |     | 6.20 |
| E1       | 3.80     |     | 4.00 |
| e        | 1.27 BSC |     |      |
| h        | 0.25     |     | 0.50 |
| L        | 0.40     |     | 1.27 |
| $\theta$ | 0°       |     | 8°   |



SIDE VIEW



END VIEW

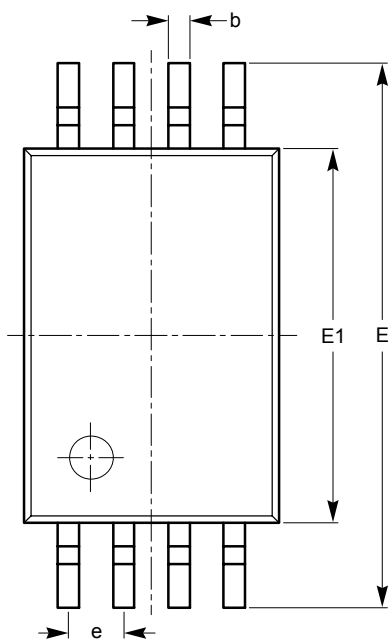
For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeand reel.pdf>.

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MS-012.

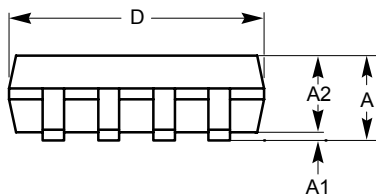


TSSOP 8-Lead 4.4mm (Y) <sup>(1)(2)</sup>

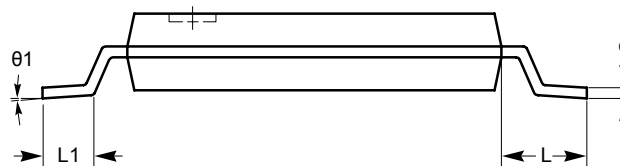


TOP VIEW

| SYMBOL     | MIN      | NOM  | MAX  |
|------------|----------|------|------|
| A          |          |      | 1.20 |
| A1         | 0.05     |      | 0.15 |
| A2         | 0.80     | 0.90 | 1.05 |
| b          | 0.19     |      | 0.30 |
| c          | 0.09     |      | 0.20 |
| D          | 2.90     | 3.00 | 3.10 |
| E          | 6.30     | 6.40 | 6.50 |
| E1         | 4.30     | 4.40 | 4.50 |
| e          | 0.65 BSC |      |      |
| L          | 1.00 REF |      |      |
| L1         | 0.50     | 0.60 | 0.75 |
| $\theta 1$ | 0°       |      | 8°   |



SIDE VIEW



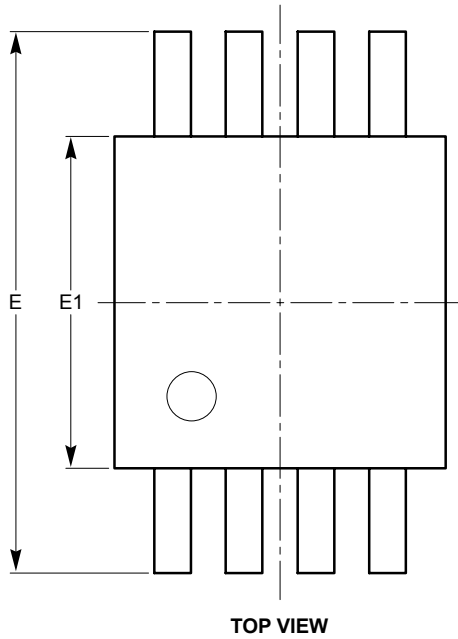
END VIEW

For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreel.pdf>.

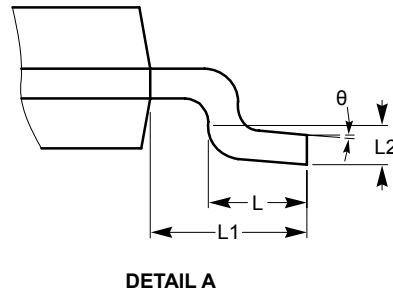
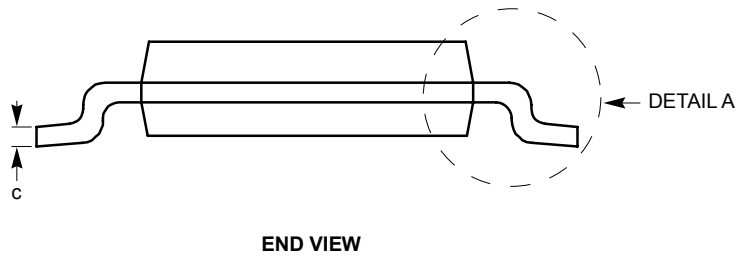
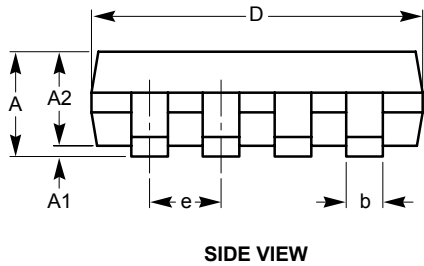
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MO-153.

MSOP 8-Lead 3.0 x 3.0mm (Z) <sup>(1)(2)</sup>



| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      |          |      | 1.10 |
| A1     | 0.05     | 0.10 | 0.15 |
| A2     | 0.75     | 0.85 | 0.95 |
| b      | 0.22     |      | 0.38 |
| c      | 0.13     |      | 0.23 |
| D      | 2.90     | 3.00 | 3.10 |
| E      | 4.80     | 4.90 | 5.00 |
| E1     | 2.90     | 3.00 | 3.10 |
| e      | 0.65 BSC |      |      |
| L      | 0.40     | 0.60 | 0.80 |
| L1     | 0.95 REF |      |      |
| L2     | 0.25 BSC |      |      |
| θ      | 0°       |      | 6°   |

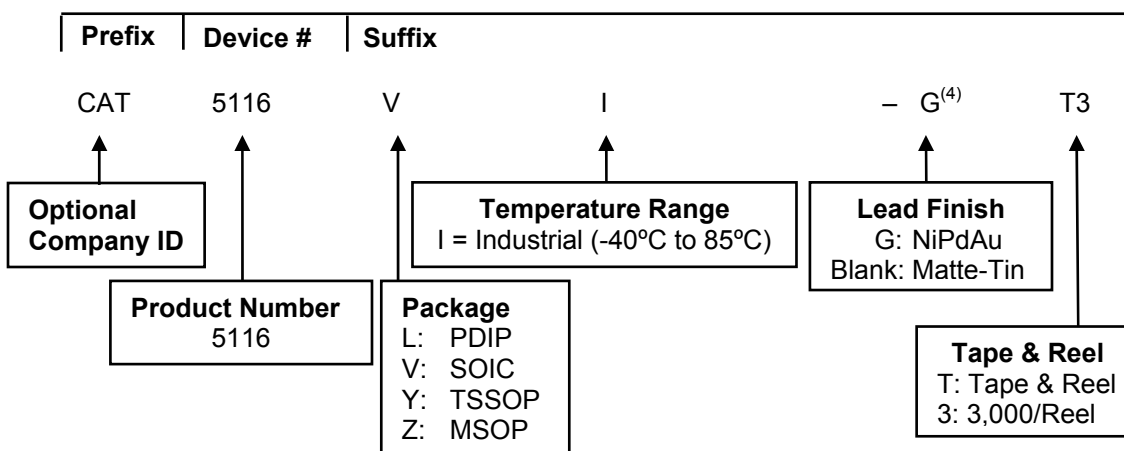


For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreeel.pdf>.

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MO-187.

**EXAMPLE OF ORDERING INFORMATION**



| <b>ORDERING PART NUMBER</b> |
|-----------------------------|
| CAT5116LI-G                 |
| CAT5116VI-G                 |
| CAT5116YI-G                 |
| CAT5116ZI                   |

**Notes:**

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT5116VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
- (4) For Matte-Tin finish, contact factory.

**REVISION HISTORY**

| <b>Date</b> | <b>Rev.</b> | <b>Description</b>   |
|-------------|-------------|--|
| 09-Oct-03   | G           | Revised Features<br>Revised Potentiometer Schematic<br>Revised DC Electrical Characteristics<br>Updated Potentiometer Parameters |
| 10-Mar-04   | H           | Updated Potentiometer Parameters   |
| 29-Mar-04   | I           | Changed Green Package marking for SOIC from W to V   |
| 12-Apr-04   | J           | Eliminated data sheet designation<br>Updated Reel Ordering Information   |
| 01-Jun-07   | K           | Added Package Outline<br>Updated Example of Ordering Information<br>Added MD- in front of Document No.                           |
| 21-Nov-08   | L           | Update Package Outline Drawings<br>Change logo and fine print to ON Semiconductor  |
| 13-Jan-09   | M           | Update Ordering Part Number  |