RD74LVC273B

Octal D-type Flip-Flops with Clear

REJ03D0323–0100Z
Rev.1.00
Jun. 16, 2004

Description

The RD74LVC273B has eight edge trigger D-type flip-flops with clear in a 20-pin package. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state. Low-voltage and high-speed operation is suitable for battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 1.65 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_{OUT} (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High Output current ±4 mA (@V_{CC} = 1.65 V)
  ±8 mA (@V_{CC} = 2.3 V)
  ±12 mA (@V_{CC} = 2.7 V)
  ±24 mA (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

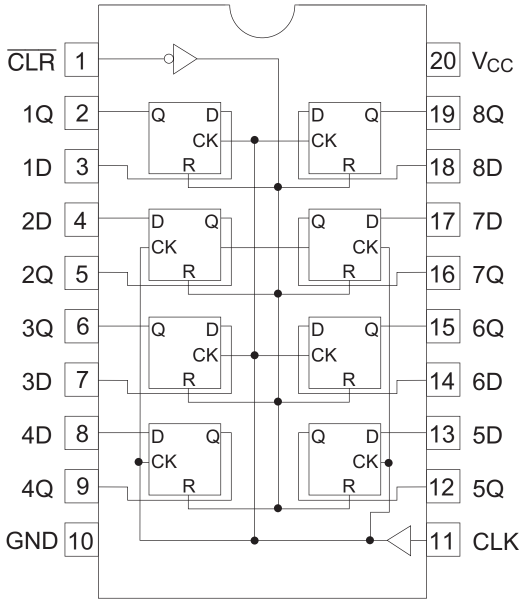
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC273BFPEL	SOP–20 pin(JEITA)	FP–20DAV	FP	EL (2,000 pcs / reel)
RD74LVC273BTELL	TSSOP–20 pin	TTP–20DAV	T	ELL (2,000 pcs / reel)

Function Table

Inputs			Output Q
$\overline{CLR}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	↓	X	Q_0

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition
Q_0: Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 7.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 7.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50		V_O = V_{CC}+0.5 V
Output voltage	V_O	–0.5 to V_{CC}+0.5	V	Output “H” or “L”
		–0.5 to 7.0		V_{CC}: OFF
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to 150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		1.65 to 5.5		At operation
Input/Output voltage	V_I	0 to 5.5	V	CLK, $\overline{CLR}$, D
	V_O	0 to V_{CC}		Output "H" or "L"
		0 to 5.5		V_{CC}: OFF
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–4	mA	V_{CC} = 1.65 V
		–8		V_{CC} = 2.3 V
		–12		V_{CC} = 2.7 V
		–24		V_{CC} = 3.0 V to 5.5 V
	I_{OL}	4	mA	V_{CC} = 1.65 V
		8		V_{CC} = 2.3 V
		12		V_{CC} = 2.7 V
		24		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time*[1]	t_r / t_f	20	ns/V	V_{CC} = 1.65 V to 2.7 V
		10		V_{CC} = 3.0 V to 5.5 V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	1.65 to 1.95	$V_{CC} \times 0.65$	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—		
	V_{IL}	1.65 to 1.95	—	$V_{CC} \times 0.35$		
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	1.65 to 5.5	$V_{CC} - 0.2$	—	V	I_{OH} = –100 µA
		1.65	1.2	—		I_{OH} = –4 mA
		2.3	1.7	—		I_{OH} = –8 mA
		2.7	2.2	—		I_{OH} = –12 mA
		3.0	2.4	—		
		3.0	2.2	—		I_{OH} = –24 mA
		4.5	3.8	—		
	V_{OL}	1.65 to 5.5	—	0.2		I_{OL} = 100 µA
		1.65	—	0.45		I_{OL} = 4 mA
		2.3	—	0.7		I_{OL} = 8 mA
		2.7	—	0.4		I_{OL} = 12 mA
		3.0	—	0.55		I_{OL} = 24 mA
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Output leak current	I_{OFF}	0	—	±5.0	µA	V_{IN}/V_{OUT} = 5.5 V
Quiescent supply current	I_{CC}	2.7 to 3.6	—	±5.0	µA	V_{IN} = 3.6 V to 5.5 V
		2.7 to 5.5	—	5.0		V_{IN} = V_{CC} or GND
	ΔI_{CC}	2.7 to 3.6	—	500		V_{IN} = one input at (V_{CC}–0.6)V, other inputs at V_{CC} or GND

Switching Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	fmax	1.8±0.15	—	—	55.0	MHz		
		2.5±0.2	—	—	95.0			
		2.7	—	—	150.0			
		3.3±0.3	—	—	150.0			
		5.0±0.5	—	—	150.0			
Propagation delay time	t_{PLH} t_{PHL}	1.8±0.15	1.0	—	21.6	ns	CLK	Q
		2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.5			
		3.3±0.3	1.5	—	7.5			
		5.0±0.5	1.0	—	6.0			
	t_{PHL}	1.8±0.15	1.0	—	21.6	ns	$\overline{\text{CLR}}$	Q
		2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.5			
		3.3±0.3	2.0	—	7.5			
		5.0±0.5	1.0	—	6.0			
Setup time	t_{SU}	1.8±0.15	6.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	2.0	—	—			
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t_h	1.8±0.15	4.0	—	—	ns		
		2.5±0.2	2.0	—	—			
		2.7	1.5	—	—			
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t_W	1.8±0.15	9.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
		5.0±0.5	3.3	—	—			
Between output pins skew*[1]	t_{OSLH} t_{OSHL}	1.8±0.15	—	—	—	ns		
		2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C_{IN}	3.3	—	4.0	—	pF		
Output capacitance	C_O	3.3	—	8.0	—	pF		

Note: 1. This parameter is characterized but not tested.

$t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

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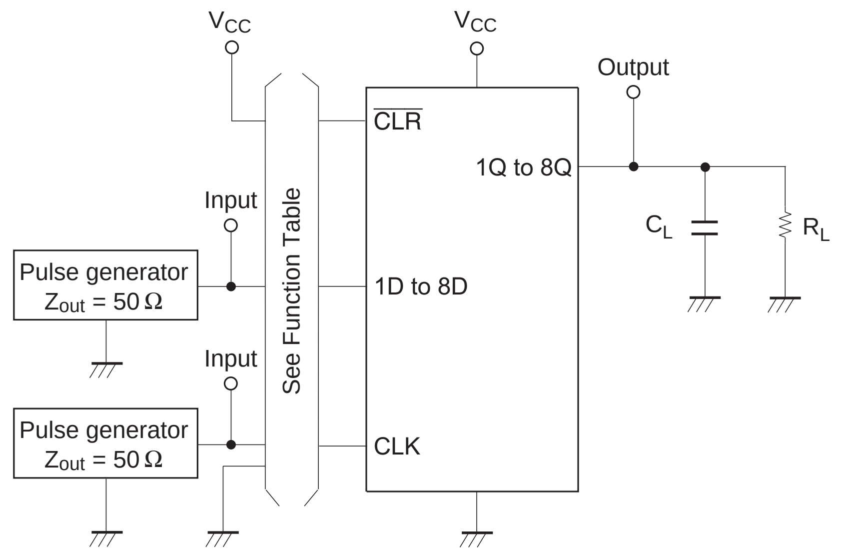
Operating Characteristics

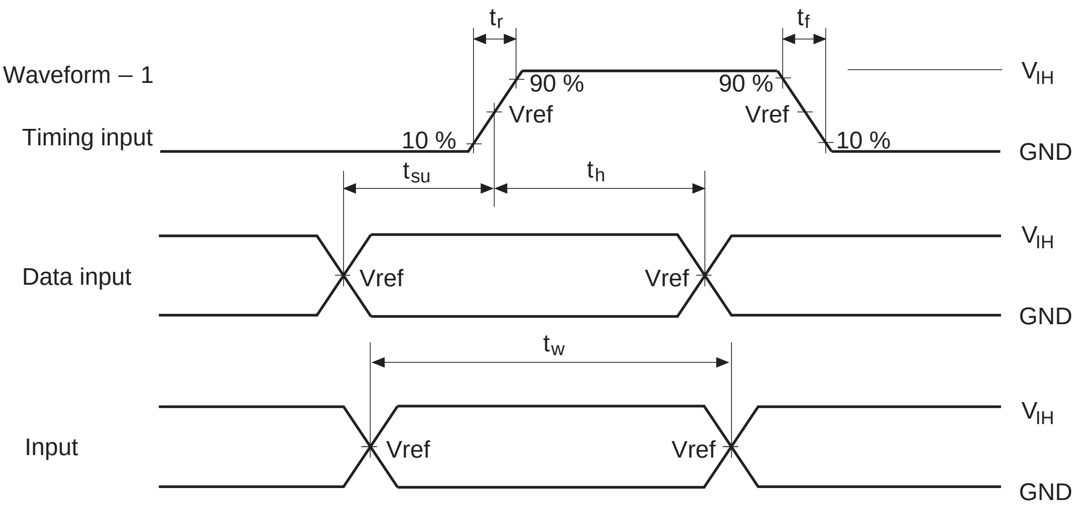
Item	Symbol	V_{CC} = (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	1.8	—	25	—	pF	f = 10 MHz
		2.5	—	26	—		
		3.3	—	28	—		
		5.0	—	32	—		

Test Circuit

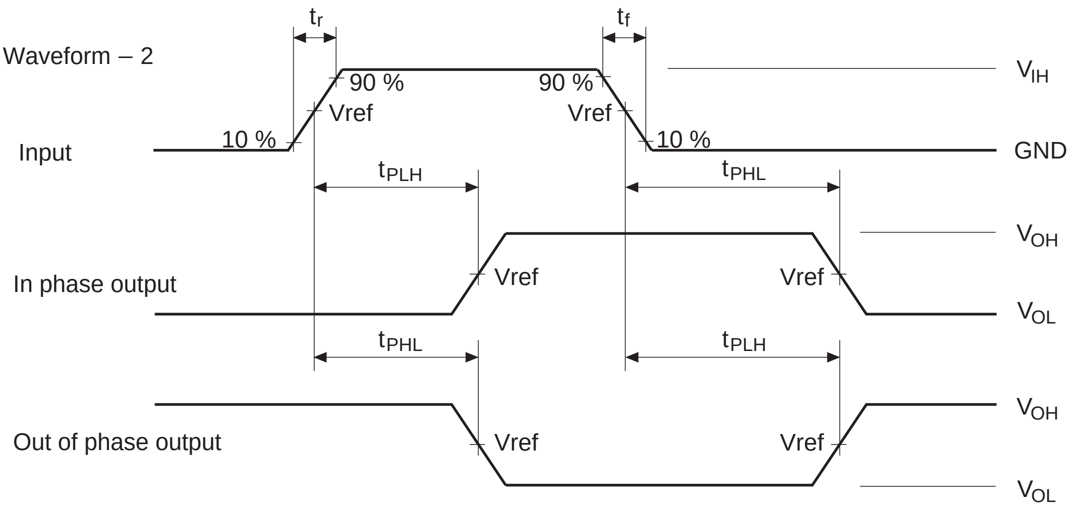


Note: 1. C_L includes probe and jig capacitance.

• Waveform – 1



• Waveform – 2

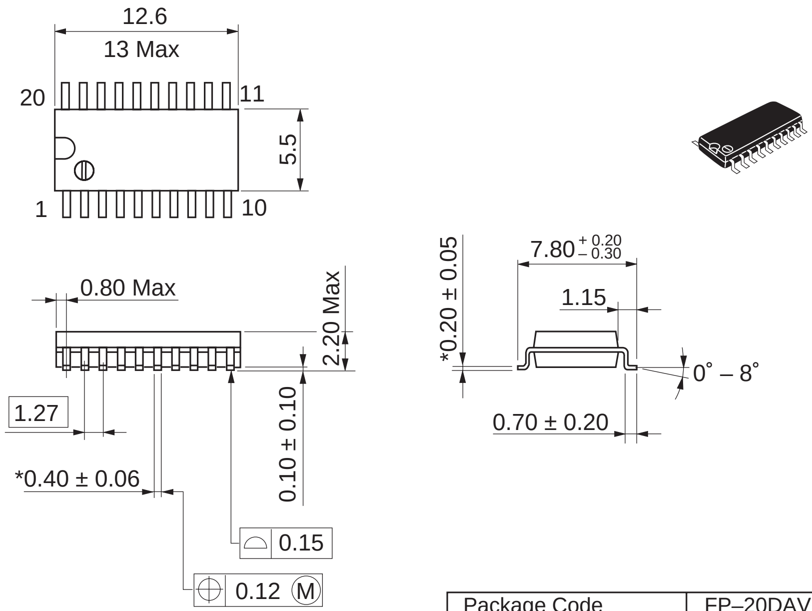


Vcc (V)	INPUTS		Vref	C_L	R_L
	V_{IH}	t_r / t_f			
Vcc = 1.8±0.15 V	Vcc	≤ 2 ns	1/2 Vcc	30 pF	1.0 kΩ
Vcc = 2.5±0.2 V	Vcc	≤ 2 ns	1/2 Vcc	30 pF	500 Ω
Vcc = 2.7 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
Vcc = 3.3±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
Vcc = 5.0±0.5 V	Vcc	≤ 2.5 ns	1/2 Vcc	50 pF	500 Ω

Notes: 1. Input waveform: PRR ≤ 10 MHz, duty cycle 50%.
2. The output is measured one at a time with one transition per measurement.

Package Dimensions

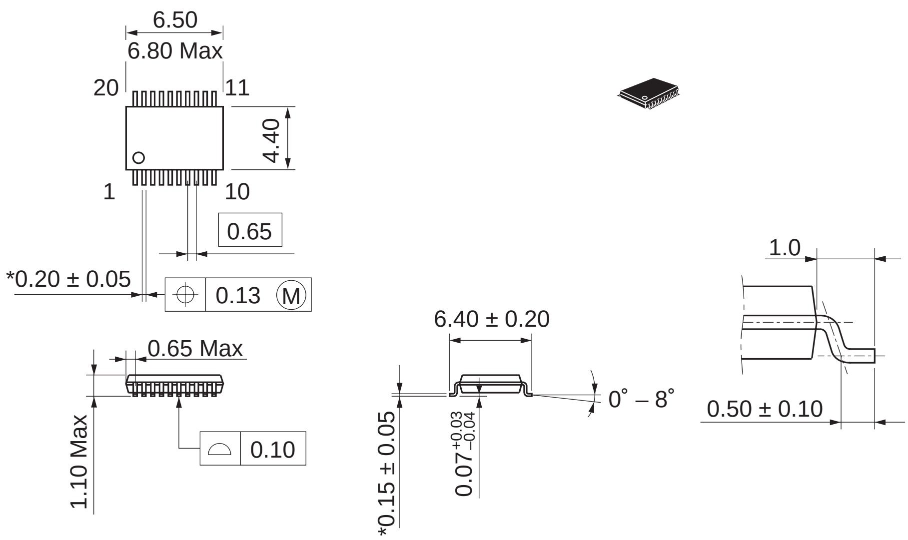
As of January, 2002
Unit: mm



*Pd plating

Package Code	FP–20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2002
Unit: mm



*Pd plating

Package Code	TTP–20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

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