

## 1. Overview

The M32C/88 Group (M32C/88T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/88 Group (M32C/88T) is available in 144-pin and 100-pin plastic molded LQFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

### 1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

## 1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/88 Group (M32C/88T).

**Table 1.1 M32C/88 Group (M32C/88T) Performance (144-Pin Package)**

Characteristic		Performance
CPU	Basic Instructions	108 instructions
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, Vcc=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode
	Address Space	16 Mbytes
	Memory Capacity	See Table 1.3
Peripheral Function	I/O Port	123 I/O pins and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus <sup>(1)</sup> , I <sup>2</sup> C bus <sup>(2)</sup>
	CAN Module	3 channels Supporting CAN 2.0B specification
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions
	CRC Calculation Circuit	CRC-CCITT
	X/Y Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	40 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (* )Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation Stop Detect Function	Main clock oscillation stop detect function
	Cold Start-up/Warm Start-up Determine Function	On-chip (option)
	Electrical Characteristics	Supply Voltage
Power Consumption		28 mA (Vcc=5 V, f(BCLK)=32 MHz) 10µA (Vcc=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)
Operating Ambient Temperature	-40 to 85°C (T version) -40 to 105°C (U version)	
Package	144-pin plastic molded LQFP	

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

**Table 1.2 M32C/88 Group (M32C/88T) Performance (100-Pin Package)**

Characteristic		Performance
CPU	Basic Instructions	108 instructions
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V <sub>CC</sub> =4.2 V to 5.5 V)
	Operating Mode	Single-chip mode
	Address Space	16 Mbytes
	Memory Capacity	See Table 1.3
	I/O Port	87 I/O pins and 1 input pin
Peripheral Function	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus <sup>(1)</sup> , I <sup>2</sup> C bus <sup>(2)</sup>
	CAN Module	3 channels Supporting CAN 2.0B specification
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions
	CRC Calculation Circuit	CRC-CCITT
	X/Y Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	40 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (* )Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation Stop Detect Function	Main clock oscillation stop detect function
	Cold Start-up/Warm Start-up Determine Function	On-chip (option)
	Electrical Characteristics	Supply Voltage
Power Consumption		28 mA (V <sub>CC</sub> =5 V, f(BCLK)=32 MHz) 10μA (V <sub>CC</sub> =5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)
Operating Ambient Temperature		-40 to 85°C (T version) -40 to 105°C (U version)
Package		100-pin plastic molded LQFP

## NOTES:

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2. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

### 1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/88 Group (M32C/88T) microcomputer.

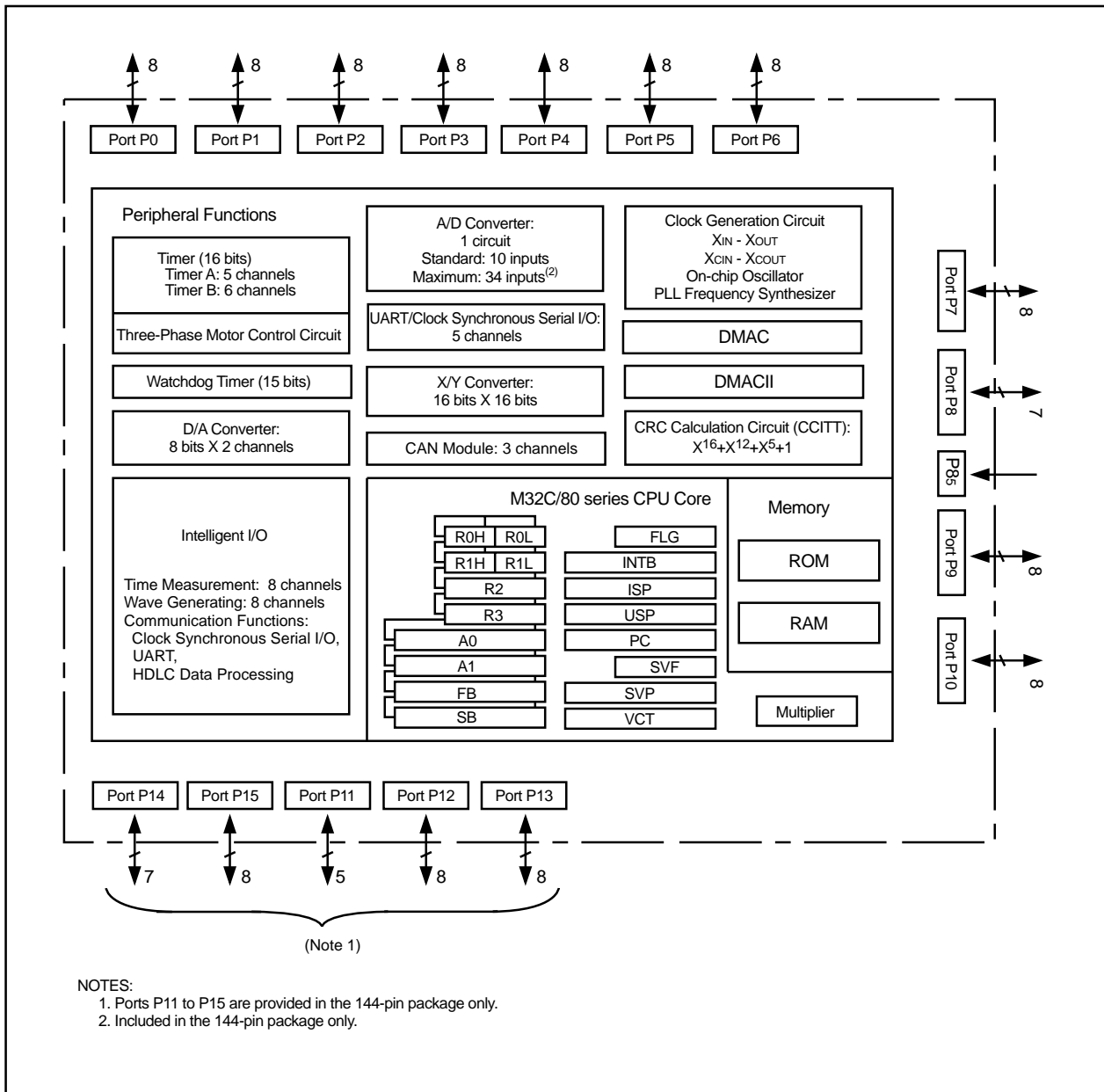


Figure 1.1 M32C/88 Group (M32C/88T) Block Diagram

## 1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

**Table 1.3 M32C/88 Group (1) (T version, M32C/88T) As of October, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30882FJTGP (D)	PLQP0144KA-A (144P6Q-A)	512K+4K	18K	Flash Memory T version (High-reliability 85° C)
M30880FJTGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FHTGP (D)	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30880FHTGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FWTGP (D)	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30880FWTGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under development

**Table 1.3 M32C/88 Group (2) (U version, M32C/88T) As of October, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30882FJUGP (D)	PLQP0144KA-A (144P6Q-A)	512K+4K	18K	Flash Memory U version (High-reliability 105° C)
M30880FJUGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FHUGP (D)	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30880FHUGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FWUGP (D)	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30880FWUGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under development

### NOTE:

Contact our sales office if you are interested in the V version.

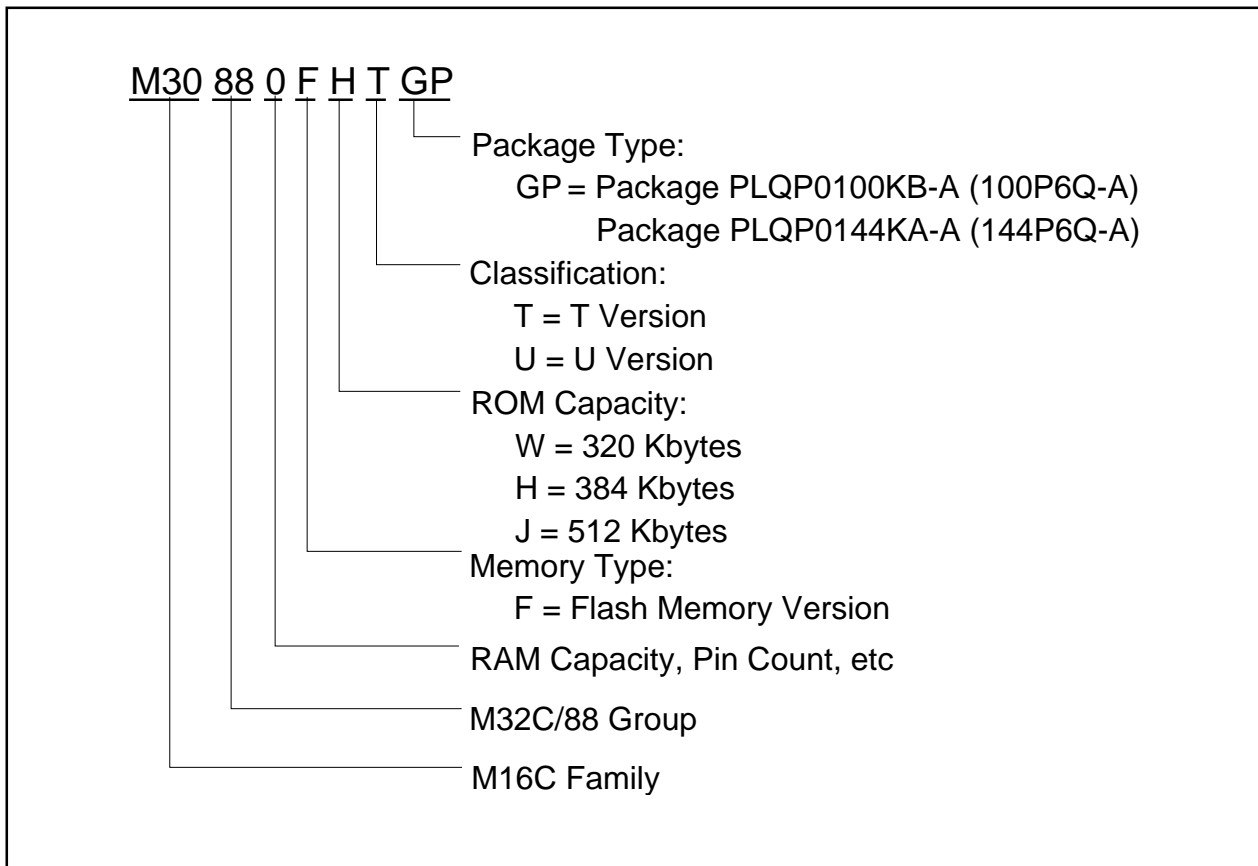


Figure 1.2 Product Numbering System

### 1.5 Pin Assignment

Figures 1.3 and 1.4 show pin assignments (top view).

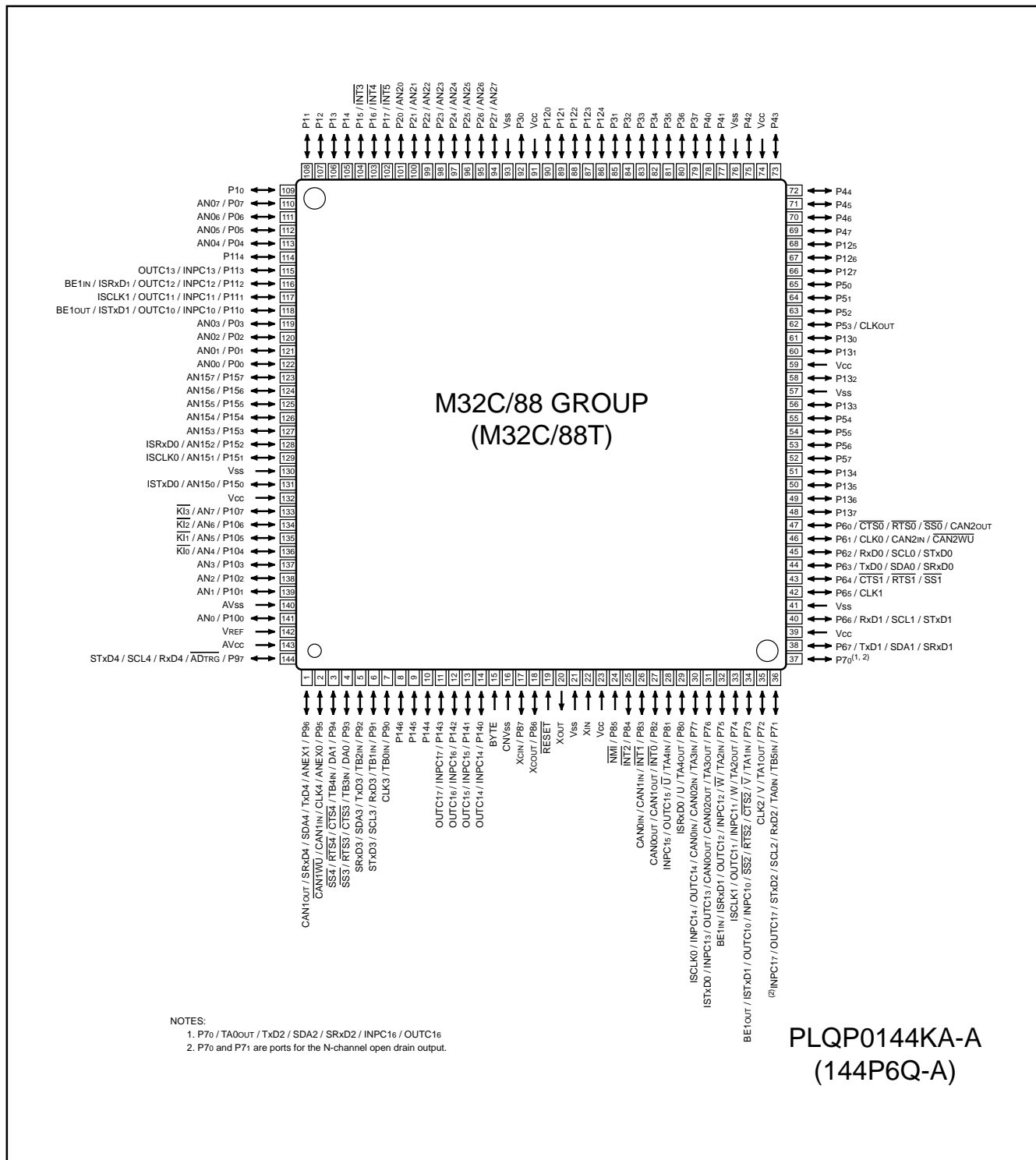


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
1		P96			TxD4/SDA4/SRxD4/CAN1out		ANEX1
2		P95			CLK4/CAN1in/CAN1WU		ANEX0
3		P94		TB4IN	CTS4/RTS4/SS4		DA1
4		P93		TB3IN	CTS3/RTS3/SS3		DA0
5		P92		TB2IN	TxD3/SDA3/SRxD3		
6		P91		TB1IN	RxD3/SCL3/STxD3		
7		P90		TB0IN	CLK3		
8		P146					
9		P145					
10		P144					
11		P143				INPC17/OUTC17	
12		P142				INPC16/OUTC16	
13		P141				INPC15/OUTC15	
14		P140				INPC14/OUTC14	
15	BYTE						
16	CNVss						
17	XcIN	P87					
18	XcOUT	P86					
19	RESET						
20	XOUT						
21	Vss						
22	Xin						
23	Vcc						
24		P85	NMI				
25		P84	INT2				
26		P83	INT1		CAN0in/CAN1in		
27		P82	INT0		CAN0out/CAN1out		
28		P81		TA4in/U		INPC15/OUTC15	
29		P80		TA4out/U		ISRxD0	
30		P77		TA3in	CAN0in/CAN02in	INPC14/OUTC14/ISCLK0	
31		P76		TA3out	CAN0out/CAN02out	INPC13/OUTC13/ISTxD0	
32		P75		TA2in/W		INPC12/OUTC12/ISRxD1/BE1in	
33		P74		TA2out/W		INPC11/OUTC11/ISCLK1	
34		P73		TA1in/V	CTS2/RTS2/SS2	INPC10/OUTC10/ISTxD1/BE1out	
35		P72		TA1out/V	CLK2		
36		P71		TB5in/TA0in	RxD2/SCL2/STxD2	INPC17/OUTC17	
37		P70		TA0out	TxD2/SDA2/SRxD2	INPC16/OUTC16	
38	Vcc	P67			TxD1/SDA1/SRxD1		
39	Vss						
40		P66			RxD1/SCL1/STxD1		
41							
42		P65			CLK1		
43		P64			CTS1/RTS1/SS1		
44		P63			TxD0/SDA0/SRxD0		
45		P62			RxD0/SCL0/STxD0		
46		P61			CLK0/CAN2in/CAN2WU		
47		P60			CTS0/RTS0/SS0/CAN2out		
48		P137					



**Table 1.4 Pin Characteristics for 144-Pin Package (Continued)**

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
49		P136					
50		P135					
51		P134					
52		P57					
53		P56					
54		P55					
55		P54					
56		P133					
57	Vss						
58		P132					
59	Vcc						
60		P131					
61		P130					
62		P53					
63		P52					
64		P51					
65		P50					
66		P127					
67		P126					
68		P125					
69		P47					
70		P46					
71		P45					
72		P44					
73	Vcc	P43					
74							
75	Vss	P42					
76							
77		P41					
78		P40					
79		P37					
80		P36					
81		P35					
82		P34					
83		P33					
84		P32					
85		P31					
86		P124					
87		P123					
88		P122					
89		P121					
90	Vcc	P120					
91	Vss						
92		P30					
93							
94		P27					AN27
95		P26					AN26
96		P25					AN25

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
97		P24					AN24
98		P23					AN23
99		P22					AN22
100		P21					AN21
101		P20					AN20
102		P17	$\overline{\text{INT5}}$				
103		P16	$\overline{\text{INT4}}$				
104		P15	$\overline{\text{INT3}}$				
105		P14					
106		P13					
107		P12					
108		P11					
109		P10					
110		P07					AN07
111		P06					AN06
112		P05					AN05
113		P04					AN04
114		P114					
115		P113				INPC13/OUTC13	
116		P112				INPC12/OUTC12/ISRxD1/BE1IN	
117		P111				INPC11/OUTC11/ISCLK1	
118		P110				INPC10/OUTC10/ISTxD1/BE1OUT	
119		P03					AN03
120		P02					AN02
121		P01					AN01
122		P00					AN00
123		P157					AN157
124		P156					AN156
125		P155					AN155
126		P154					AN154
127		P153					AN153
128		P152				ISRxD0	AN152
129		P151				ISCLK0	AN151
130	Vss						
131		P150				ISTxD0	AN150
132	Vcc						
133		P107	$\overline{\text{KI3}}$				AN7
134		P106	$\overline{\text{KI2}}$				AN6
135		P105	$\overline{\text{KI1}}$				AN5
136		P104	$\overline{\text{KI0}}$				AN4
137		P103					AN3
138		P102					AN2
139		P101					AN1
140	AVss						
141		P100					AN0
142	VREF						
143	AVcc						
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$

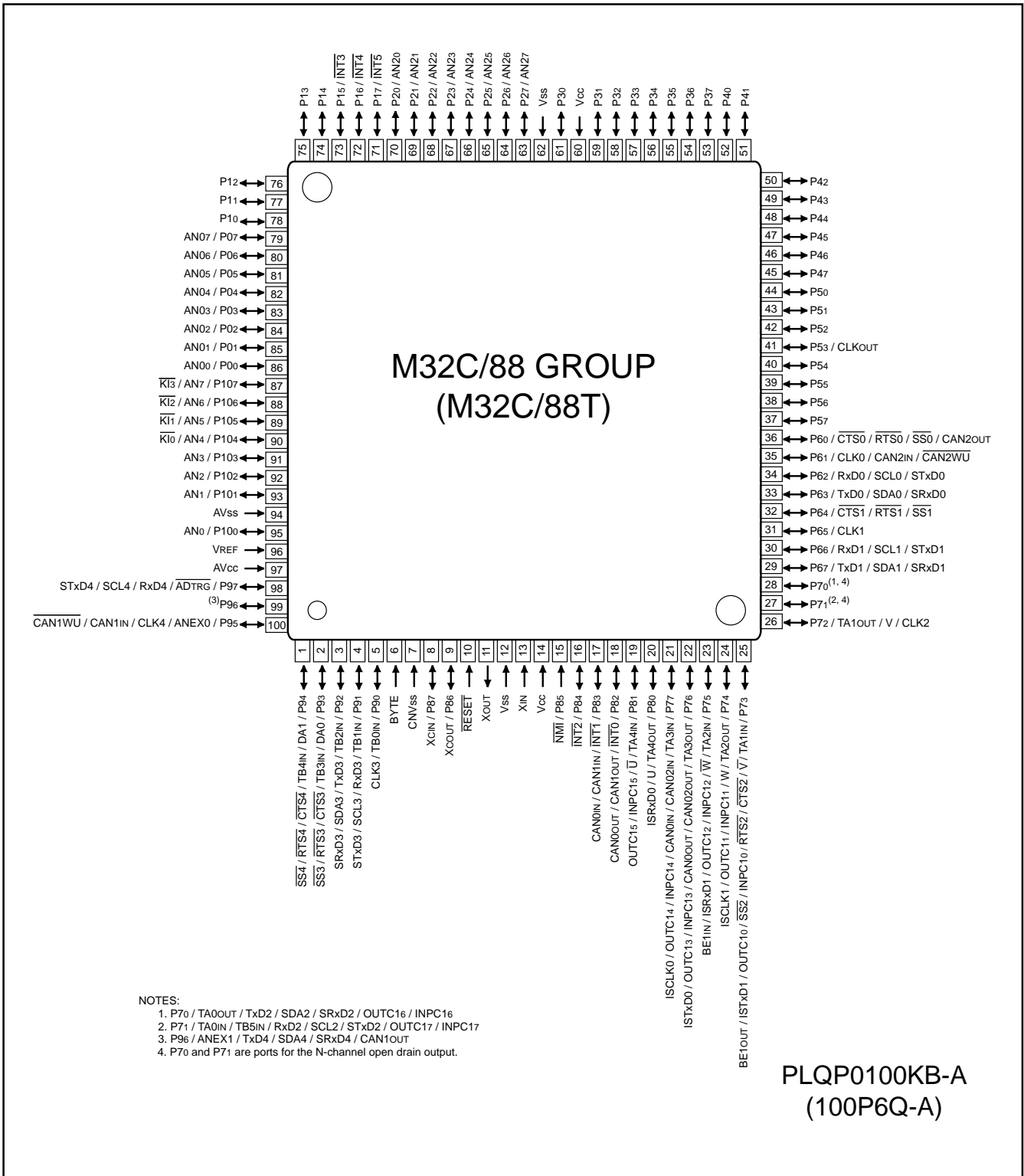


Figure 1.4 Pin Assignment for 100-Pin Package

**Table 1.5 Pin Characteristics for 100-Pin Package**

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
1		P94		TB4IN	$\overline{\text{CTS4}}/\overline{\text{RTS4}}/\overline{\text{SS4}}$		DA1
2		P93		TB3IN	$\overline{\text{CTS3}}/\overline{\text{RTS3}}/\overline{\text{SS3}}$		DA0
3		P92		TB2IN	TxD3/SDA3/SRx3D3		
4		P91		TB1IN	RxD3/SCL3/STxD3		
5		P90		TB0IN	CLK3		
6	BYTE						
7	CNVss						
8	XCIN	P87					
9	XCOUT	P86					
10	$\overline{\text{RESET}}$						
11	XOUT						
12	Vss						
13	XIN						
14	Vcc						
15		P85	$\overline{\text{NMI}}$				
16		P84	$\overline{\text{INT2}}$				
17		P83	$\overline{\text{INT1}}$		CAN0IN/CAN1IN		
18		P82	$\overline{\text{INT0}}$		CAN0OUT/CAN1OUT		
19		P81		TA4IN $\overline{\text{U}}$		INPC15/OUTC15	
20		P80		TA4OUT/U		ISRxD0	
21		P77		TA3IN	CAN0IN/CAN02IN	INPC14/OUTC14/ISCLK0	
22		P76		TA3OUT	CAN0OUT/CAN02OUT	INPC13/OUTC13/ISTxD0	
23		P75		TA2IN $\overline{\text{W}}$		INPC12/OUTC12/ISRxD1/BE1IN	
24		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1	
25		P73		TA1IN $\overline{\text{V}}$	$\overline{\text{CTS2}}/\overline{\text{RTS2}}/\overline{\text{SS2}}$	INPC10/OUTC10/ISTxD1/BE1OUT	
26		P72		TA1OUT/V	CLK2		
27		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	INPC17/OUTC17	
28		P70		TA0OUT	TxD2/SDA2/SRx2D2	INPC16/OUTC16	
29		P67			TxD1/SDA1/SRx1D1		
30		P66			RxD1/SCL1/STxD1		
31		P65			CLK1		
32		P64			$\overline{\text{CTS1}}/\overline{\text{RTS1}}/\overline{\text{SS1}}$		
33		P63			TxD0/SDA0/SRx0D0		
34		P62			RxD0/SCL0/STxD0		
35		P61			CLK0/CAN2IN/CAN2WU		
36		P60			$\overline{\text{CTS0}}/\overline{\text{RTS0}}/\overline{\text{SS0}}/\text{CAN2OUT}$		
37		P57					
38		P56					
39		P55					
40		P54					
41		P53					
42		P52					
43		P51					
44		P50					
45		P47					
46		P46					
47		P45					
48		P44					
49		P43					
50		P42					

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
51		P41					
52		P40					
53		P37					
54		P36					
55		P35					
56		P34					
57		P33					
58		P32					
59		P31					
60	Vcc						
61		P30					
62	Vss						
63		P27					AN27
64		P26					AN26
65		P25					AN25
66		P24					AN24
67		P23					AN23
68		P22					AN22
69		P21					AN21
70		P20					AN20
71		P17	$\overline{\text{INT5}}$				
72		P16	$\overline{\text{INT4}}$				
73		P15	$\overline{\text{INT3}}$				
74		P14					
75		P13					
76		P12					
77		P11					
78		P10					
79		P07					AN07
80		P06					AN06
81		P05					AN05
82		P04					AN04
83		P03					AN03
84		P02					AN02
85		P01					AN01
86		P00					AN00
87		P107	$\overline{\text{KI3}}$				AN7
88		P106	$\overline{\text{KI2}}$				AN6
89		P105	$\overline{\text{KI1}}$				AN5
90		P104	$\overline{\text{KI0}}$				AN4
91		P103					AN3
92		P102					AN2
93		P101					AN1
94	AVss						
95		P100					AN0
96	VREF						
97	AVcc						
98		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$
99		P96			TxD4/SDA4/SRxD4/CAN1out		ANEX1
100		P95			CLK4/CAN1IN/CAN1WU		ANEX0

## 1.6 Pin Description

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages)**

Classification	Symbol	I/O Type	Function
Power Supply	Vcc Vss	I	Apply 4.2 to 5.5 V to both Vcc pins. Apply 0 V to the Vss pin
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to Vcc and the AVSS pin to Vss
Reset Input	RESET	I	The microcomputer is in a reset state when "L" is applied to the RESET pin
CNVss	CNVss	I	Switches processor mode. Connect the CNVss pin to Vss
Input to Switch External Data Bus Width	BYTE	I	Connect the BYTE pin to Vss
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and Xcout. To apply external clock, apply it to XCIN and leave Xcout open
Sub Clock output	Xcout	O	
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as fc, f8 or f32
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	Input pins for Timer A0 to A4
Timer B	TB0IN to TB5IN	I	Input pins for Timer B0 to B5
Three-phase Motor Control Timer Output	U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$	O	Output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS4	I	Input pins for data transmission control
	RTS0 to RTS4	O	Output pins for data reception control
	CLK0 to CLK4	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	Inputs serial data
	TxD0 to TxD4	O	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I <sup>2</sup> C Mode	SDA0 to SDA4	I/O	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4		Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	Inputs serial data when slave mode is selected
	SS0 to SS4	I	Input pins to control serial I/O special function

I : Input    O : Output    I/O : Input and output

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

Classification	Symbol	I/O Type	Function	
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter and D/A converter	
A/D Converter	AN0 to AN7 AN00 to AN07 AN20 to AN27	I	Analog input pins for the A/D converter	
	ADTRG	I	Input pin for an external A/D trigger	
	ANEX0	I/O	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode	
	ANEX1	I	Extended analog input pin for the A/D converter	
D/A Converter	DA0, DA1	O	Output pin for the D/A converter	
Intelligent I/O	INPC10 to INPC17	I	Input pins for the time measurement function	
	OUTC10 to OUTC17	O	Output pins for the waveform generating function (OUTC16 and OUTC17 assigned to P70 and P71 are pins for the N-channel open drain output.)	
	ISCLK0 ISCLK1	I/O	Inputs and outputs the clock for the intelligent I/O communication function	
	ISRXD0 ISRXD1	I	Inputs data for the intelligent I/O communication function	
	ISTXD0 ISTXD1	O	Outputs data for the intelligent I/O communication function	
	BE1IN	I	Inputs data for the intelligent I/O communication function	
	BE1OUT	O	Outputs data for the intelligent I/O communication function	
	CAN	CAN0IN CAN02IN CAN1IN CAN2IN	I	Input pin for the CAN communication function
		CAN0OUT CAN02OUT CAN1OUT CAN2OUT	O	Output pin for the CAN communication function
CAN1WU CAN2WU		I	Input pin for the CANi wake-up interrupt (i=1, 2)	
I/O Ports		P00 to P07 P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57	I/O	8-bit I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
		P60 to P67 P70 to P77 P90 to P97 P100 to P107	I/O	I/O ports having equivalent functions to P0 (P70 and P71 are ports for the N-channel open drain output.)
		P80 to P84 P86, P87	I/O	I/O ports having equivalent functions to P0
Input Port		P85	I	Shares a pin with NMI. NMI input state can be got by reading P85

I : Input    O : Output    I/O : Input and output

**Table 1.6 Pin Description (144-Pin Package Only) (Continued)**

Classification	Symbol	I/O Type	Function
A/D Converter	AN150 to AN157	I	Analog input pins for the A/D converter
I/O Ports	P110 to P114 P120 to P127 P130 to P137 P140 to P146 P150 to P157	I/O	I/O ports having equivalent functions to P0

I : Input    O : Output    I/O : Input and output



## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

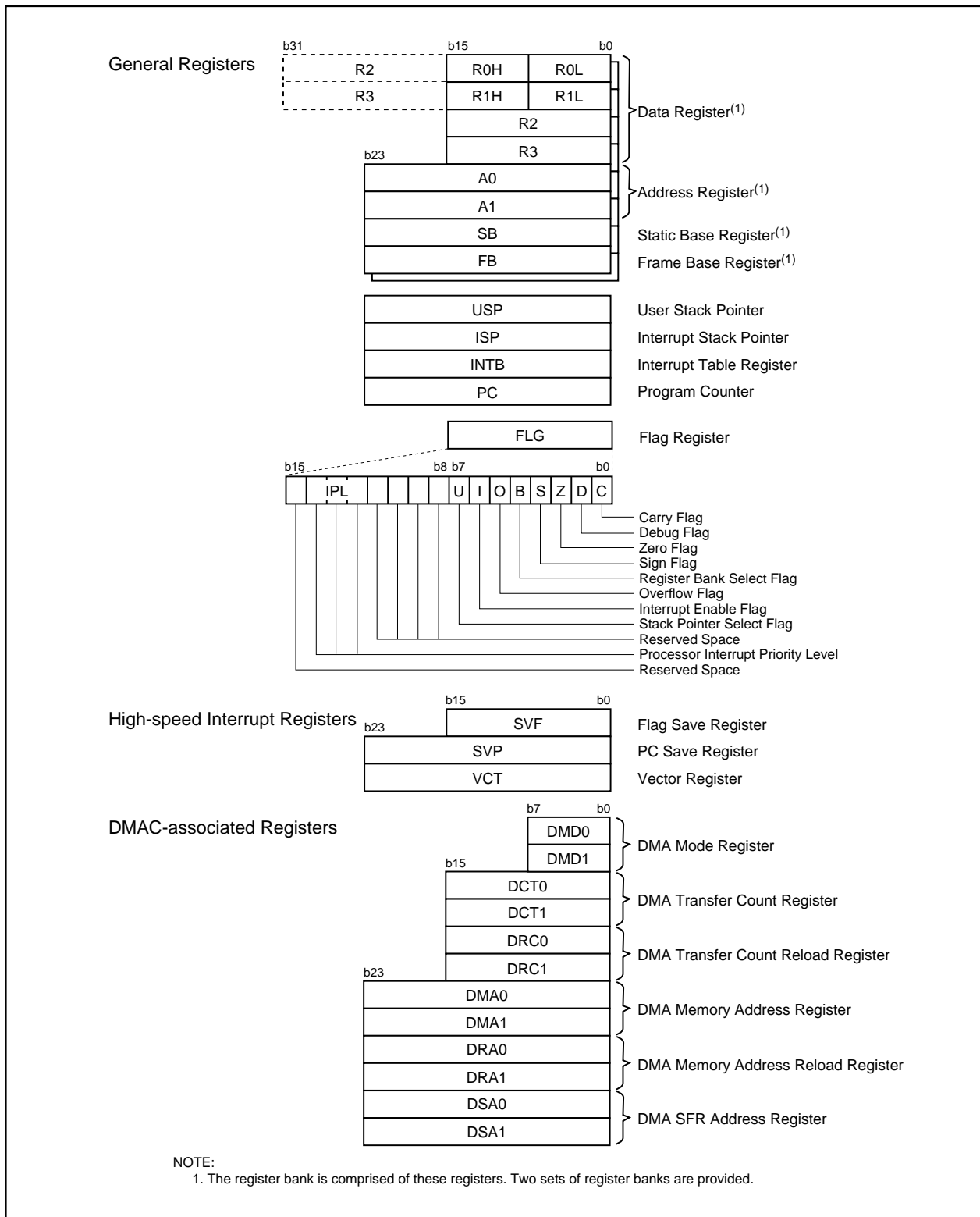


Figure 2.1 CPU Register

## 2.1 General Registers

### 2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

### 2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

### 2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

### 2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

### 2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

### 2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

### 2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

### 2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

#### 2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

#### 2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

#### 2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

#### 2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

### 2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

### 2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

### 2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

### 2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

### 2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

## 2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

## 2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

### 3. Memory

Figure 3.1 shows a memory map of the M32C/88 Group (M32C/88T).

The M32C/88 Group (M32C/88T) provides 16-Mbyte address space addressed from 000000<sub>16</sub> to FFFFFFF<sub>16</sub>.

The internal ROM is allocated from address FFFFFFF<sub>16</sub> to lower. For example, a 64-Kbyte internal ROM is addressed from FF0000<sub>16</sub> to FFFFFFF<sub>16</sub>.

The fixed interrupt vectors are allocated from address FFFFDC<sub>16</sub> to FFFFFFF<sub>16</sub>. It stores the starting address of each interrupt routine.

The internal RAM is allocated from address 000400<sub>16</sub> to higher. For example, a 10-Kbyte internal RAM is allocated from address 000400<sub>16</sub> to 002BFF<sub>16</sub>. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFRs, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers, is allocated from address 000000<sub>16</sub> to 0003FF<sub>16</sub>. All blank spaces within SFRs are reserved and cannot be accessed by users.

The special page vectors are addressed from FFFE00<sub>16</sub> to FFFFDB<sub>16</sub>. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

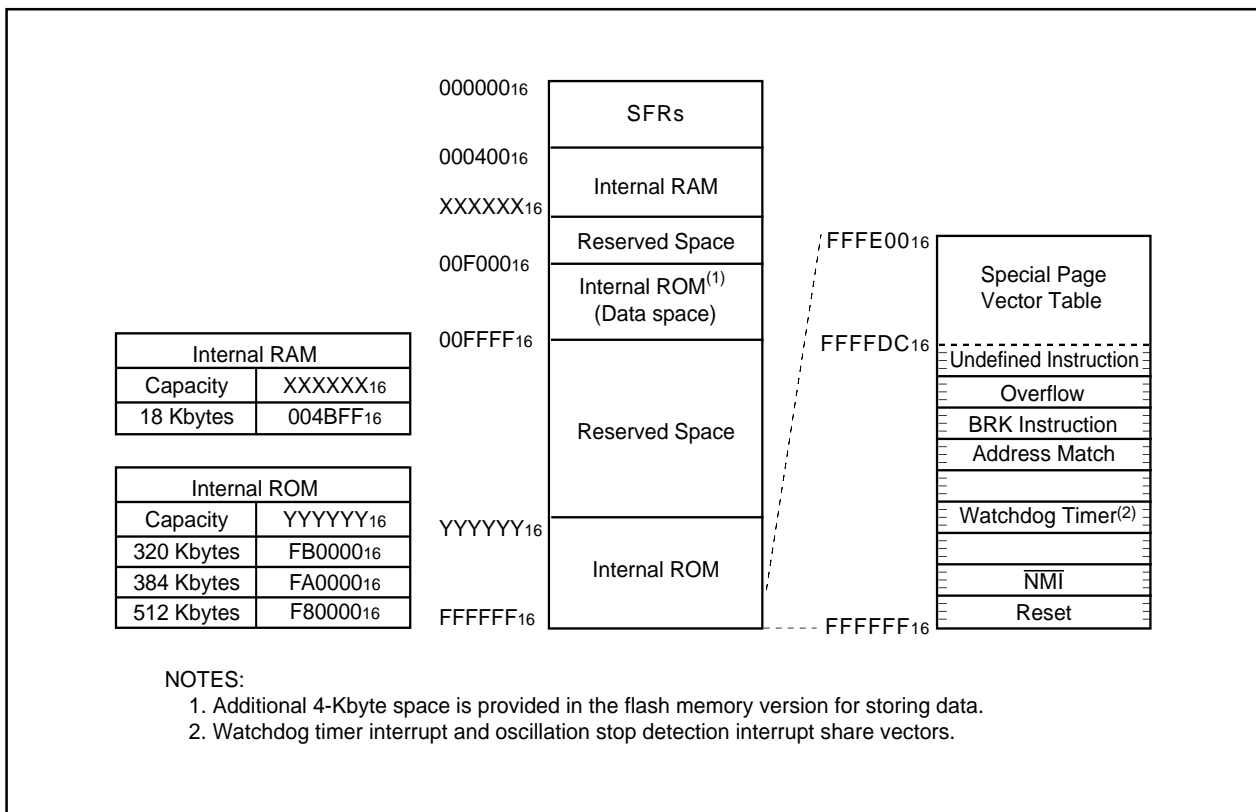


Figure 3.1 Memory Map

## 4. Special Function Registers (SFRs)

Address	Register	Symbol	Value after RESET
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor Mode Register <sup>(1)</sup>	PM0	1000 0000 <sub>2</sub> (CNVss pin ="L")
0005 <sub>16</sub>	Processor Mode Register 1	PM1	00 <sub>16</sub>
0006 <sub>16</sub>	System Clock Control Register 0	CM0	0000 1000 <sub>2</sub>
0007 <sub>16</sub>	System Clock Control Register 1	CM1	0010 0000 <sub>2</sub>
0008 <sub>16</sub>			
0009 <sub>16</sub>	Address Match Interrupt Enable Register	AIER	00 <sub>16</sub>
000A <sub>16</sub>	Protect Register	PRCR	XXXX 0000 <sub>2</sub>
000B <sub>16</sub>			
000C <sub>16</sub>	Main Clock Division Register	MCD	XXX0 1000 <sub>2</sub>
000D <sub>16</sub>	Oscillation Stop Detection Register	CM2	00 <sub>16</sub>
000E <sub>16</sub>	Watchdog Timer Start Register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog Timer Control Register	WDC	000X XXXX <sub>2</sub>
0010 <sub>16</sub>	Address Match Interrupt Register 0	RMAD0	000000 <sub>16</sub>
0011 <sub>16</sub>			
0012 <sub>16</sub>			
0013 <sub>16</sub>	Processor Mode Register 2	PM2	00 <sub>16</sub>
0014 <sub>16</sub>	Address Match Interrupt Register 1	RMAD1	000000 <sub>16</sub>
0015 <sub>16</sub>			
0016 <sub>16</sub>			
0017 <sub>16</sub>			
0018 <sub>16</sub>	Address Match Interrupt Register 2	RMAD2	000000 <sub>16</sub>
0019 <sub>16</sub>			
001A <sub>16</sub>			
001B <sub>16</sub>			
001C <sub>16</sub>	Address Match Interrupt Register 3	RMAD3	000000 <sub>16</sub>
001D <sub>16</sub>			
001E <sub>16</sub>			
001F <sub>16</sub>			
0020 <sub>16</sub>			
0021 <sub>16</sub>			
0022 <sub>16</sub>			
0023 <sub>16</sub>			
0024 <sub>16</sub>			
0025 <sub>16</sub>			
0026 <sub>16</sub>	PLL Control Register 0	PLC0	0001 X010 <sub>2</sub>
0027 <sub>16</sub>	PLL Control Register 1	PLC1	000X 0000 <sub>2</sub>
0028 <sub>16</sub>	Address Match Interrupt Register 4	RMAD4	000000 <sub>16</sub>
0029 <sub>16</sub>			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>	Address Match Interrupt Register 5	RMAD5	000000 <sub>16</sub>
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0060 <sub>16</sub>			
0030 <sub>16</sub>			
0031 <sub>16</sub>			
0032 <sub>16</sub>			
0033 <sub>16</sub>			
0034 <sub>16</sub>			
0035 <sub>16</sub>			
0036 <sub>16</sub>			
0037 <sub>16</sub>			
0038 <sub>16</sub> 0039 <sub>16</sub> 003A <sub>16</sub>	Address Match Interrupt Register 6	RMAD6	000000 <sub>16</sub>
003B <sub>16</sub>			
003C <sub>16</sub> 003D <sub>16</sub> 003E <sub>16</sub>	Address Match Interrupt Register 7	RMAD7	000000 <sub>16</sub>
003F <sub>16</sub>			
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>			
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>			
0049 <sub>16</sub>			
004A <sub>16</sub>			
004B <sub>16</sub>			
004C <sub>16</sub>			
004D <sub>16</sub>			
004E <sub>16</sub>			
004F <sub>16</sub>			
0050 <sub>16</sub>			
0051 <sub>16</sub>			
0052 <sub>16</sub>			
0053 <sub>16</sub>			
0054 <sub>16</sub>			
0055 <sub>16</sub> 0056 <sub>16</sub>	Flash Memory Control Register 1	FMR1	0000 0101 <sub>2</sub>
0057 <sub>16</sub> 0058 <sub>16</sub>	Flash Memory Control Register 0	FMR0	0000 0001 <sub>2</sub>
0059 <sub>16</sub>			
005A <sub>16</sub>			
005B <sub>16</sub>			
005C <sub>16</sub>			
005D <sub>16</sub>			
005E <sub>16</sub>			
005F <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>	DMA0 Interrupt Control Register	DM0IC	XXXX X000 <sub>2</sub>
0069 <sub>16</sub>	Timer B5 Interrupt Control Register	TB5IC	XXXX X000 <sub>2</sub>
006A <sub>16</sub>	DMA2 Interrupt Control Register	DM2IC	XXXX X000 <sub>2</sub>
006B <sub>16</sub>	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X000 <sub>2</sub>
006C <sub>16</sub>	Timer A0 Interrupt Control Register	TA0IC	XXXX X000 <sub>2</sub>
006D <sub>16</sub>	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X000 <sub>2</sub>
006E <sub>16</sub>	Timer A2 Interrupt Control Register	TA2IC	XXXX X000 <sub>2</sub>
006F <sub>16</sub>	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X000 <sub>2</sub>
0070 <sub>16</sub>	Timer A4 Interrupt Control Register	TA4IC	XXXX X000 <sub>2</sub>
0071 <sub>16</sub>	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000 <sub>2</sub>
0072 <sub>16</sub>	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000 <sub>2</sub>
0073 <sub>16</sub>	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000 <sub>2</sub>
0074 <sub>16</sub>	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000 <sub>2</sub>
0075 <sub>16</sub>	Intelligent I/O Interrupt Control Register 0/ CAN Interrupt 3 Control Register	IIO0IC/ CAN3IC	XXXX X000 <sub>2</sub>
0076 <sub>16</sub>	Timer B1 Interrupt Control Register	TB1IC	XXXX X000 <sub>2</sub>
0077 <sub>16</sub>	Intelligent I/O Interrupt Control Register 2/ CAN Interrupt 6 Control Register	IIO2IC/ CAN6IC	XXXX X000 <sub>2</sub>
0078 <sub>16</sub>	Timer B3 Interrupt Control Register	TB3IC	XXXX X000 <sub>2</sub>
0079 <sub>16</sub>	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000 <sub>2</sub>
007A <sub>16</sub>	INT5 Interrupt Control Register	INT5IC	XX00 X000 <sub>2</sub>
007B <sub>16</sub>	CAN Interrupt 8 Control Register	CAN8IC	XXXX X000 <sub>2</sub>
007C <sub>16</sub>	INT3 Interrupt Control Register	INT3IC	XX00 X000 <sub>2</sub>
007D <sub>16</sub>	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000 <sub>2</sub>
007E <sub>16</sub>	INT1 Interrupt Control Register	INT1IC	XX00 X000 <sub>2</sub>
007F <sub>16</sub>	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC/ CAN1IC	XXXX X000 <sub>2</sub>
0080 <sub>16</sub>			
0081 <sub>16</sub>	CAN Interrupt 2 Control Register	CAN2IC	XXXX X000 <sub>2</sub>
0082 <sub>16</sub>			
0083 <sub>16</sub>			
0084 <sub>16</sub>			
0085 <sub>16</sub>			
0086 <sub>16</sub>			
0087 <sub>16</sub>			
0088 <sub>16</sub>	DMA1 Interrupt Control Register	DM1IC	XXXX X000 <sub>2</sub>
0089 <sub>16</sub>	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X000 <sub>2</sub>
008A <sub>16</sub>	DMA3 Interrupt Control Register	DM3IC	XXXX X000 <sub>2</sub>
008B <sub>16</sub>	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X000 <sub>2</sub>
008C <sub>16</sub>	Timer A1 Interrupt Control Register	TA1IC	XXXX X000 <sub>2</sub>
008D <sub>16</sub>	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X000 <sub>2</sub>
008E <sub>16</sub>	Timer A3 Interrupt Control Register	TA3IC	XXXX X000 <sub>2</sub>
008F <sub>16</sub>	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X000 <sub>2</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 <sub>16</sub>	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
0091 <sub>16</sub>	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
0092 <sub>16</sub>	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
0093 <sub>16</sub>	Key Input Interrupt Control Register	KUPIC	XXXX X0002
0094 <sub>16</sub>	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
0095 <sub>16</sub>	Intelligent I/O Interrupt Control Register 1/ CAN Interrupt 4 Control Register	IIO1IC/ CAN4IC	XXXX X0002
0096 <sub>16</sub>	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
0097 <sub>16</sub>	Intelligent I/O Interrupt Control Register 3/ CAN Interrupt 7 Control Register	IIO3IC/ CAN7IC	XXXX X0002
0098 <sub>16</sub>	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
0099 <sub>16</sub>	CAN Interrupt 5 Control Register	CAN5IC	XXXX X0002
009A <sub>16</sub>	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B <sub>16</sub>			
009C <sub>16</sub>	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D <sub>16</sub>	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC/ CAN0IC	XXXX X0002
009E <sub>16</sub>	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F <sub>16</sub>	Exit Priority Control Register	RLVL	XXXX 00002
00A0 <sub>16</sub>	Interrupt Request Register 0	IIO0IR	0000 000X2
00A1 <sub>16</sub>	Interrupt Request Register 1	IIO1IR	0000 000X2
00A2 <sub>16</sub>	Interrupt Request Register 2	IIO2IR	0000 000X2
00A3 <sub>16</sub>	Interrupt Request Register 3	IIO3IR	0000 000X2
00A4 <sub>16</sub>	Interrupt Request Register 4	IIO4IR	0000 000X2
00A5 <sub>16</sub>	Interrupt Request Register 5	IIO5IR	0000 000X2
00A6 <sub>16</sub>	Interrupt Request Register 6	IIO6IR	0000 000X2
00A7 <sub>16</sub>			
00A8 <sub>16</sub>	Interrupt Request Register 8	IIO8IR	0000 000X2
00A9 <sub>16</sub>	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA <sub>16</sub>	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB <sub>16</sub>	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC <sub>16</sub>			
00AD <sub>16</sub>			
00AE <sub>16</sub>			
00AF <sub>16</sub>			
00B0 <sub>16</sub>	Interrupt Enable Register 0	IIO0IE	00 <sub>16</sub>
00B1 <sub>16</sub>	Interrupt Enable Register 1	IIO1IE	00 <sub>16</sub>
00B2 <sub>16</sub>	Interrupt Enable Register 2	IIO2IE	00 <sub>16</sub>
00B3 <sub>16</sub>	Interrupt Enable Register 3	IIO3IE	00 <sub>16</sub>
00B4 <sub>16</sub>	Interrupt Enable Register 4	IIO4IE	00 <sub>16</sub>
00B5 <sub>16</sub>	Interrupt Enable Register 5	IIO5IE	00 <sub>16</sub>
00B6 <sub>16</sub>	Interrupt Enable Register 6	IIO6IE	00 <sub>16</sub>
00B7 <sub>16</sub>			
00B8 <sub>16</sub>	Interrupt Enable Register 8	IIO8IE	00 <sub>16</sub>
00B9 <sub>16</sub>	Interrupt Enable Register 9	IIO9IE	00 <sub>16</sub>
00BA <sub>16</sub>	Interrupt Enable Register 10	IIO10IE	00 <sub>16</sub>
00BB <sub>16</sub>	Interrupt Enable Register 11	IIO11IE	00 <sub>16</sub>
00BC <sub>16</sub>			
00BD <sub>16</sub>			
00BE <sub>16</sub>			
00BF <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.



Address	Register	Symbol	Value after RESET
00C0 <sup>16</sup>			
00C1 <sup>16</sup>			
00C2 <sup>16</sup>			
00C3 <sup>16</sup>			
00C4 <sup>16</sup>			
00C5 <sup>16</sup>			
00C6 <sup>16</sup>			
00C7 <sup>16</sup>			
00C8 <sup>16</sup>			
00C9 <sup>16</sup>			
00CA <sup>16</sup>			
00CB <sup>16</sup>			
00CC <sup>16</sup>			
00CD <sup>16</sup>			
00CE <sup>16</sup>			
00CF <sup>16</sup>			
00D0 <sup>16</sup>			
00D1 <sup>16</sup>			
00D2 <sup>16</sup>			
00D3 <sup>16</sup>			
00D4 <sup>16</sup>			
00D5 <sup>16</sup>			
00D6 <sup>16</sup>			
00D7 <sup>16</sup>			
00D8 <sup>16</sup>			
00D9 <sup>16</sup>			
00DA <sup>16</sup>			
00DB <sup>16</sup>			
00DC <sup>16</sup>			
00DD <sup>16</sup>			
00DE <sup>16</sup>			
00DF <sup>16</sup>			
00E0 <sup>16</sup>			
00E1 <sup>16</sup>			
00E2 <sup>16</sup>			
00E3 <sup>16</sup>			
00E4 <sup>16</sup>			
00E5 <sup>16</sup>			
00E6 <sup>16</sup>			
00E7 <sup>16</sup>			
00E8 <sup>16</sup> 00E9 <sup>16</sup>	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX <sub>2</sub> XXX0 XXXX <sub>2</sub>
00EA <sup>16</sup> 00EB <sup>16</sup>	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX <sub>16</sub>
00EC <sup>16</sup>	Receive Input Register 0	G0RI	XX <sub>16</sub>
00ED <sup>16</sup>	SI/O Communication Mode Register 0	G0MR	00 <sub>16</sub>
00EE <sup>16</sup>	Transmit Output Register 0	G0TO	XX <sub>16</sub>
00EF <sup>16</sup>	SI/O Communication Control Register 0	G0CR	0000 X011 <sub>2</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0 <sub>16</sub>	Data Compare Register 00	G0CMP0	XX <sub>16</sub>
00F1 <sub>16</sub>	Data Compare Register 01	G0CMP1	XX <sub>16</sub>
00F2 <sub>16</sub>	Data Compare Register 02	G0CMP2	XX <sub>16</sub>
00F3 <sub>16</sub>	Data Compare Register 03	G0CMP3	XX <sub>16</sub>
00F4 <sub>16</sub>	Data Mask Register 00	G0MSK0	XX <sub>16</sub>
00F5 <sub>16</sub>	Data Mask Register 01	G0MSK1	XX <sub>16</sub>
00F6 <sub>16</sub>	Communication Clock Select Register	CCS	XXXX 0000 <sub>2</sub>
00F7 <sub>16</sub>			
00F8 <sub>16</sub> 00F9 <sub>16</sub>	Receive CRC Code Register 0	G0RCRC	XX <sub>16</sub> XX <sub>16</sub>
00FA <sub>16</sub> 00FB <sub>16</sub>	Transmit CRC Code Register 0	G0TCRC	00 <sub>16</sub> 00 <sub>16</sub>
00FC <sub>16</sub>	SI/O Extended Mode Register 0	G0EMR	00 <sub>16</sub>
00FD <sub>16</sub>	SI/O Extended Receive Control Register 0	G0ERC	00 <sub>16</sub>
00FE <sub>16</sub>	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00 <sub>16</sub>
00FF <sub>16</sub>	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX <sub>2</sub>
0100 <sub>16</sub> 0101 <sub>16</sub>	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX <sub>16</sub> XX <sub>16</sub>
0102 <sub>16</sub> 0103 <sub>16</sub>	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX <sub>16</sub> XX <sub>16</sub>
0104 <sub>16</sub> 0105 <sub>16</sub>	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX <sub>16</sub> XX <sub>16</sub>
0106 <sub>16</sub> 0107 <sub>16</sub>	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX <sub>16</sub> XX <sub>16</sub>
0108 <sub>16</sub> 0109 <sub>16</sub>	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX <sub>16</sub> XX <sub>16</sub>
010A <sub>16</sub> 010B <sub>16</sub>	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX <sub>16</sub> XX <sub>16</sub>
010C <sub>16</sub> 010D <sub>16</sub>	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX <sub>16</sub> XX <sub>16</sub>
010E <sub>16</sub> 010F <sub>16</sub>	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX <sub>16</sub> XX <sub>16</sub>
0110 <sub>16</sub>	Waveform Generating Control Register 10	G1POCR0	0000 X000 <sub>2</sub>
0111 <sub>16</sub>	Waveform Generating Control Register 11	G1POCR1	0X00 X000 <sub>2</sub>
0112 <sub>16</sub>	Waveform Generating Control Register 12	G1POCR2	0X00 X000 <sub>2</sub>
0113 <sub>16</sub>	Waveform Generating Control Register 13	G1POCR3	0X00 X000 <sub>2</sub>
0114 <sub>16</sub>	Waveform Generating Control Register 14	G1POCR4	0X00 X000 <sub>2</sub>
0115 <sub>16</sub>	Waveform Generating Control Register 15	G1POCR5	0X00 X000 <sub>2</sub>
0116 <sub>16</sub>	Waveform Generating Control Register 16	G1POCR6	0X00 X000 <sub>2</sub>
0117 <sub>16</sub>	Waveform Generating Control Register 17	G1POCR7	0X00 X000 <sub>2</sub>
0118 <sub>16</sub>	Time Measurement Control Register 10	G1TMCR0	00 <sub>16</sub>
0119 <sub>16</sub>	Time Measurement Control Register 11	G1TMCR1	00 <sub>16</sub>
011A <sub>16</sub>	Time Measurement Control Register 12	G1TMCR2	00 <sub>16</sub>
011B <sub>16</sub>	Time Measurement Control Register 13	G1TMCR3	00 <sub>16</sub>
011C <sub>16</sub>	Time Measurement Control Register 14	G1TMCR4	00 <sub>16</sub>
011D <sub>16</sub>	Time Measurement Control Register 15	G1TMCR5	00 <sub>16</sub>
011E <sub>16</sub>	Time Measurement Control Register 16	G1TMCR6	00 <sub>16</sub>
011F <sub>16</sub>	Time Measurement Control Register 17	G1TMCR7	00 <sub>16</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0120 <sub>16</sub> 0121 <sub>16</sub>	Base Timer Register 1	G1BT	XX <sub>16</sub> XX <sub>16</sub>
0122 <sub>16</sub>	Base Timer Control Register 10	G1BCR0	00 <sub>16</sub>
0123 <sub>16</sub>	Base Timer Control Register 11	G1BCR1	X000 000X <sub>2</sub>
0124 <sub>16</sub>	Time Measurement Prescaler Register 16	G1TPR6	00 <sub>16</sub>
0125 <sub>16</sub>	Time Measurement Prescaler Register 17	G1TPR7	00 <sub>16</sub>
0126 <sub>16</sub>	Function Enable Register 1	G1FE	00 <sub>16</sub>
0127 <sub>16</sub>	Function Select Register 1	G1FS	00 <sub>16</sub>
0128 <sub>16</sub> 0129 <sub>16</sub>	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX <sub>2</sub> X000 XXXX <sub>2</sub>
012A <sub>16</sub> 012B <sub>16</sub>	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX <sub>16</sub>
012C <sub>16</sub>	Receive Input Register 1	G1RI	XX <sub>16</sub>
012D <sub>16</sub>	SI/O Communication Mode Register 1	G1MR	00 <sub>16</sub>
012E <sub>16</sub>	Transmit Output Register 1	G1TO	XX <sub>16</sub>
012F <sub>16</sub>	SI/O Communication Control Register 1	G1CR	0000 X011 <sub>2</sub>
0130 <sub>16</sub>	Data Compare Register 10	G1CMP0	XX <sub>16</sub>
0131 <sub>16</sub>	Data Compare Register 11	G1CMP1	XX <sub>16</sub>
0132 <sub>16</sub>	Data Compare Register 12	G1CMP2	XX <sub>16</sub>
0133 <sub>16</sub>	Data Compare Register 13	G1CMP3	XX <sub>16</sub>
0134 <sub>16</sub>	Data Mask Register 10	G1MSK0	XX <sub>16</sub>
0135 <sub>16</sub>	Data Mask Register 11	G1MSK1	XX <sub>16</sub>
0136 <sub>16</sub>			
0137 <sub>16</sub>			
0138 <sub>16</sub> 0139 <sub>16</sub>	Receive CRC Code Register 1	G1RCRC	XX <sub>16</sub> XX <sub>16</sub>
013A <sub>16</sub> 013B <sub>16</sub>	Transmit CRC Code Register 1	G1TCRC	00 <sub>16</sub> 00 <sub>16</sub>
013C <sub>16</sub>	SI/O Extended Mode Register 1	G1EMR	00 <sub>16</sub>
013D <sub>16</sub>	SI/O Extended Receive Control Register 1	G1ERC	00 <sub>16</sub>
013E <sub>16</sub>	SI/O Special Communication Interrupt Detection Register 1	G1IRF	00 <sub>16</sub>
013F <sub>16</sub>	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX <sub>2</sub>
0140 <sub>16</sub>			
0141 <sub>16</sub>			
0142 <sub>16</sub>			
0143 <sub>16</sub>			
0144 <sub>16</sub>			
0145 <sub>16</sub>			
0146 <sub>16</sub>			
0147 <sub>16</sub>			
0148 <sub>16</sub>			
0149 <sub>16</sub>			
014A <sub>16</sub>			
014B <sub>16</sub>			
014C <sub>16</sub>			
014D <sub>16</sub> to 016F <sub>16</sub>			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0170 <sub>16</sub>	CAN2 Slot Buffer Select Register	C2SBS	00 <sub>16</sub> <sup>(1)</sup>
0171 <sub>16</sub>	CAN2 Control Register 1	C2CTLR1	X000 00XX <sub>2</sub> <sup>(1)</sup>
0172 <sub>16</sub>	CAN2 Sleep Control Register	C2SLPR	XXXX XXX0 <sub>2</sub>
0173 <sub>16</sub>			
0174 <sub>16</sub> 0175 <sub>16</sub>	CAN2 Acceptance Filter Support Register	C2AFS	00 <sub>16</sub> <sup>(1)</sup> 01 <sub>16</sub> <sup>(1)</sup>
0176 <sub>16</sub>			
0177 <sub>16</sub>			
0178 <sub>16</sub>	Input Function Select Register	IPS	00 <sub>16</sub>
0179 <sub>16</sub>	Input Function Select Register A	IPSA	00 <sub>16</sub>
017A <sub>16</sub>			
017B <sub>16</sub>			
017C <sub>16</sub>			
017D <sub>16</sub>			
017E <sub>16</sub>			
017F <sub>16</sub>			
0180 <sub>16</sub>	CAN2 Message Slot Buffer 0 Standard ID0	C2SLOT0_0	XX <sub>16</sub>
0181 <sub>16</sub>	CAN2 Message Slot Buffer 0 Standard ID1	C2SLOT0_1	XX <sub>16</sub>
0182 <sub>16</sub>	CAN2 Message Slot Buffer 0 Extended ID0	C2SLOT0_2	XX <sub>16</sub>
0183 <sub>16</sub>	CAN2 Message Slot Buffer 0 Extended ID1	C2SLOT0_3	XX <sub>16</sub>
0184 <sub>16</sub>	CAN2 Message Slot Buffer 0 Extended ID2	C2SLOT0_4	XX <sub>16</sub>
0185 <sub>16</sub>	CAN2 Message Slot Buffer 0 Data Length Code	C2SLOT0_5	XX <sub>16</sub>
0186 <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 0	C2SLOT0_6	XX <sub>16</sub>
0187 <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 1	C2SLOT0_7	XX <sub>16</sub>
0188 <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 2	C2SLOT0_8	XX <sub>16</sub>
0189 <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 3	C2SLOT0_9	XX <sub>16</sub>
018A <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 4	C2SLOT0_10	XX <sub>16</sub>
018B <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 5	C2SLOT0_11	XX <sub>16</sub>
018C <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 6	C2SLOT0_12	XX <sub>16</sub>
018D <sub>16</sub>	CAN2 Message Slot Buffer 0 Data 7	C2SLOT0_13	XX <sub>16</sub>
018E <sub>16</sub>	CAN2 Message Slot Buffer 0 Time Stamp High-Order	C2SLOT0_14	XX <sub>16</sub>
018F <sub>16</sub>	CAN2 Message Slot Buffer 0 Time Stamp Low-Order	C2SLOT0_15	XX <sub>16</sub>
0190 <sub>16</sub>	CAN2 Message Slot Buffer 1 Standard ID0	C2SLOT1_0	XX <sub>16</sub>
0191 <sub>16</sub>	CAN2 Message Slot Buffer 1 Standard ID1	C2SLOT1_1	XX <sub>16</sub>
0192 <sub>16</sub>	CAN2 Message Slot Buffer 1 Extended ID0	C2SLOT1_2	XX <sub>16</sub>
0193 <sub>16</sub>	CAN2 Message Slot Buffer 1 Extended ID1	C2SLOT1_3	XX <sub>16</sub>
0194 <sub>16</sub>	CAN2 Message Slot Buffer 1 Extended ID2	C2SLOT1_4	XX <sub>16</sub>
0195 <sub>16</sub>	CAN2 Message Slot Buffer 1 Data Length Code	C2SLOT1_5	XX <sub>16</sub>
0196 <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 0	C2SLOT1_6	XX <sub>16</sub>
0197 <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 1	C2SLOT1_7	XX <sub>16</sub>
0198 <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 2	C2SLOT1_8	XX <sub>16</sub>
0199 <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 3	C2SLOT1_9	XX <sub>16</sub>
019A <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 4	C2SLOT1_10	XX <sub>16</sub>
019B <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 5	C2SLOT1_11	XX <sub>16</sub>
019C <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 6	C2SLOT1_12	XX <sub>16</sub>
019D <sub>16</sub>	CAN2 Message Slot Buffer 1 Data 7	C2SLOT1_13	XX <sub>16</sub>
019E <sub>16</sub>	CAN2 Message Slot Buffer 1 Time Stamp High-Order	C2SLOT1_14	XX <sub>16</sub>
019F <sub>16</sub>	CAN2 Message Slot Buffer 1 Time Stamp Low-Order	C2SLOT1_15	XX <sub>16</sub>

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NOTE:

1. Values are obtained by setting the SLEEP bit in the C2SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
01A0 <sub>16</sub> 01A1 <sub>16</sub>	CAN2 Control Register 0	C2CTLR0	XX01 0X01 <sub>2</sub> <sup>(2)</sup> XXXX 0000 <sub>2</sub> <sup>(2)</sup>
01A2 <sub>16</sub> 01A3 <sub>16</sub>	CAN2 Status Register	C2STR	0000 0000 <sub>2</sub> <sup>(2)</sup> X000 0X01 <sub>2</sub> <sup>(2)</sup>
01A4 <sub>16</sub> 01A5 <sub>16</sub>	CAN2 Extended ID Register	C2IDR	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
01A6 <sub>16</sub> 01A7 <sub>16</sub>	CAN2 Configuration Register	C2CONR	0000 XXXX <sub>2</sub> <sup>(2)</sup> 0000 0000 <sub>2</sub> <sup>(2)</sup>
01A8 <sub>16</sub> 01A9 <sub>16</sub>	CAN2 Time Stamp Register	C2TSR	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
01AA <sub>16</sub>	CAN2 Transmit Error Count Register	C2TEC	00 <sub>16</sub> <sup>(2)</sup>
01AB <sub>16</sub>	CAN2 Receive Error Count Register	C2REC	00 <sub>16</sub> <sup>(2)</sup>
01AC <sub>16</sub> 01AD <sub>16</sub>	CAN2 Slot Interrupt Status Register	C2SISTR	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
01AE <sub>16</sub>			
01AF <sub>16</sub>			
01B0 <sub>16</sub> 01B1 <sub>16</sub>	CAN2 Slot Interrupt Mask Register	C2SIMKR	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
01B2 <sub>16</sub>			
01B3 <sub>16</sub>			
01B4 <sub>16</sub>	CAN2 Error Interrupt Mask Register	C2EIMKR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
01B5 <sub>16</sub>	CAN2 Error Interrupt Status Register	C2EISTR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
01B6 <sub>16</sub>	CAN2 Error Cause Register	C2EFR	00 <sub>16</sub> <sup>(2)</sup>
01B7 <sub>16</sub>	CAN2 Baud Rate Prescaler	C2BRP	0000 0001 <sub>2</sub> <sup>(2)</sup>
01B8 <sub>16</sub>			
01B9 <sub>16</sub>	CAN2 Mode Register	C2MDR	XXXX XX00 <sub>2</sub> <sup>(2)</sup>
01BA <sub>16</sub>			
01BB <sub>16</sub>			
01BC <sub>16</sub>			
01BD <sub>16</sub>			
01BE <sub>16</sub>			
01BF <sub>16</sub>			
01C0 <sub>16</sub> 01C1 <sub>16</sub>	CAN2 Single Shot Control Register	C2SSCTLR	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
01C2 <sub>16</sub>			
01C3 <sub>16</sub>			
01C4 <sub>16</sub> 01C5 <sub>16</sub>	CAN2 Single Shot Status Register	C2SSSTR	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
01C6 <sub>16</sub>			
01C7 <sub>16</sub>			
01C8 <sub>16</sub>	CAN2 Global Mask Register Standard ID0	C2GMR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
01C9 <sub>16</sub>	CAN2 Global Mask Register Standard ID1	C2GMR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
01CA <sub>16</sub>	CAN2 Global Mask Register Extended ID0	C2GMR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
01CB <sub>16</sub>	CAN2 Global Mask Register Extended ID1	C2GMR3	00 <sub>16</sub> <sup>(2)</sup>
01CC <sub>16</sub>	CAN2 Global Mask Register Extended ID2	C2GMR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
01CD <sub>16</sub>			
01CE <sub>16</sub>			
01CF <sub>16</sub>			

(Note 1)

X: Indeterminate

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## NOTES:

1. The BANKSEL bit in the C2CTLR1 register switches functions for addresses 01C0<sub>16</sub> to 01DF<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C2SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
01D0 <sub>16</sub>	CAN2 Message Slot 0 Control Register /	C2MCTL0/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register A Standard ID0	C2LMAR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
01D1 <sub>16</sub>	CAN2 Message Slot 1 Control Register /	C2MCTL1/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register A Standard ID1	C2LMAR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
01D2 <sub>16</sub>	CAN2 Message Slot 2 Control Register /	C2MCTL2/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register A Extended ID0	C2LMAR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
01D3 <sub>16</sub>	CAN2 Message Slot 3 Control Register /	C2MCTL3/	00 <sub>16</sub> <sup>(2)</sup>
	CAN2 local Mask Register A Extended ID1	C2LMAR3	00 <sub>16</sub> <sup>(2)</sup>
01D4 <sub>16</sub>	CAN2 Message Slot 4 Control Register /	C2MCTL4/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register A Extended ID2	C2LMAR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
01D5 <sub>16</sub>	CAN2 Message Slot 5 Control Register	C2MCTL5	00 <sub>16</sub> <sup>(2)</sup>
01D6 <sub>16</sub>	CAN2 Message Slot 6 Control Register	C2MCTL6	00 <sub>16</sub> <sup>(2)</sup>
01D7 <sub>16</sub>	CAN2 Message Slot 7 Control Register	C2MCTL7	00 <sub>16</sub> <sup>(2)</sup>
01D8 <sub>16</sub>	CAN2 Message Slot 8 Control Register /	C2MCTL8/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register B Standard ID0	C2LMBR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
01D9 <sub>16</sub>	CAN2 Message Slot 9 Control Register /	C2MCTL9/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register B Standard ID1	C2LMBR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
01DA <sub>16</sub>	CAN2 Message Slot 10 Control Register /	C2MCTL10/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register B Extended ID2	C2LMBR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
01DB <sub>16</sub>	CAN2 Message Slot 11 Control Register /	C2MCTL11/	00 <sub>16</sub> <sup>(2)</sup>
	CAN2 Local Mask Register B Extended ID3	C2LMBR3	00 <sub>16</sub> <sup>(2)</sup>
01DC <sub>16</sub>	CAN2 Message Slot 12 Control Register /	C2MCTL12/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN2 Local Mask Register B Extended ID4	C2LMBR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
01DD <sub>16</sub>	CAN2 Message Slot 13 Control Register	C2MCTL13	00 <sub>16</sub> <sup>(2)</sup>
01DE <sub>16</sub>	CAN2 Message Slot 14 Control Register	C2MCTL14	00 <sub>16</sub> <sup>(2)</sup>
01DF <sub>16</sub>	CAN2 Message Slot 15 Control Register	C2MCTL15	00 <sub>16</sub> <sup>(2)</sup>

(Note 1)

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## NOTES:

1. The BANKSEL bit in the C2CTLR1 register switches functions for addresses 01C0<sub>16</sub> to 01DF<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C2SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
01E0 <sub>16</sub>	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX <sub>16</sub>
01E1 <sub>16</sub>	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX <sub>16</sub>
01E2 <sub>16</sub>	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX <sub>16</sub>
01E3 <sub>16</sub>	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX <sub>16</sub>
01E4 <sub>16</sub>	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX <sub>16</sub>
01E5 <sub>16</sub>	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX <sub>16</sub>
01E6 <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX <sub>16</sub>
01E7 <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX <sub>16</sub>
01E8 <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX <sub>16</sub>
01E9 <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX <sub>16</sub>
01EA <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX <sub>16</sub>
01EB <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX <sub>16</sub>
01EC <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX <sub>16</sub>
01ED <sub>16</sub>	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX <sub>16</sub>
01EE <sub>16</sub>	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX <sub>16</sub>
01EF <sub>16</sub>	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX <sub>16</sub>
01F0 <sub>16</sub>	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX <sub>16</sub>
01F1 <sub>16</sub>	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX <sub>16</sub>
01F2 <sub>16</sub>	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX <sub>16</sub>
01F3 <sub>16</sub>	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX <sub>16</sub>
01F4 <sub>16</sub>	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX <sub>16</sub>
01F5 <sub>16</sub>	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX <sub>16</sub>
01F6 <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX <sub>16</sub>
01F7 <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX <sub>16</sub>
01F8 <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX <sub>16</sub>
01F9 <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX <sub>16</sub>
01FA <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX <sub>16</sub>
01FB <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX <sub>16</sub>
01FC <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX <sub>16</sub>
01FD <sub>16</sub>	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX <sub>16</sub>
01FE <sub>16</sub>	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX <sub>16</sub>
01FF <sub>16</sub>	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX <sub>16</sub>
0200 <sub>16</sub> 0201 <sub>16</sub>	CAN0 Control Register 0	C0CTRL0	XX01 0X01 <sub>2</sub> <sup>(1)</sup> XXXX 0000 <sub>2</sub> <sup>(1)</sup>
0202 <sub>16</sub> 0203 <sub>16</sub>	CAN0 Status Register	C0STR	0000 0000 <sub>2</sub> <sup>(1)</sup> X000 0X01 <sub>2</sub> <sup>(1)</sup>
0204 <sub>16</sub> 0205 <sub>16</sub>	CAN0 Extended ID Register	C0IDR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
0206 <sub>16</sub> 0207 <sub>16</sub>	CAN0 Configuration Register	C0CONR	0000 XXXX <sub>2</sub> <sup>(1)</sup> 0000 0000 <sub>2</sub> <sup>(1)</sup>
0208 <sub>16</sub> 0209 <sub>16</sub>	CAN0 Time Stamp Register	C0TSR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
020A <sub>16</sub>	CAN0 Transmit Error Count Register	C0TEC	00 <sub>16</sub> <sup>(1)</sup>
020B <sub>16</sub>	CAN0 Receive Error Count Register	C0REC	00 <sub>16</sub> <sup>(1)</sup>
020C <sub>16</sub> 020D <sub>16</sub>	CAN0 Slot Interrupt Status Register	C0SISTR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
020E <sub>16</sub>			
020F <sub>16</sub>			

X: Indeterminate

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NOTE:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
0210 <sub>16</sub>	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 <sub>16</sub> <sup>(2)</sup>
0211 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
0212 <sub>16</sub>			
0213 <sub>16</sub>			
0214 <sub>16</sub>	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
0215 <sub>16</sub>	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
0216 <sub>16</sub>	CAN0 Error Cause Register	C0EFR	00 <sub>16</sub> <sup>(2)</sup>
0217 <sub>16</sub>	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 <sub>2</sub> <sup>(2)</sup>
0218 <sub>16</sub>			
0219 <sub>16</sub>	CAN0 Mode Register	C0MDR	XXXX XX00 <sub>2</sub> <sup>(2)</sup>
021A <sub>16</sub>			
021B <sub>16</sub>			
021C <sub>16</sub>			
021D <sub>16</sub>			
021E <sub>16</sub>			
021F <sub>16</sub>			
0220 <sub>16</sub>	CAN0 Single Shot Control Register	C0SSCTLR	00 <sub>16</sub> <sup>(2)</sup>
0221 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
0222 <sub>16</sub>			
0223 <sub>16</sub>			
0224 <sub>16</sub>	CAN0 Single Shot Status Register	C0SSSTR	00 <sub>16</sub> <sup>(2)</sup>
0225 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
0226 <sub>16</sub>			
0227 <sub>16</sub>			
0228 <sub>16</sub>	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
0229 <sub>16</sub>	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
022A <sub>16</sub>	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
022B <sub>16</sub>	CAN0 Global Mask Register Extended ID1	C0GMR3	00 <sub>16</sub> <sup>(2)</sup>
022C <sub>16</sub>	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
022D <sub>16</sub>			
022E <sub>16</sub>			
022F <sub>16</sub>			
0230 <sub>16</sub>	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000 <sub>2</sub> <sup>(2)</sup> XXX0 0000 <sub>2</sub> <sup>(2)</sup>
0231 <sub>16</sub>	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
0232 <sub>16</sub>	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000 <sub>2</sub> <sup>(2)</sup> XXXX 0000 <sub>2</sub> <sup>(2)</sup>
0233 <sub>16</sub>	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
0234 <sub>16</sub>	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
0235 <sub>16</sub>	CAN0 Message Slot 5 Control Register	C0MCTL5	00 <sub>16</sub> <sup>(2)</sup>
0236 <sub>16</sub>	CAN0 Message Slot 6 Control Register	C0MCTL6	00 <sub>16</sub> <sup>(2)</sup>
0237 <sub>16</sub>	CAN0 Message Slot 7 Control Register	C0MCTL7	00 <sub>16</sub> <sup>(2)</sup>
0238 <sub>16</sub>	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000 <sub>2</sub> <sup>(2)</sup> XXX0 0000 <sub>2</sub> <sup>(2)</sup>
0239 <sub>16</sub>	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220<sub>16</sub> to 023F<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.



Address	Register	Symbol	Value after RESET
023A <sub>16</sub>	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 0000 <sub>2</sub> <sup>(2)</sup> XXXX 0000 <sub>2</sub> <sup>(2)</sup>
023B <sub>16</sub>	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
023C <sub>16</sub>	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
023D <sub>16</sub>	CAN0 Message Slot 13 Control Register	C0MCTL13	00 <sub>16</sub> <sup>(2)</sup>
023E <sub>16</sub>	CAN0 Message Slot 14 Control Register	C0MCTL14	00 <sub>16</sub> <sup>(2)</sup>
023F <sub>16</sub>	CAN0 Message Slot 15 Control Register	C0MCTL15	00 <sub>16</sub> <sup>(2)</sup>
0240 <sub>16</sub>	CAN0 Slot Buffer Select Register	C0SBS	00 <sub>16</sub> <sup>(2)</sup>
0241 <sub>16</sub>	CAN0 Control Register 1	C0CTLR1	X000 00XX <sub>2</sub> <sup>(2)</sup>
0242 <sub>16</sub>	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0 <sub>2</sub>
0243 <sub>16</sub>			
0244 <sub>16</sub> 0245 <sub>16</sub>	CAN0 Acceptance Filter Support Register	C0AFS	00 <sub>16</sub> <sup>(2)</sup> 01 <sub>16</sub> <sup>(2)</sup>
0246 <sub>16</sub>			
0247 <sub>16</sub>			
0248 <sub>16</sub>			
0249 <sub>16</sub>			
024A <sub>16</sub>			
024B <sub>16</sub>			
024C <sub>16</sub>			
024D <sub>16</sub>			
024E <sub>16</sub>			
024F <sub>16</sub>			
0250 <sub>16</sub>	CAN1 Slot Buffer Select Register	C1SBS	00 <sub>16</sub> <sup>(3)</sup>
0251 <sub>16</sub>	CAN1 Control Register 1	C1CTLR1	X000 00XX <sub>2</sub> <sup>(3)</sup>
0252 <sub>16</sub>	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0 <sub>2</sub> <sup>(3)</sup>
0253 <sub>16</sub>			
0254 <sub>16</sub> 0255 <sub>16</sub>	CAN1 Acceptance Filter Support Register	C1AFS	00 <sub>16</sub> <sup>(3)</sup> 01 <sub>16</sub> <sup>(3)</sup>
0256 <sub>16</sub>			
0257 <sub>16</sub>			
0258 <sub>16</sub>			
0259 <sub>16</sub>			
025A <sub>16</sub>			
025B <sub>16</sub>			
025C <sub>16</sub>			
025D <sub>16</sub>			
025E <sub>16</sub>			
025F <sub>16</sub>			

(Note 1)

X: Indeterminate

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## NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220<sub>16</sub> to 023F<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
0260 <sub>16</sub>	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XX <sub>16</sub>
0261 <sub>16</sub>	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XX <sub>16</sub>
0262 <sub>16</sub>	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XX <sub>16</sub>
0263 <sub>16</sub>	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XX <sub>16</sub>
0264 <sub>16</sub>	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XX <sub>16</sub>
0265 <sub>16</sub>	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XX <sub>16</sub>
0266 <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XX <sub>16</sub>
0267 <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XX <sub>16</sub>
0268 <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XX <sub>16</sub>
0269 <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XX <sub>16</sub>
026A <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XX <sub>16</sub>
026B <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XX <sub>16</sub>
026C <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XX <sub>16</sub>
026D <sub>16</sub>	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XX <sub>16</sub>
026E <sub>16</sub>	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XX <sub>16</sub>
026F <sub>16</sub>	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XX <sub>16</sub>
0270 <sub>16</sub>	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XX <sub>16</sub>
0271 <sub>16</sub>	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XX <sub>16</sub>
0272 <sub>16</sub>	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XX <sub>16</sub>
0273 <sub>16</sub>	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XX <sub>16</sub>
0274 <sub>16</sub>	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XX <sub>16</sub>
0275 <sub>16</sub>	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XX <sub>16</sub>
0276 <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XX <sub>16</sub>
0277 <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XX <sub>16</sub>
0278 <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XX <sub>16</sub>
0279 <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XX <sub>16</sub>
027A <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XX <sub>16</sub>
027B <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XX <sub>16</sub>
027C <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XX <sub>16</sub>
027D <sub>16</sub>	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XX <sub>16</sub>
027E <sub>16</sub>	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XX <sub>16</sub>
027F <sub>16</sub>	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XX <sub>16</sub>
0280 <sub>16</sub> 0281 <sub>16</sub>	CAN1 Control Register 0	C1CTRL0	XX01 0X01 <sub>2</sub> <sup>(1)</sup> XXXX 0000 <sub>2</sub> <sup>(1)</sup>
0282 <sub>16</sub> 0283 <sub>16</sub>	CAN1 Status Register	C1STR	0000 0000 <sub>2</sub> <sup>(1)</sup> X000 0X01 <sub>2</sub> <sup>(1)</sup>
0284 <sub>16</sub> 0285 <sub>16</sub>	CAN1 Extended ID Register	C1IDR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
0286 <sub>16</sub> 0287 <sub>16</sub>	CAN1 Configuration Register	C1CONR	0000 XXXX <sub>2</sub> <sup>(1)</sup> 0000 0000 <sub>2</sub> <sup>(1)</sup>
0288 <sub>16</sub> 0289 <sub>16</sub>	CAN1 Time Stamp Register	C1TSR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
028A <sub>16</sub>	CAN1 Transmit Error Count Register	C1TEC	00 <sub>16</sub> <sup>(1)</sup>
028B <sub>16</sub>	CAN1 Receive Error Count Register	C1REC	00 <sub>16</sub> <sup>(1)</sup>
028C <sub>16</sub> 028D <sub>16</sub>	CAN1 Slot Interrupt Status Register	C1SISTR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
028E <sub>16</sub>			
028F <sub>16</sub>			

X: Indeterminate

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NOTE:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0290 <sub>16</sub>	CAN1 Slot Interrupt Mask Register	C1SIMKR	00 <sub>16</sub> <sup>(2)</sup>
0291 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
0292 <sub>16</sub>			
0293 <sub>16</sub>			
0294 <sub>16</sub>	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
0295 <sub>16</sub>	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
0296 <sub>16</sub>	CAN1 Error Factor Register	C1EFR	00 <sub>16</sub> <sup>(2)</sup>
0297 <sub>16</sub>	CAN1 Baud Rate Prescaler	C1BRP	0000 0001 <sub>2</sub> <sup>(2)</sup>
0298 <sub>16</sub>			
0299 <sub>16</sub>	CAN1 Mode Register	C1MDR	XXXX XX00 <sub>2</sub> <sup>(2)</sup>
029A <sub>16</sub>			
029B <sub>16</sub>			
029C <sub>16</sub>			
029D <sub>16</sub>			
029E <sub>16</sub>			
029F <sub>16</sub>			
02A0 <sub>16</sub>	CAN1 Single Shot Control Register	C1SSCTLR	00 <sub>16</sub> <sup>(2)</sup>
02A1 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
02A2 <sub>16</sub>			
02A3 <sub>16</sub>			
02A4 <sub>16</sub>	CAN1 Single Shot Status Register	C1SSSTR	00 <sub>16</sub> <sup>(2)</sup>
02A5 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
02A6 <sub>16</sub>			
02A7 <sub>16</sub>			
02A8 <sub>16</sub>	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
02A9 <sub>16</sub>	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
02AA <sub>16</sub>	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
02AB <sub>16</sub>	CAN1 Global Mask Register Extended ID1	C1GMR3	00 <sub>16</sub> <sup>(2)</sup>
02AC <sub>16</sub>	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
02AD <sub>16</sub>			
02AE <sub>16</sub>			
02AF <sub>16</sub>			
02B0 <sub>16</sub>	CAN1 Message Slot 0 Control Register /	C1MCTL0/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN1 Local Mask Register A Standard ID0	C1LMAR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
02B1 <sub>16</sub>	CAN1 Message Slot 1 Control Register /	C1MCTL1/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN1 Local Mask Register A Standard ID1	C1LMAR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
02B2 <sub>16</sub>	CAN1 Message Slot 2 Control Register /	C1MCTL2/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN1 Local Mask Register A Extended ID0	C1LMAR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
02B3 <sub>16</sub>	CAN1 Message Slot 3 Control Register /	C1MCTL3/	00 <sub>16</sub> <sup>(2)</sup>
	CAN1 Local Mask Register A Extended ID1	C1LMAR3	00 <sub>16</sub> <sup>(2)</sup>
02B4 <sub>16</sub>	CAN1 Message Slot 4 Control Register /	C1MCTL4/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN1 Local Mask Register A Extended ID2	C1LMAR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
02B5 <sub>16</sub>	CAN1 Message Slot 5 Control Register	C1MCTL5	00 <sub>16</sub> <sup>(2)</sup>
02B6 <sub>16</sub>	CAN1 Message Slot 6 Control Register	C1MCTL6	00 <sub>16</sub> <sup>(2)</sup>
02B7 <sub>16</sub>	CAN1 Message Slot 7 Control Register	C1MCTL7	00 <sub>16</sub> <sup>(2)</sup>
02B8 <sub>16</sub>	CAN1 Message Slot 8 Control Register /	C1MCTL8/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN1 Local Mask Register B Standard ID0	C1LMBR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
02B9 <sub>16</sub>	CAN1 Message Slot 9 Control Register /	C1MCTL9/	0000 0000 <sub>2</sub> <sup>(2)</sup>
	CAN1 Local Mask Register B Standard ID1	C1LMBR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>

(Note 1)

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## NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A0<sub>16</sub> to 02BF<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
02BA <sub>16</sub>	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10/ C1LMBR2	0000 0000 <sub>2</sub> <sup>(2)</sup> XXXX 0000 <sub>2</sub> <sup>(2)</sup>
02BB <sub>16</sub>	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11/ C1LMBR3	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
02BC <sub>16</sub>	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12/ C1LMBR4	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
02BD <sub>16</sub>	CAN1 Message Slot 13 Control Register	C1MCTL13	00 <sub>16</sub> <sup>(2)</sup>
02BE <sub>16</sub>	CAN1 Message Slot 14 Control Register	C1MCTL14	00 <sub>16</sub> <sup>(2)</sup>
02BF <sub>16</sub>	CAN1 Message Slot 15 Control Register	C1MCTL15	00 <sub>16</sub> <sup>(2)</sup>
02C0 <sub>16</sub> 02C1 <sub>16</sub>	X0 Register Y0 Register	X0R,Y0R	XX <sub>16</sub> XX <sub>16</sub>
02C2 <sub>16</sub> 02C3 <sub>16</sub>	X1 Register Y1 Register	X1R,Y1R	XX <sub>16</sub> XX <sub>16</sub>
02C4 <sub>16</sub> 02C5 <sub>16</sub>	X2 Register Y2 Register	X2R,Y2R	XX <sub>16</sub> XX <sub>16</sub>
02C6 <sub>16</sub> 02C7 <sub>16</sub>	X3 Register Y3 Register	X3R,Y3R	XX <sub>16</sub> XX <sub>16</sub>
02C8 <sub>16</sub> 02C9 <sub>16</sub>	X4 Register Y4 Register	X4R,Y4R	XX <sub>16</sub> XX <sub>16</sub>
02CA <sub>16</sub> 02CB <sub>16</sub>	X5 Register Y5 Register	X5R,Y5R	XX <sub>16</sub> XX <sub>16</sub>
02CC <sub>16</sub> 02CD <sub>16</sub>	X6 Register Y6 Register	X6R,Y6R	XX <sub>16</sub> XX <sub>16</sub>
02CE <sub>16</sub> 02CF <sub>16</sub>	X7 Register Y7 Register	X7R,Y7R	XX <sub>16</sub> XX <sub>16</sub>
02D0 <sub>16</sub> 02D1 <sub>16</sub>	X8 Register Y8 Register	X8R,Y8R	XX <sub>16</sub> XX <sub>16</sub>
02D2 <sub>16</sub> 02D3 <sub>16</sub>	X9 Register Y9 Register	X9R,Y9R	XX <sub>16</sub> XX <sub>16</sub>
02D4 <sub>16</sub> 02D5 <sub>16</sub>	X10 Register Y10 Register	X10R,Y10R	XX <sub>16</sub> XX <sub>16</sub>
02D6 <sub>16</sub> 02D7 <sub>16</sub>	X11 Register Y11 Register	X11R,Y11R	XX <sub>16</sub> XX <sub>16</sub>
02D8 <sub>16</sub> 02D9 <sub>16</sub>	X12 Register Y12 Register	X12R,Y12R	XX <sub>16</sub> XX <sub>16</sub>
02DA <sub>16</sub> 02DB <sub>16</sub>	X13 Register Y13 Register	X13R,Y13R	XX <sub>16</sub> XX <sub>16</sub>
02DC <sub>16</sub> 02DD <sub>16</sub>	X14 Register Y14 Register	X14R,Y14R	XX <sub>16</sub> XX <sub>16</sub>
02DE <sub>16</sub> 02DF <sub>16</sub>	X15 Register Y15 Register	X15R,Y15R	XX <sub>16</sub> XX <sub>16</sub>

(Note 1)

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## NOTES:

1. The BANKSEL bit in the C1CTRL1 register switches functions for addresses 02A0<sub>16</sub> to 02BF<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
02E0 <sub>16</sub>	X/Y Control Register	XYC	XXXX XX00 <sub>2</sub>
02E1 <sub>16</sub>			
02E2 <sub>16</sub>			
02E3 <sub>16</sub>			
02E4 <sub>16</sub>	UART1 Special Mode Register 4	U1SMR4	00 <sub>16</sub>
02E5 <sub>16</sub>	UART1 Special Mode Register 3	U1SMR3	00 <sub>16</sub>
02E6 <sub>16</sub>	UART1 Special Mode Register 2	U1SMR2	00 <sub>16</sub>
02E7 <sub>16</sub>	UART1 Special Mode Register	U1SMR	00 <sub>16</sub>
02E8 <sub>16</sub>	UART1 Transmit/Receive Mode Register	U1MR	00 <sub>16</sub>
02E9 <sub>16</sub>	UART1 Bit Rate Register	U1BRG	XX <sub>16</sub>
02EA <sub>16</sub>	UART1 Transmit Buffer Register	U1TB	XX <sub>16</sub>
02EB <sub>16</sub>			XX <sub>16</sub>
02EC <sub>16</sub>	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 <sub>2</sub>
02ED <sub>16</sub>	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 <sub>2</sub>
02EE <sub>16</sub>	UART1 Receive Buffer Register	U1RB	XX <sub>16</sub>
02EF <sub>16</sub>			XX <sub>16</sub>
02F0 <sub>16</sub>			
02F1 <sub>16</sub>			
02F2 <sub>16</sub>			
02F3 <sub>16</sub>			
02F4 <sub>16</sub>	UART4 Special Mode Register 4	U4SMR4	00 <sub>16</sub>
02F5 <sub>16</sub>	UART4 Special Mode Register 3	U4SMR3	00 <sub>16</sub>
02F6 <sub>16</sub>	UART4 Special Mode Register 2	U4SMR2	00 <sub>16</sub>
02F7 <sub>16</sub>	UART4 Special Mode Register	U4SMR	00 <sub>16</sub>
02F8 <sub>16</sub>	UART4 Transmit/Receive Mode Register	U4MR	00 <sub>16</sub>
02F9 <sub>16</sub>	UART4 Bit Rate Register	U4BRG	XX <sub>16</sub>
02FA <sub>16</sub>	UART4 Transmit Buffer Register	U4TB	XX <sub>16</sub>
02FB <sub>16</sub>			XX <sub>16</sub>
02FC <sub>16</sub>	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 <sub>2</sub>
02FD <sub>16</sub>	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 <sub>2</sub>
02FE <sub>16</sub>	UART4 Receive Buffer Register	U4RB	XX <sub>16</sub>
02FF <sub>16</sub>			XX <sub>16</sub>
0300 <sub>16</sub>	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX <sub>2</sub>
0301 <sub>16</sub>			
0302 <sub>16</sub>	Timer A1-1 Register	TA11	XX <sub>16</sub>
0303 <sub>16</sub>			XX <sub>16</sub>
0304 <sub>16</sub>	Timer A2-1 Register	TA21	XX <sub>16</sub>
0305 <sub>16</sub>			XX <sub>16</sub>
0306 <sub>16</sub>	Timer A4-1 Register	TA41	XX <sub>16</sub>
0307 <sub>16</sub>			XX <sub>16</sub>
0308 <sub>16</sub>	Three-Phase PWM Control Register 0	INVC0	00 <sub>16</sub>
0309 <sub>16</sub>	Three-Phase PWM Control Register 1	INVC1	00 <sub>16</sub>
030A <sub>16</sub>	Three-Phase Output Buffer Register 0	IDB0	XX11 1111 <sub>2</sub>
030B <sub>16</sub>	Three-Phase Output Buffer Register 1	IDB1	XX11 1111 <sub>2</sub>
030C <sub>16</sub>	Dead Time Timer	DTT	XX <sub>16</sub>
030D <sub>16</sub>	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX <sub>16</sub>
030E <sub>16</sub>			
030F <sub>16</sub>			

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Address	Register	Symbol	Value after RESET
0310 <sub>16</sub>	Timer B3 Register	TB3	XX <sub>16</sub>
0311 <sub>16</sub>			XX <sub>16</sub>
0312 <sub>16</sub>	Timer B4 Register	TB4	XX <sub>16</sub>
0313 <sub>16</sub>			XX <sub>16</sub>
0314 <sub>16</sub>	Timer B5 Register	TB5	XX <sub>16</sub>
0315 <sub>16</sub>			XX <sub>16</sub>
0316 <sub>16</sub>			
0317 <sub>16</sub>			
0318 <sub>16</sub>			
0319 <sub>16</sub>			
031A <sub>16</sub>			
031B <sub>16</sub>	Timer B3 Mode Register	TB3MR	00XX 0000 <sub>2</sub>
031C <sub>16</sub>	Timer B4 Mode Register	TB4MR	00XX 0000 <sub>2</sub>
031D <sub>16</sub>	Timer B5 Mode Register	TB5MR	00XX 0000 <sub>2</sub>
031E <sub>16</sub>			
031F <sub>16</sub>	External Interrupt Request Source Select Register	IFSR	00 <sub>16</sub>
0320 <sub>16</sub>			
0321 <sub>16</sub>			
0322 <sub>16</sub>			
0323 <sub>16</sub>			
0324 <sub>16</sub>	UART3 Special Mode Register 4	U3SMR4	00 <sub>16</sub>
0325 <sub>16</sub>	UART3 Special Mode Register 3	U3SMR3	00 <sub>16</sub>
0326 <sub>16</sub>	UART3 Special Mode Register 2	U3SMR2	00 <sub>16</sub>
0327 <sub>16</sub>	UART3 Special Mode Register	U3SMR	00 <sub>16</sub>
0328 <sub>16</sub>	UART3 Transmit/Receive Mode Register	U3MR	00 <sub>16</sub>
0329 <sub>16</sub>	UART3 Bit Rate Register	U3BRG	XX <sub>16</sub>
032A <sub>16</sub>	UART3 Transmit Buffer Register	U3TB	XX <sub>16</sub>
032B <sub>16</sub>			XX <sub>16</sub>
032C <sub>16</sub>	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 <sub>2</sub>
032D <sub>16</sub>	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 <sub>2</sub>
032E <sub>16</sub>	UART3 Receive Buffer Register	U3RB	XX <sub>16</sub>
032F <sub>16</sub>			XX <sub>16</sub>
0330 <sub>16</sub>			
0331 <sub>16</sub>			
0332 <sub>16</sub>			
0333 <sub>16</sub>			
0334 <sub>16</sub>	UART2 Special Mode Register 4	U2SMR4	00 <sub>16</sub>
0335 <sub>16</sub>	UART2 Special Mode Register 3	U2SMR3	00 <sub>16</sub>
0336 <sub>16</sub>	UART2 Special Mode Register 2	U2SMR2	00 <sub>16</sub>
0337 <sub>16</sub>	UART2 Special Mode Register	U2SMR	00 <sub>16</sub>
0338 <sub>16</sub>	UART2 Transmit/Receive Mode Register	U2MR	00 <sub>16</sub>
0339 <sub>16</sub>	UART2 Bit Rate Register	U2BRG	XX <sub>16</sub>
033A <sub>16</sub>	UART2 Transmit Buffer Register	U2TB	XX <sub>16</sub>
033B <sub>16</sub>			XX <sub>16</sub>
033C <sub>16</sub>	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 <sub>2</sub>
033D <sub>16</sub>	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 <sub>2</sub>
033E <sub>16</sub>	UART2 Receive Buffer Register	U2RB	XX <sub>16</sub>
033F <sub>16</sub>			XX <sub>16</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0340 <sub>16</sub>	Count Start Flag	TABSR	00 <sub>16</sub>
0341 <sub>16</sub>	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX <sub>2</sub>
0342 <sub>16</sub>	One-Shot Start Flag	ONSF	00 <sub>16</sub>
0343 <sub>16</sub>	Trigger Select Register	TRGSR	00 <sub>16</sub>
0344 <sub>16</sub>	Up/Down Flag	UDF	00 <sub>16</sub>
0345 <sub>16</sub>			
0346 <sub>16</sub> 0347 <sub>16</sub>	Timer A0 Register	TA0	XX <sub>16</sub> XX <sub>16</sub>
0348 <sub>16</sub> 0349 <sub>16</sub>	Timer A1 Register	TA1	XX <sub>16</sub> XX <sub>16</sub>
034A <sub>16</sub> 034B <sub>16</sub>	Timer A2 Register	TA2	XX <sub>16</sub> XX <sub>16</sub>
034C <sub>16</sub> 034D <sub>16</sub>	Timer A3 Register	TA3	XX <sub>16</sub> XX <sub>16</sub>
034E <sub>16</sub> 034F <sub>16</sub>	Timer A4 Register	TA4	XX <sub>16</sub> XX <sub>16</sub>
0350 <sub>16</sub> 0351 <sub>16</sub>	Timer B0 Register	TB0	XX <sub>16</sub> XX <sub>16</sub>
0352 <sub>16</sub> 0353 <sub>16</sub>	Timer B1 Register	TB1	XX <sub>16</sub> XX <sub>16</sub>
0354 <sub>16</sub> 0355 <sub>16</sub>	Timer B2 Register	TB2	XX <sub>16</sub> XX <sub>16</sub>
0356 <sub>16</sub>	Timer A0 Mode Register	TA0MR	00 <sub>16</sub>
0357 <sub>16</sub>	Timer A1 Mode Register	TA1MR	00 <sub>16</sub>
0358 <sub>16</sub>	Timer A2 Mode Register	TA2MR	00 <sub>16</sub>
0359 <sub>16</sub>	Timer A3 Mode Register	TA3MR	00 <sub>16</sub>
035A <sub>16</sub>	Timer A4 Mode Register	TA4MR	00 <sub>16</sub>
035B <sub>16</sub>	Timer B0 Mode Register	TB0MR	00XX 0000 <sub>2</sub>
035C <sub>16</sub>	Timer B1 Mode Register	TB1MR	00XX 0000 <sub>2</sub>
035D <sub>16</sub>	Timer B2 Mode Register	TB2MR	00XX 0000 <sub>2</sub>
035E <sub>16</sub>	Timer B2 Special Mode Register	TB2SC	XXXX XXX0 <sub>2</sub>
035F <sub>16</sub>	Count Source Prescaler Register <sup>(1)</sup>	TCSPR	0XXX 0000 <sub>2</sub>
0360 <sub>16</sub>			
0361 <sub>16</sub>			
0362 <sub>16</sub>			
0363 <sub>16</sub>			
0364 <sub>16</sub>	UART0 Special Mode Register 4	U0SMR4	00 <sub>16</sub>
0365 <sub>16</sub>	UART0 Special Mode Register 3	U0SMR3	00 <sub>16</sub>
0366 <sub>16</sub>	UART0 Special Mode Register 2	U0SMR2	00 <sub>16</sub>
0367 <sub>16</sub>	UART0 Special Mode Register	U0SMR	00 <sub>16</sub>
0368 <sub>16</sub>	UART0 Transmit/Receive Mode Register	U0MR	00 <sub>16</sub>
0369 <sub>16</sub>	UART0 Bit Rate Register	U0BRG	XX <sub>16</sub>
036A <sub>16</sub> 036B <sub>16</sub>	UART0 Transmit Buffer Register	U0TB	XX <sub>16</sub> XX <sub>16</sub>
036C <sub>16</sub>	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000 <sub>2</sub>
036D <sub>16</sub>	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010 <sub>2</sub>
036E <sub>16</sub> 036F <sub>16</sub>	UART0 Receive Buffer Register	U0RB	XX <sub>16</sub> XX <sub>16</sub>

X: Indeterminate

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NOTE:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0370 <sub>16</sub>			
0371 <sub>16</sub>			
0372 <sub>16</sub>			
0373 <sub>16</sub>			
0374 <sub>16</sub>			
0375 <sub>16</sub>			
0376 <sub>16</sub>			
0377 <sub>16</sub>			
0378 <sub>16</sub>	DMA0 Request Source Select Register	DM0SL	0X00 0000 <sub>2</sub>
0379 <sub>16</sub>	DMA1 Request Source Select Register	DM1SL	0X00 0000 <sub>2</sub>
037A <sub>16</sub>	DMA2 Request Source Select Register	DM2SL	0X00 0000 <sub>2</sub>
037B <sub>16</sub>	DMA3 Request Source Select Register	DM3SL	0X00 0000 <sub>2</sub>
037C <sub>16</sub>	CRC Data Register	CRCD	XX <sub>16</sub>
037D <sub>16</sub>			XX <sub>16</sub>
037E <sub>16</sub>	CRC Input Register	CRCIN	XX <sub>16</sub>
037F <sub>16</sub>			
0380 <sub>16</sub>	A/D0 Register 0	AD00	XXXX XXXX <sub>2</sub>
0381 <sub>16</sub>			0000 0000 <sub>2</sub>
0382 <sub>16</sub>	A/D0 Register 1	AD01	XX <sub>16</sub>
0383 <sub>16</sub>			XX <sub>16</sub>
0384 <sub>16</sub>	A/D0 Register 2	AD02	XX <sub>16</sub>
0385 <sub>16</sub>			XX <sub>16</sub>
0386 <sub>16</sub>	A/D0 Register 3	AD03	XX <sub>16</sub>
0387 <sub>16</sub>			XX <sub>16</sub>
0388 <sub>16</sub>	A/D0 Register 4	AD04	XX <sub>16</sub>
0389 <sub>16</sub>			XX <sub>16</sub>
038A <sub>16</sub>	A/D0 Register 5	AD05	XX <sub>16</sub>
038B <sub>16</sub>			XX <sub>16</sub>
038C <sub>16</sub>	A/D0 Register 6	AD06	XX <sub>16</sub>
038D <sub>16</sub>			XX <sub>16</sub>
038E <sub>16</sub>	A/D0 Register 7	AD07	XX <sub>16</sub>
038F <sub>16</sub>			XX <sub>16</sub>
0390 <sub>16</sub>			
0391 <sub>16</sub>			
0392 <sub>16</sub>	A/D0 Control Register 4	AD0CON4	XXXX 00XX <sub>2</sub>
0393 <sub>16</sub>			
0394 <sub>16</sub>	A/D0 Control Register 2	AD0CON2	XX0X X000 <sub>2</sub>
0395 <sub>16</sub>	A/D0 Control Register 3	AD0CON3	XXXX X000 <sub>2</sub>
0396 <sub>16</sub>	A/D0 Control Register 0	AD0CON0	00 <sub>16</sub>
0397 <sub>16</sub>	A/D0 Control Register 1	AD0CON1	00 <sub>16</sub>
0398 <sub>16</sub>	D/A Register 0	DA0	XX <sub>16</sub>
0399 <sub>16</sub>			
039A <sub>16</sub>	D/A Register 1	DA1	XX <sub>16</sub>
039B <sub>16</sub>			
039C <sub>16</sub>	D/A Control Register	DACON	XXXX XX00 <sub>2</sub>
039D <sub>16</sub>			
039E <sub>16</sub>			
039F <sub>16</sub>			

X: Indeterminate

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&lt;144-pin package&gt;

Address	Register	Symbol	Value after RESET
03A0 <sub>16</sub>	Function Select Register A8	PS8	X000 0000 <sub>2</sub>
03A1 <sub>16</sub>	Function Select Register A9	PS9	00 <sub>16</sub>
03A2 <sub>16</sub>			
03A3 <sub>16</sub>			
03A4 <sub>16</sub>			
03A5 <sub>16</sub>			
03A6 <sub>16</sub>			
03A7 <sub>16</sub>	Function Select Register D1	PSD1	X0XX XX00 <sub>2</sub>
03A8 <sub>16</sub>			
03A9 <sub>16</sub>			
03AA <sub>16</sub>			
03AB <sub>16</sub>			
03AC <sub>16</sub>	Function Select Register C2	PSC2	XXXX X00X <sub>2</sub>
03AD <sub>16</sub>	Function Select Register C3	PSC3	X0XX XXXX <sub>2</sub>
03AE <sub>16</sub>			
03AF <sub>16</sub>	Function Select Register C	PSC	00X0 0000 <sub>2</sub>
03B0 <sub>16</sub>	Function Select Register A0	PS0	00 <sub>16</sub>
03B1 <sub>16</sub>	Function Select Register A1	PS1	00 <sub>16</sub>
03B2 <sub>16</sub>	Function Select Register B0	PSL0	00 <sub>16</sub>
03B3 <sub>16</sub>	Function Select Register B1	PSL1	00 <sub>16</sub>
03B4 <sub>16</sub>	Function Select Register A2	PS2	00X0 0000 <sub>2</sub>
03B5 <sub>16</sub>	Function Select Register A3	PS3	00 <sub>16</sub>
03B6 <sub>16</sub>	Function Select Register B2	PSL2	00X0 0000 <sub>2</sub>
03B7 <sub>16</sub>	Function Select Register B3	PSL3	00 <sub>16</sub>
03B8 <sub>16</sub>			
03B9 <sub>16</sub>	Function Select Register A5	PS5	XXX0 0000 <sub>2</sub>
03BA <sub>16</sub>			
03BB <sub>16</sub>			
03BC <sub>16</sub>			
03BD <sub>16</sub>			
03BE <sub>16</sub>			
03BF <sub>16</sub>			
03C0 <sub>16</sub>	Port P6 Register	P6	XX <sub>16</sub>
03C1 <sub>16</sub>	Port P7 Register	P7	XX <sub>16</sub>
03C2 <sub>16</sub>	Port P6 Direction Register	PD6	00 <sub>16</sub>
03C3 <sub>16</sub>	Port P7 Direction Register	PD7	00 <sub>16</sub>
03C4 <sub>16</sub>	Port P8 Register	P8	XX <sub>16</sub>
03C5 <sub>16</sub>	Port P9 Register	P9	XX <sub>16</sub>
03C6 <sub>16</sub>	Port P8 Direction Register	PD8	00X0 0000 <sub>2</sub>
03C7 <sub>16</sub>	Port P9 Direction Register	PD9	00 <sub>16</sub>
03C8 <sub>16</sub>	Port P10 Register	P10	XX <sub>16</sub>
03C9 <sub>16</sub>	Port P11 Register	P11	XX <sub>16</sub>
03CA <sub>16</sub>	Port P10 Direction Register	PD10	00 <sub>16</sub>
03CB <sub>16</sub>	Port P11 Direction Register	PD11	XXX0 0000 <sub>2</sub>
03CC <sub>16</sub>	Port P12 Register	P12	XX <sub>16</sub>
03CD <sub>16</sub>	Port P13 Register	P13	XX <sub>16</sub>
03CE <sub>16</sub>	Port P12 Direction Register	PD12	00 <sub>16</sub>
03CF <sub>16</sub>	Port P13 Direction Register	PD13	00 <sub>16</sub>

X: Indeterminate

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&lt;144-pin package&gt;

Address	Register	Symbol	Value after RESET
03D0 <sub>16</sub>	Port P14 Register	P14	XX <sub>16</sub>
03D1 <sub>16</sub>	Port P15 Register	P15	XX <sub>16</sub>
03D2 <sub>16</sub>	Port P14 Direction Register	PD14	X000 0000 <sub>2</sub>
03D3 <sub>16</sub>	Port P15 Direction Register	PD15	00 <sub>16</sub>
03D4 <sub>16</sub>			
03D5 <sub>16</sub>			
03D6 <sub>16</sub>			
03D7 <sub>16</sub>			
03D8 <sub>16</sub>			
03D9 <sub>16</sub>			
03DA <sub>16</sub>	Pull-Up Control Register 2	PUR2	00 <sub>16</sub>
03DB <sub>16</sub>	Pull-Up Control Register 3	PUR3	00 <sub>16</sub>
03DC <sub>16</sub>	Pull-Up Control Register 4	PUR4	XXXX 0000 <sub>2</sub>
03DD <sub>16</sub>			
03DE <sub>16</sub>			
03DF <sub>16</sub>			
03E0 <sub>16</sub>	Port P0 Register	P0	XX <sub>16</sub>
03E1 <sub>16</sub>	Port P1 Register	P1	XX <sub>16</sub>
03E2 <sub>16</sub>	Port P0 Direction Register	PD0	00 <sub>16</sub>
03E3 <sub>16</sub>	Port P1 Direction Register	PD1	00 <sub>16</sub>
03E4 <sub>16</sub>	Port P2 Register	P2	XX <sub>16</sub>
03E5 <sub>16</sub>	Port P3 Register	P3	XX <sub>16</sub>
03E6 <sub>16</sub>	Port P2 Direction Register	PD2	00 <sub>16</sub>
03E7 <sub>16</sub>	Port P3 Direction Register	PD3	00 <sub>16</sub>
03E8 <sub>16</sub>	Port P4 Register	P4	XX <sub>16</sub>
03E9 <sub>16</sub>	Port P5 Register	P5	XX <sub>16</sub>
03EA <sub>16</sub>	Port P4 Direction Register	PD4	00 <sub>16</sub>
03EB <sub>16</sub>	Port P5 Direction Register	PD5	00 <sub>16</sub>
03EC <sub>16</sub>			
03ED <sub>16</sub>			
03EE <sub>16</sub>			
03EF <sub>16</sub>			
03F0 <sub>16</sub>	Pull-Up Control Register 0	PUR0	00 <sub>16</sub>
03F1 <sub>16</sub>	Pull-Up Control Register 1	PUR1	XXXX 0000 <sub>2</sub>
03F2 <sub>16</sub>			
03F3 <sub>16</sub>			
03F4 <sub>16</sub>			
03F5 <sub>16</sub>			
03F6 <sub>16</sub>			
03F7 <sub>16</sub>			
03F8 <sub>16</sub>			
03F9 <sub>16</sub>			
03FA <sub>16</sub>			
03FB <sub>16</sub>			
03FC <sub>16</sub>			
03FD <sub>16</sub>			
03FE <sub>16</sub>			
03FF <sub>16</sub>	Port Control Register	PCR	XXXX XXX0 <sub>2</sub>

X: Indeterminate

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&lt;100-pin package&gt;

Address	Register	Symbol	Value after RESET
03A0 <sub>16</sub>			
03A1 <sub>16</sub>			
03A2 <sub>16</sub>			
03A3 <sub>16</sub>			
03A4 <sub>16</sub>			
03A5 <sub>16</sub>			
03A6 <sub>16</sub>			
03A7 <sub>16</sub>	Function Select Register D1	PSD1	X0XX XX00 <sub>2</sub>
03A8 <sub>16</sub>			
03A9 <sub>16</sub>			
03AA <sub>16</sub>			
03AB <sub>16</sub>			
03AC <sub>16</sub>	Function Select Register C2	PSC2	XXXX X00X <sub>2</sub>
03AD <sub>16</sub>	Function Select Register C3	PSC3	X0XX XXXX <sub>2</sub>
03AE <sub>16</sub>			
03AF <sub>16</sub>	Function Select Register C	PSC	00X0 0000 <sub>2</sub>
03B0 <sub>16</sub>	Function Select Register A0	PS0	00 <sub>16</sub>
03B1 <sub>16</sub>	Function Select Register A1	PS1	00 <sub>16</sub>
03B2 <sub>16</sub>	Function Select Register B0	PSL0	00 <sub>16</sub>
03B3 <sub>16</sub>	Function Select Register B1	PSL1	00 <sub>16</sub>
03B4 <sub>16</sub>	Function Select Register A2	PS2	00X0 0000 <sub>2</sub>
03B5 <sub>16</sub>	Function Select Register A3	PS3	00 <sub>16</sub>
03B6 <sub>16</sub>	Function Select Register B2	PSL2	00X0 0000 <sub>2</sub>
03B7 <sub>16</sub>	Function Select Register B3	PSL3	00 <sub>16</sub>
03B8 <sub>16</sub>			
03B9 <sub>16</sub>			
03BA <sub>16</sub>			
03BB <sub>16</sub>			
03BC <sub>16</sub>			
03BD <sub>16</sub>			
03BE <sub>16</sub>			
03BF <sub>16</sub>			
03C0 <sub>16</sub>	Port P6 Register	P6	XX <sub>16</sub>
03C1 <sub>16</sub>	Port P7 Register	P7	XX <sub>16</sub>
03C2 <sub>16</sub>	Port P6 Direction Register	PD6	00 <sub>16</sub>
03C3 <sub>16</sub>	Port P7 Direction Register	PD7	00 <sub>16</sub>
03C4 <sub>16</sub>	Port P8 Register	P8	XX <sub>16</sub>
03C5 <sub>16</sub>	Port P9 Register	P9	XX <sub>16</sub>
03C6 <sub>16</sub>	Port P8 Direction Register	PD8	00X0 0000 <sub>2</sub>
03C7 <sub>16</sub>	Port P9 Direction Register	PD9	00 <sub>16</sub>
03C8 <sub>16</sub>	Port P10 Register	P10	XX <sub>16</sub>
03C9 <sub>16</sub>			
03CA <sub>16</sub>	Port P10 Direction Register	PD10	00 <sub>16</sub>
03CB <sub>16</sub>	Set default value to "FF <sub>16</sub> "		
03CC <sub>16</sub>			
03CD <sub>16</sub>			
03CE <sub>16</sub>	Set default value to "FF <sub>16</sub> "		
03CF <sub>16</sub>	Set default value to "FF <sub>16</sub> "		

X: Indeterminate

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&lt;100-pin package&gt;

Address	Register	Symbol	Value after RESET
03D0 <sub>16</sub>			
03D1 <sub>16</sub>			
03D2 <sub>16</sub>	Set default value to "FF <sub>16</sub> "		
03D3 <sub>16</sub>	Set default value to "FF <sub>16</sub> "		
03D4 <sub>16</sub>			
03D5 <sub>16</sub>			
03D6 <sub>16</sub>			
03D7 <sub>16</sub>			
03D8 <sub>16</sub>			
03D9 <sub>16</sub>			
03DA <sub>16</sub>	Pull-Up Control Register 2	PUR2	00 <sub>16</sub>
03DB <sub>16</sub>	Pull-Up Control Register 3	PUR3	00 <sub>16</sub>
03DC <sub>16</sub>	Set default value to "00 <sub>16</sub> "		
03DD <sub>16</sub>			
03DE <sub>16</sub>			
03DF <sub>16</sub>			
03E0 <sub>16</sub>	Port P0 Register	P0	XX <sub>16</sub>
03E1 <sub>16</sub>	Port P1 Register	P1	XX <sub>16</sub>
03E2 <sub>16</sub>	Port P0 Direction Register	PD0	00 <sub>16</sub>
03E3 <sub>16</sub>	Port P1 Direction Register	PD1	00 <sub>16</sub>
03E4 <sub>16</sub>	Port P2 Register	P2	XX <sub>16</sub>
03E5 <sub>16</sub>	Port P3 Register	P3	XX <sub>16</sub>
03E6 <sub>16</sub>	Port P2 Direction Register	PD2	00 <sub>16</sub>
03E7 <sub>16</sub>	Port P3 Direction Register	PD3	00 <sub>16</sub>
03E8 <sub>16</sub>	Port P4 Register	P4	XX <sub>16</sub>
03E9 <sub>16</sub>	Port P5 Register	P5	XX <sub>16</sub>
03EA <sub>16</sub>	Port P4 Direction Register	PD4	00 <sub>16</sub>
03EB <sub>16</sub>	Port P5 Direction Register	PD5	00 <sub>16</sub>
03EC <sub>16</sub>			
03ED <sub>16</sub>			
03EE <sub>16</sub>			
03EF <sub>16</sub>			
03F0 <sub>16</sub>	Pull-up Control Register 0	PUR0	00 <sub>16</sub>
03F1 <sub>16</sub>	Pull-up Control Register 1	PUR1	XXXX 0000 <sub>2</sub>
03F2 <sub>16</sub>			
03F3 <sub>16</sub>			
03F4 <sub>16</sub>			
03F5 <sub>16</sub>			
03F6 <sub>16</sub>			
03F7 <sub>16</sub>			
03F8 <sub>16</sub>			
03F9 <sub>16</sub>			
03FA <sub>16</sub>			
03FB <sub>16</sub>			
03FC <sub>16</sub>			
03FD <sub>16</sub>			
03FE <sub>16</sub>			
03FF <sub>16</sub>	Port Control Register	PCR	XXXX XXX0 <sub>2</sub>

X: Indeterminate

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## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter		Condition	Value	Unit	
V <sub>CC</sub>	Supply Voltage		V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.0	V	
AV <sub>CC</sub>	Analog Supply Voltage		V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.0	V	
V <sub>I</sub>	Input Voltage	RESET, CNV <sub>SS</sub> , BYTE, P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , V <sub>REF</sub> , X <sub>IN</sub>		-0.3 to V <sub>CC</sub> +0.3	V	
		P70, P71		-0.3 to 6.0		
V <sub>O</sub>	Output Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>OUT</sub>		-0.3 to V <sub>CC</sub> +0.3	V	
		P70, P71		-0.3 to 6.0		
P <sub>d</sub>	Power Dissipation		T version	T <sub>opr</sub> =25° C	500	mW
			U version		400	
T <sub>opr</sub>	Operating Ambient Temperature	during CPU operation	T version		-40 to 85	° C
			U version		-40 to 105	
		during flash memory program and erase operation	0 to 60			
T <sub>stg</sub>	Storage Temperature				-65 to 150	° C

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

**Table 5.2 Recommended Operating Conditions**  
**(V<sub>CC</sub>=4.2 to 5.5V, V<sub>SS</sub>=0V at T<sub>opr</sub> = -40 to 85°C (T version)/-40 to 105°C (U version)**  
**unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Supply Voltage		4.2	5.0	5.5	V
AV <sub>CC</sub>	Analog Supply Voltage			V <sub>CC</sub>		V
V <sub>SS</sub>	Supply Voltage			0		V
AV <sub>SS</sub>	Analog Supply Voltage			0		V
V <sub>IH</sub>	Input High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 <sup>(3)</sup> , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137 <sup>(4)</sup> , P140-P146, P150-P157 <sup>(4)</sup> , X <sub>IN</sub> , $\overline{\text{RESET}}$ , CNV <sub>SS</sub> , BYTE P70, P71	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
			0.8V <sub>CC</sub>		6.0	
V <sub>IL</sub>	Input Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 <sup>(3)</sup> , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137 <sup>(4)</sup> , P140-P146, P150-P157 <sup>(4)</sup> , X <sub>IN</sub> , $\overline{\text{RESET}}$ , CNV <sub>SS</sub> , BYTE	0		0.2V <sub>CC</sub>	V
I <sub>OH(peak)</sub>	Peak Output High ("H") Current <sup>(2)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup>			-10.0	mA
I <sub>OH(avg)</sub>	Average Output High ("H") Current <sup>(1)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup>			-5.0	mA
I <sub>OL(peak)</sub>	Peak Output Low ("L") Current <sup>(2)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup>			10.0	mA
I <sub>OL(avg)</sub>	Average Output Low ("L") Current <sup>(1)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup>			5.0	mA

## NOTES:

- Typical values when average output current is 100 ms.
- Total I<sub>OL(peak)</sub> for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80 mA or less.  
 Total I<sub>OL(peak)</sub> for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80 mA or less.  
 Total I<sub>OH(peak)</sub> for P0, P1, P2, and P11 must be -40mA or less.  
 Total I<sub>OH(peak)</sub> for P86, P87, P9, P10, P14 and P15 must be -40 mA or less.  
 Total I<sub>OH(peak)</sub> for P3, P4, P5, P12 and P13 must be -40 mA or less.  
 Total I<sub>OH(peak)</sub> for P6, P7, and P80 to P84 must be -40 mA or less.
- V<sub>IH</sub> and V<sub>IL</sub> reference for P87 applies when P87 is used as a programmable input port.  
 It does not apply when P87 is used as X<sub>CIN</sub>.
- Ports P11 to P15 are provided in the 144-pin package only.

**Table 5.3 Recommended Operating Conditions (Continued)**  
**(V<sub>CC</sub>=4.2 to 5.5V, V<sub>SS</sub>=0V at T<sub>opr</sub> = -40 to 85°C (T version)/-40 to 105°C (U version)**  
**unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(BCLK)	CPU Operation Frequency	V <sub>CC</sub> =4.2 to 5.5 V	0		32	MHz
f(XIN)	Main Clock Input Frequency	V <sub>CC</sub> =4.2 to 5.5 V	0		24	MHz
f(XCIN)	Sub Clock Frequency			32.768	50	kHz
f(Ring)	On-chip Oscillator Frequency (V <sub>CC</sub> =5.0V, T <sub>opr</sub> =25° C)		0.5	1	2	MHz
f(PLL)	PLL Clock Frequency	V <sub>CC</sub> =4.2 to 5.5 V	10		32	MHz
tsu(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer	V <sub>CC</sub> =5.0 V			5	ms

V<sub>CC</sub>=5V**Table 5.4 Electrical Characteristics**

(V<sub>CC</sub>=4.2 to 5.5V, V<sub>SS</sub>=0V at T<sub>opr</sub> = -40 to 85°C (T version)/-40 to 105°C (U version),  
f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V <sub>OH</sub>	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	I <sub>OH</sub> =-5 mA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	I <sub>OH</sub> =-200 μA	V <sub>CC</sub> -0.3		V <sub>CC</sub>	V
		X <sub>OUT</sub>	I <sub>OH</sub> =-1 mA	3.0			V
		X <sub>COUT</sub>	High Power	No load applied		2.5	
		Low Power	No load applied		1.6		
V <sub>OL</sub>	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	I <sub>OL</sub> =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	I <sub>OL</sub> =200 μA			0.45	V
		X <sub>OUT</sub>	I <sub>OL</sub> =1 mA			2.0	V
		X <sub>COUT</sub>	High Power	No load applied		0	
		Low Power	No load applied		0		
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I <sub>IH</sub>	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	V <sub>I</sub> =5 V			5.0	μA
I <sub>IL</sub>	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	V <sub>I</sub> =0 V			-5.0	μA
R <sub>PULLUP</sub>	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	V <sub>I</sub> =0 V	30	50	167	kΩ
R <sub>fXIN</sub>	Feedback Resistance	X <sub>IN</sub>			1.5		MΩ
R <sub>fXCIN</sub>	Feedback Resistance	X <sub>CIN</sub>			10		MΩ
V <sub>RAM</sub>	RAM Standby Voltage	In stop mode		2.0			V

NOTE:

1. Ports P11 to P15 are provided in the 144-pin package only.



VCC=5V

**Table 5.4 Electrical Characteristics (Continued)**

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version),  
f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to Vss.	f(BCLK)=32 MHz, Square wave, No division		28	50	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM		430		μA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM <sup>(1)</sup>		25		μA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		μA
			While clock stops, Topr=25° C		0.8	5	μA
			While clock stops, Topr=85° C			50	μA
			While clock stops, Topr=105° C			100	μA
While clock stops, Topr=125° C			200	μA			

NOTE:

1. Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

VCC=5V

**Table 5.5 A/D Conversion Characteristics**

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version),  
f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	VREF=VCC				10	Bits
INL	Integral Nonlinearity Error	VREF=VCC=5V	AN0 to AN7, AN00 to AN07, AN20 to AN27, AN150 to AN157, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
RLADDER	Resistor Ladder	VREF=VCC		8		40	kΩ
tCONV	10-bit Conversion Time <sup>(1, 2)</sup>			2.06			μs
tCONV	8-bit Conversion Time <sup>(1, 2)</sup>			1.75			μs
tsAMP	Sampling Time <sup>(1)</sup>			0.188			μs
VREF	Reference Voltage			2		VCC	V
VIA	Analog Input Voltage			0		VREF	V

## NOTES:

1. Divide f(XIN), if exceeding 16 MHz, to keep φAD frequency at 16 MHz or less.
2. With using the sample and hold function.

**Table 5.6 D/A Conversion Characteristics**

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version),  
f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution					8	Bits
-	Absolute Accuracy					1.0	%
tsU	Setup Time					3	μs
Ro	Output Resistance			4	10	20	kΩ
IvREF	Reference Power Supply Input Current	(Note 1)				1.5	mA

## NOTE:

1. Measurement when using one D/A converter. The DAI register (i=0, 1) of the D/A converter, not being used, is set to "0016". The resistor ladder in the A/D converter is excluded.  
IvREF flows even if the VCUT bit in the ADOCON1 register is set to "0" (no VREF connection).

**Table 5.7 Flash Memory Version Electrical Characteristics**  
 (VCC=4.5 to 5.5V at Topr= 0 to 60°C unless otherwise specified)

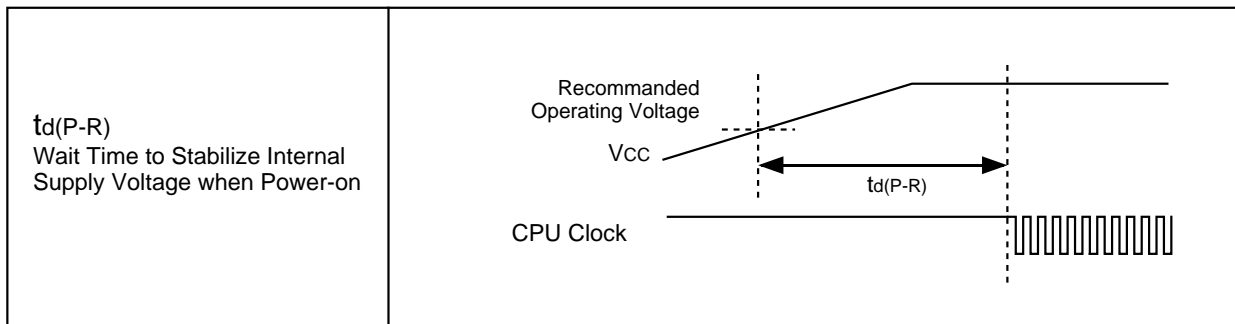
Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance <sup>(2)</sup>		100			cycles
-	Word Program Time (Vcc=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (Vcc=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time <sup>(1)</sup>				4 x n	s
tps	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (Topr=-40 to 85 ° C)		10			years

NOTES:

1. *n* denotes the number of block to be erased.
2. Number of program-erase cycles per block.  
 If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles.  
 For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

**Table 5.8 Power Supply Timing**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	Vcc=4.2 to 5.5V			2	ms



**Figure 5.1 Power Supply Timing Diagram**

VCC=5V

**Timing Requirements**

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

**Table 5.9 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
tw(H)	External Clock Input High ("H") Width	13.75		ns
tw(L)	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

**Timing Requirements**

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

**Table 5.10 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	100		ns
tw(TAH)	TAiIN Input High ("H") Width	40		ns
tw(TAL)	TAiIN Input Low ("L") Width	40		ns

**Table 5.11 Timer A Input (Gate Input in Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	400		ns
tw(TAH)	TAiIN Input High ("H") Width	200		ns
tw(TAL)	TAiIN Input Low ("L") Width	200		ns

**Table 5.12 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	200		ns
tw(TAH)	TAiIN Input High ("H") Width	100		ns
tw(TAL)	TAiIN Input Low ("L") Width	100		ns

**Table 5.13 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN Input High ("H") Width	100		ns
tw(TAL)	TAiIN Input Low ("L") Width	100		ns

**Table 5.14 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT Input Cycle Time	2000		ns
tw(UPH)	TAiOUT Input High ("H") Width	1000		ns
tw(UPL)	TAiOUT Input Low ("L") Width	1000		ns
tsu(UP-TIN)	TAiOUT Input Setup Time	400		ns
th(TIN-UP)	TAiOUT Input Hold Time	400		ns

**Timing Requirements**

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

**Table 5.15 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN Input Cycle Time (counted on one edge)	100		ns
tw(TBH)	TBiIN Input High ("H") Width (counted on one edge)	40		ns
tw(TBL)	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
tc(TB)	TBiIN Input Cycle Time (counted on both edges)	200		ns
tw(TBH)	TBiIN Input High ("H") Width (counted on both edges)	80		ns
tw(TBL)	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

**Table 5.16 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN Input Cycle Time	400		ns
tw(TBH)	TBiIN Input High ("H") Width	200		ns
tw(TBL)	TBiIN Input Low ("L") Width	200		ns

**Table 5.17 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN Input Cycle Time	400		ns
tw(TBH)	TBiIN Input High ("H") Width	200		ns
tw(TBL)	TBiIN Input Low ("L") Width	200		ns

**Table 5.18 A/D Trigger Input**

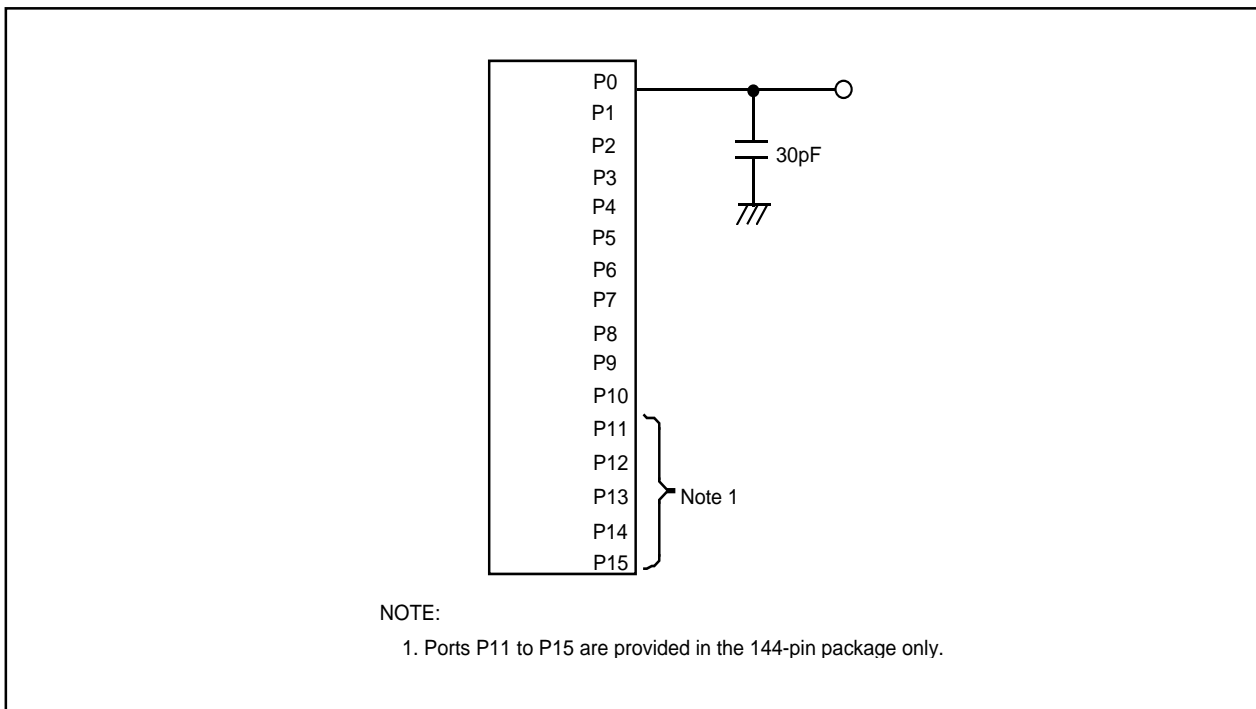
Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	ADTRG Input Cycle Time (required for trigger)	1000		ns
tw(ADL)	ADTRG Input Low ("L") Pulse Width	125		ns

**Table 5.19 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi Input Cycle Time	200		ns
tw(CKH)	CLKi Input High ("H") Width	100		ns
tw(CKL)	CLKi Input Low ("L") Width	100		ns
td(C-Q)	TxDi Output Delay Time		80	ns
th(C-Q)	TxDi Hold Time	0		ns
tsu(D-C)	RxDi Input Setup Time	30		ns
th(C-Q)	RxDi Input Hold Time	90		ns

**Table 5.20 External Interrupt INTi Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	INTi Input High ("H") Width	250		ns
tw(INL)	INTi Input Low ("L") Width	250		ns

**Figure 5.2 P0 to P15 Measurement Circuit**

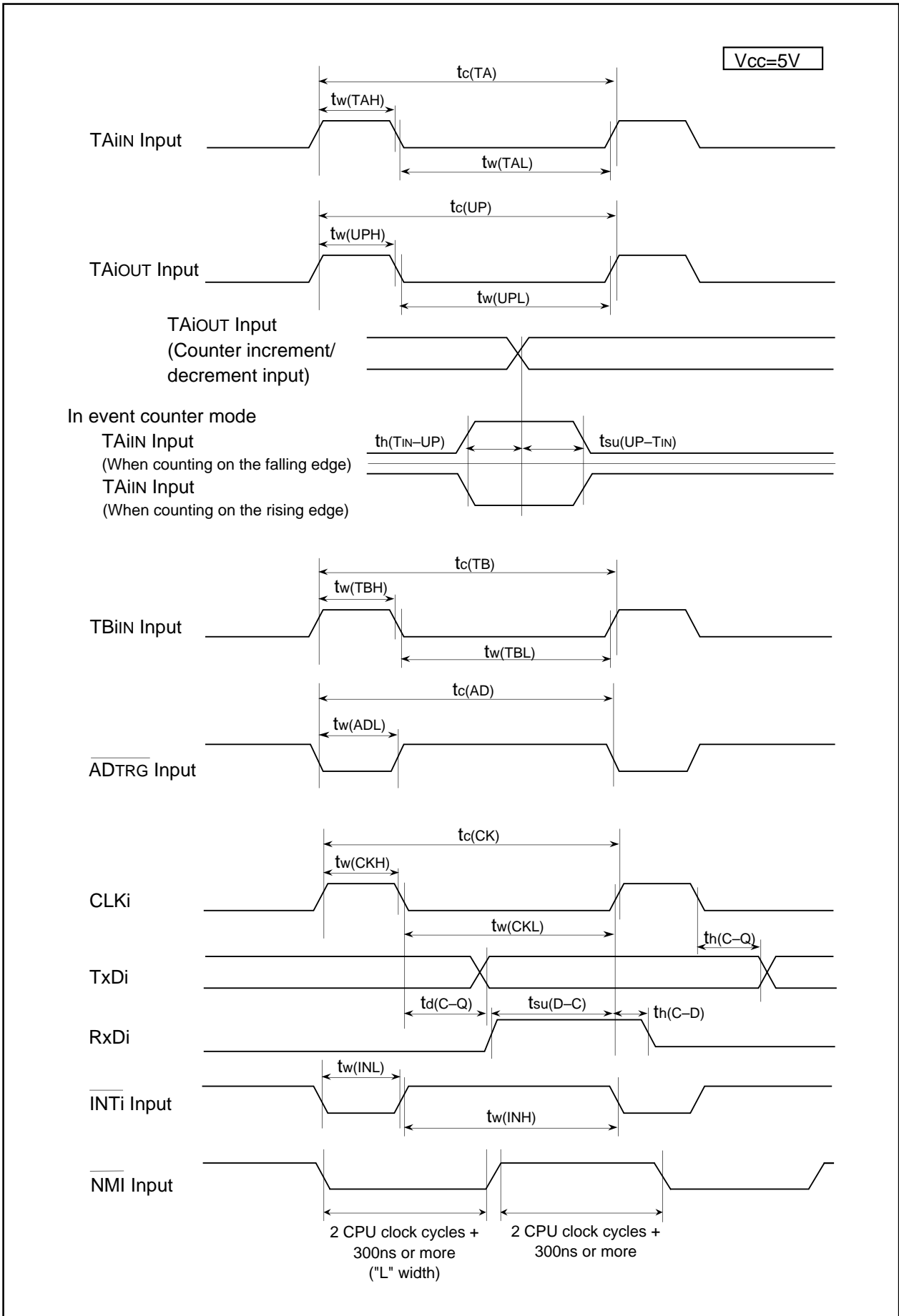
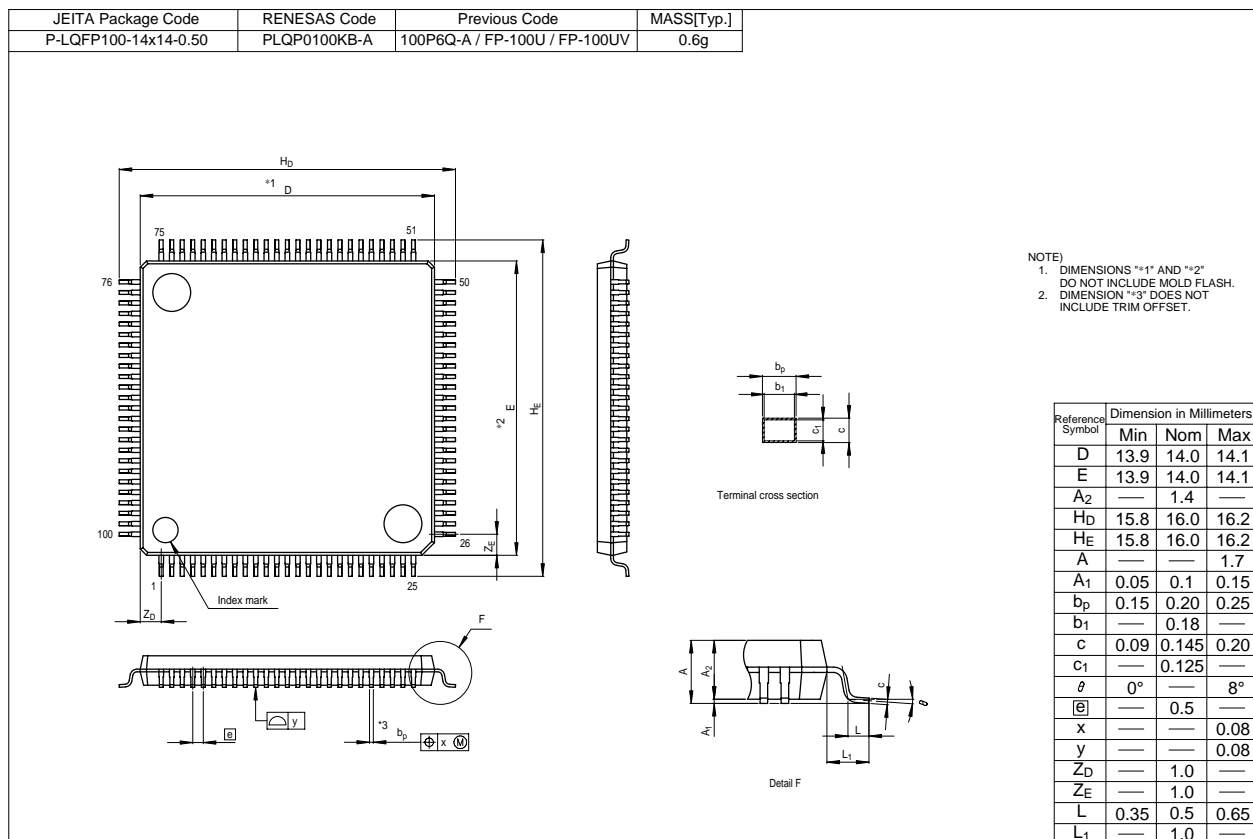
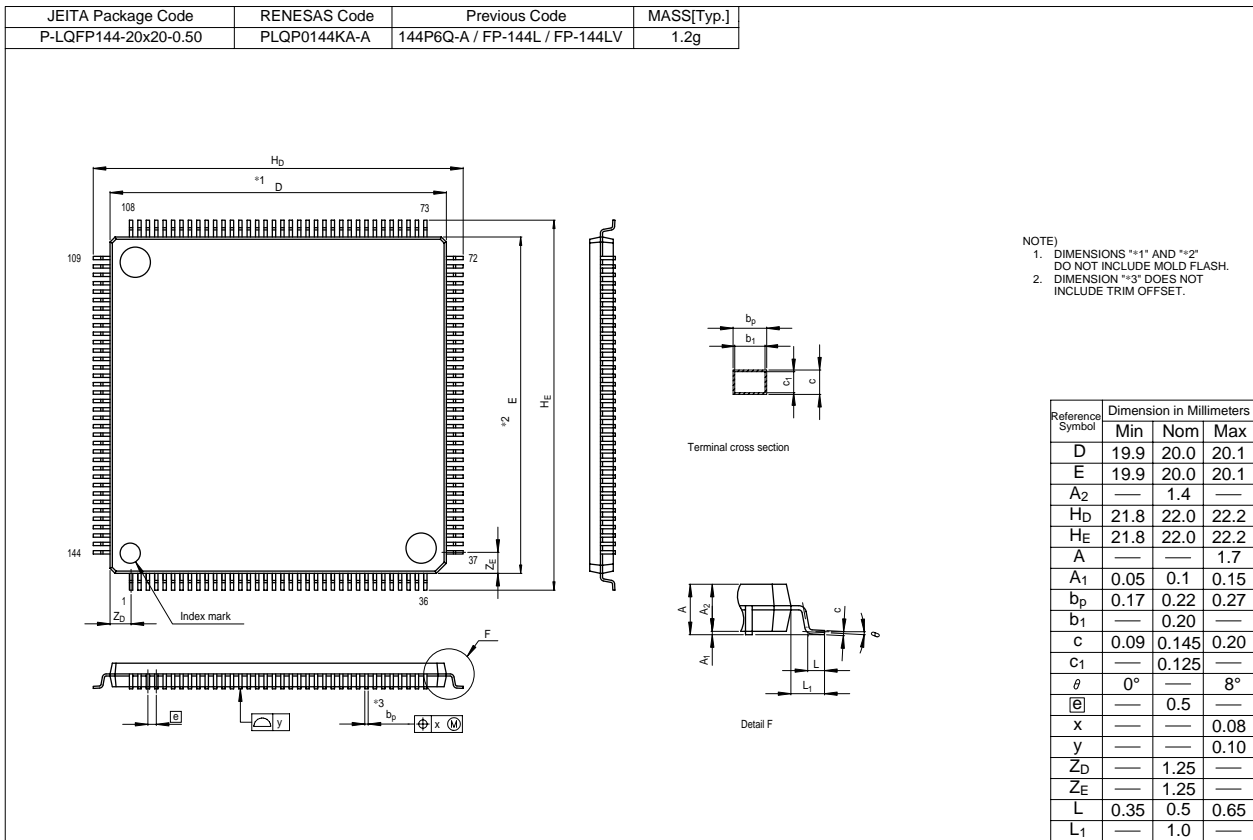


Figure 5.3 Vcc=5V Timing Diagram



# Package Dimensions





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