Section I. Stratix IV Device Datasheet

This section includes the following chapters:

- Chapter 1, DC and Switching Characteristics

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

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Electrical Characteristics

This chapter covers the electrical characteristics for Stratix IV devices.

Operating Conditions

When Stratix® IV devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix IV devices, system designers must consider the following operating requirements. Stratix IV devices are offered in both commercial and industrial grades. Commercial devices are offered in -2 (fastest), -2x, -3, and -4 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix IV devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions.

Conditions beyond those listed in Table 1–1 and Table 1–2 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. Stratix IV Device Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	-0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	-0.5	2.25	V
V_{CCPGM}	Configuration pins power supply	-0.5	3.75	V
V_{CCAUX}	Auxiliary supply for the programmable power technology	-0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_{CCPD}	I/O pre-driver power supply	-0.5	3.75	V
V_{CCIO}	I/O power supply	-0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply	-0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	-0.5	1.35	V
V_{CCA_PLL}	PLL analog power supply	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
T_J	Operating junction temperature	-40	100	C
T_{STG}	Storage temperature (No bias)	-65	150	C

Table 1–2. Stratix IV GX Transceiver Power Supply Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	—	3.15 / 2.625	V
V_{CCA_R}	Transceiver high voltage power (right side)	—	3.15 / 2.625	
V_{CCHIP_L}	Transceiver HIP digital power (left side)	—	0.99	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	—	0.99	
V_{CCR_L}	Receiver power (left side)	—	1.21	V
V_{CCR_R}	Receiver power (right side)	—	1.21	
V_{CCT_L}	Transmitter power (left side)	—	1.21	V
V_{CCT_R}	Transmitter power (right side)	—	1.21	
V_{CCL_GXBLn} *(2)*	Transceiver clock power (left side)	—	1.21	V
V_{CCL_GXBRn} *(2)*	Transceiver clock power (right side)	—	1.21	V
V_{CCH_GXBLn} *(2)*	Transmitter output buffer power (left side)	—	1.54 / 1.65	V
V_{CCH_GXBRn} *(2)*	Transmitter output buffer power (right side)	—	1.54 / 1.65	V

Note to Table 1–2:

(1) n=0, 1, 2, 3

Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–3 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–3 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 5/10ths of a year.

Table 1–3. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	4.0 V	100.000	%
		4.05 V	79.330	%
		4.1 V	46.270	%
		4.15 V	27.030	%
		4.2 V	15.800	%
		4.25 V	9.240	%
		4.3 V	5.410	%
		4.35 V	3.160	%
		4.4 V	1.850	%
		4.45 V	1.080	%
		4.5 V	0.630	%
		4.55 V	0.370	%
		4.6 V	0.220	%

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Stratix IV devices. The steady-state voltage and current values expected from Stratix IV devices are provided in Table 1–4. All supplies must be strictly monotonic, without plateaus.

Table 1–4. Stratix IV Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	—	0.87	0.90	0.93	V
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CCAUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD}	I/O pre-driver (3.0 V) power supply	—	2.85	3	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0-V) power supply	—	2.85	3	3.15	V
	I/O buffers (2.5-V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8-V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5-V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.2-V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0-V) power supply	—	2.85	3	3.15	V
	Configuration pins (2.5-V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8-V) power supply	—	1.71	1.8	1.89	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_PLL}	PLL digital voltage regulator power supply	—	0.87	0.90	0.93	V

Table 1–4. Stratix IV Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC_CLKIN}	Differential clock input power supply	—	2.375	2.5	2.625	V
V_{CCBAT}	Battery back-up power supply (For design security volatile key register)	—	1.2	3.0	3.3	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	C
		Industrial	–40	—	100	C
t_{RAMP}	Power supply ramp time	Normal POR	0.05	—	100	ms
		Fast POR *(1)*	0.05	—	12	ms

Note to Table 1–4:

(1) If the PORSEL pin is connected to V_{CC}, all supplies must ramp up within 12 ms.

Table 1–5 shows the transceiver power supply recommended operating conditions.

Table 1–5. Stratix IV GX Transceiver Power Supply Recommended Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	2.85/2.375	3.0/2.5	3.15/2.625	V
V_{CCA_R}	Transceiver high voltage power (right side)				
V_{CCHIP_L} *(1)*	Transceiver HIP digital power (left side)	0.855	0.9	0.945	V
V_{CCHIP_R} *(1)*	Transceiver HIP digital power (right side)				
V_{CCR_L}	Receiver power (left side)	1.045	1.1	1.155	V
V_{CCR_R}	Receiver power (right side)				
V_{CCT_L}	Transmitter power (left side)	1.045	1.1	1.155	V
V_{CCT_R}	Transmitter power (right side)				
V_{CCL_GXBLn} *(2)*	Transceiver clock power (left side)	1.045	1.1	1.155	V
V_{CCL_GXBRn} *(2)*	Transceiver clock power (right side)				V
V_{CCH_GXBLn} *(2)*	Transmitter output buffer power (left side)	1.33/1.425	1.4/1.5	1.47/1.575	V
V_{CCH_GXBRn} *(2)*	Transmitter output buffer power (right side)				V

Note to Table 1–5:

(1) If V_{CCHIP_L} is connected to the same power supply source as V_{CC}, the tighter V_{CC} recommended operating conditions need to be met.
(2) n=0, 1, 2, 3

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current the device draws after the device is configured, with no inputs or outputs toggling and no activity in the device. Since these currents vary largely with resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–6 lists supply current specifications for V_{CC_CLKIN}, V_{CCPGM}, and V_{CCAUX}. Use the EPE to get supply current estimates for remaining power supplies.

Table 1–6. Supply Current Specifications for V_{CC_CLKIN}, V_{CCPGM}, and V_{CCAUX}

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	250	mA
I_{PGM}	V_{CCPGM} current specifications	0	250	mA
I_{AUX}	V_{CCAUX} current specification	0	250	mA

I/O Pin Leakage Current

Table 1–7 defines the Stratix IV I/O pin leakage current specifications.

Table 1–7. Stratix IV I/O Pin Leakage Current

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0V to $V_{CCIOMAX}$	-10	—	10	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0V to $V_{CCIOMAX}$	-10	—	10	µA

On-Chip Termination (OCT) Specifications

Table 1–8 lists the Stratix IV series and parallel OCT calibration accuracy.

Table 1–8. On-Chip Termination With Calibration Specification for I/Os - Preliminary

Symbol	Description	Conditions	Calibration Accuracy	Unit
			Commercial	
25-Ω R_S 3.0/2.5	25-Ω series termination	V_{CCIO} = 3.0/2.5 V	± 5	%
50-Ω R_S 3.0/2.5	50-Ω series termination	V_{CCIO} = 3.0/2.5 V	± 5	%
50-Ω R_T 2.5	50-Ω parallel termination	V_{CCIO} = 2.5 V	± 10	%
25-Ω R_S 1.8	25-Ω series termination	V_{CCIO} = 1.8 V	± 5	%
50-Ω R_S 1.8	50-Ω series termination	V_{CCIO} = 1.8 V	± 5	%
50-Ω R_T 1.8	50-Ω parallel termination	V_{CCIO} = 1.8 V	± 10	%
50-Ω R_S 1.5	50-Ω series termination	V_{CCIO} = 1.5 V	± 8	%
50-Ω R_T 1.5	50-Ω parallel termination	V_{CCIO} = 1.5 V	± 10	%
50-Ω R_S 1.2	50-Ω series termination	V_{CCIO} = 1.2 V	± 8	%
50-Ω R_T 1.2	50-Ω series termination	V_{CCIO} = 1.2 V	± 10	%

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When PVT conditions change after calibration, the tolerance may change. Table 1–9 lists the Stratix IV OCT resistance tolerance to PVT changes.

Table 1–9. I/O On-Chip Termination Resistance Tolerance - Preliminary

Symbol	Description	Resistance Tolerance	
		Commercial	Unit
R_{OCT_UNCAL}	Internal series/parallel OCT with calibration	± 5	%
R_{OCT_CAL}	Internal series/parallel OCT without calibration	± 30	%

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 1–10 lists OCT variation with temperature and voltage after power-up calibration. Use Equation 1–1 to determine the OCT variation when voltage and temperature vary after power-up calibration.

Equation 1–1. OCT Variation Without Re-Calibration *(Note 1)*

$$R_{OCT} = R_{CAL}\left(1 + \frac{dR}{dT} \times \Delta T + \frac{dR}{dV} \times \Delta V\right)$$

Note to Equation 1–1:

(1) R_{CAL} is calibrated on-chip termination at power up. ΔT and ΔV are variations in temperature and voltage with respect to temperature and V_{CCIO} values, respectively, at power up.

Table 1–10. On-Chip Termination Variation after Power-Up Calibration - Preliminary

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Industrial Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.029	—	Ω/V
		2.5	0.036	—	
		1.8	0.033	—	
		1.5	0.033	—	
		1.2	0.033	—	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.294	—	Ω/C
		2.5	0.301	—	
		1.8	0.355	—	
		1.5	0.344	—	
		1.2	0.348	—	

Pin Capacitance

Table 1–11 shows the Stratix IV device family pin capacitance.

Table 1–11. Stratix IV Device Capacitance *(Note 1)* - Preliminary (Part 1 of 2)

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	8	pF
C_{IOLR}	Input capacitance on left/right I/O pins	8	pF
C_{CLKTB}	Input capacitance on top/bottom dedicated clock input pins	5	pF
C_{CLKLR}	Input capacitance on left/right dedicated clock input pins	5	pF

Table 1–11. Stratix IV Device Capacitance *(Note 1)* - Preliminary (Part 2 of 2)

Symbol	Description	Typical	Unit
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	8	pF

Note to Table 1–11:

(1) Pending silicon characterization.

Hot Socketing

Table 1–12 defines the hot socketing specification for Stratix IV devices.

Table 1–12. Stratix IV Hot Socketing Specifications - Preliminary

Symbol	Description	Maximum
$I_{IIOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA for Trise > 10 ns

I/O Standard Specifications

Table 1–13 through Table 1–18 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix IV devices. These tables also show the Stratix IV device family I/O standard specifications. Refer to the "Glossary" on page 1–34 for an explanation of terms used in Table 1–13 through Table 1–18. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

Table 1–13. Single-Ended I/O Standards

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	V_{CCIO} + 0.3	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} - 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	V_{CCIO} + 0.3	0.2	2.1	0.1	-0.1
								0.4	2	1	-1
								0.7	1.7	2	-2
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} -0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	-	0.3 * V_{CCIO}	0.5 * V_{CCIO}	3.6	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	-	0.35 * V_{CCIO}	0.5 * V_{CCIO}	-	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5

Table 1–14. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 * V_{CCIO}	0.5 * V_{CCIO}	0.52 * V_{CCIO}	—	V_{CCIO}/2	—

Table 1–15. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$(V)		$V_{IH(DC)}$(V)		$V_{IL(AC)}$(V)	$V_{IH(AC)}$(V)	V_{OL}(V)	V_{OH}(V)		
	Min	Max	Min	Max	Max	Min	Max	Min	I_{ol} (mA)	I_{oh} (mA)
SSTL-2 Class I	-0.3	V_{REF} - 0.15	V_{REF}+ 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF}+ 0.31	V_{TT} - 0.57	V_{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	-0.3	V_{REF} - 0.15	V_{REF}+ 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF}+ 0.31	V_{TT} - 0.76	V_{TT} + 0.76	16.2	-16.2
SSTL-18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	V_{TT} - 0.475	V_{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	-13.4
SSTL-15 Class I	-0.3	V_{REF} -0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	-8
SSTL-15 Class II	-0.3	V_{REF} -0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	-16
HSTL-18 Class I	-0.3	V_{REF} -0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	8	-8
HSTL-18 Class II	-0.3	V_{REF} -0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	16	-16
HSTL-15 Class I	-0.3	V_{REF} -0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	8	-8
HSTL-15 Class II	-0.3	V_{REF} -0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	16	-16
HSTL-12 Class I	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF}+ 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	-8
HSTL-12 Class II	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF}+ 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	-16

Table 1–16. Differential SSTL I/O Standards

I/O Standard	V_{CCIO}(V)			$V_{CSWING(DC)}$(V)		$V_{X(AC)}$(V)			$V_{SWING(AC)}$(V)		$V_{OX(AC)}$(V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.2	—	V_{CCIO}/2 + 0.2	0.6	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	V_{CCIO}/2	—	0.4	—	—	V_{CCIO}/2	—

Table 1–17. Differential HSTL I/O Standards

I/O Standard	V_{CCIO}(V)			$V_{DIF(DC)}$(V)		$V_{X(AC)}$(V)			$V_{CM(DC)}$(V)			$V_{DIF(AC)}$(V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.8	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.7	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.2	—	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	—

Table 1–18. Differential I/O Standard Specifications (Part 1 of 2) *(Note 1)*, *(2)*

I/O Standard	V_{CCIO}(V)			V_{ID}(mV)			$V_{ICM(DC)}$(V)			V_{OD}(V) *(3)*			V_{OCM}(V) *(3)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5V LVDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.05	D_{max} <= 700Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D_{max} > 700Mbps	1.55	—	—	—	—	—	—
2.5V LVDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.05	D_{max} <= 700Mbps	1.8	0.247	-	0.6	1	1.25	1.5
						—	1.05	D_{max} > 700Mbps	1.55	—	—	—	—	—	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.5

Table 1–18. Differential I/O Standard Specifications (Part 2 of 2) *(Note 1)*, *(2)*

I/O Standard	V_{CCIO}(V)			V_{ID}(mV)			$V_{ICM(DC)}$(V)			V_{OD}(V) *(3)*			V_{OCM}(V) *(3)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (VIO) *(4)*	2.375	2.5	2.625	300	—	—	0.6	D_{max} <= 700Mbps	1.8 *(5)*	—	—	—	—	—	—
	—	—	—	—	—	—	0.6	D_{max} > 700Mbps	1.6 *(5)*	—	—	—	—	—	—

Notes to *Table 1–18:*

(1) VIO (vertical I/O) is top and bottom I/Os; HIO (horizontal I/O) is left and right I/Os.

(2) 1.4V/1.5V PCML transceiver I/O standard specifications are described in the section "Transceiver Performance Specifications" on page 1–10.

(3) RL range: 90 <= RL <= 110 Ω

(4) LVPECL specifications apply only to CLK input pins on column I/Os.

(5) For D_{MAX} > 700 Mbps, the minimum input voltage is 0.85 V; the maximum input voltage is 1.75 V. For F_{MAX} <=700Mbps, the minimum input voltage is 0.45 V; the maximum input voltage is 1.95 V.

Power Consumption

Altera® offers two ways to estimate power consumption for a design: the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide for Stratix III and Stratix IV FPGAs* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Stratix IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary and Final. Preliminary characteristics are created using simulation results, process data, and other known parameters. Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. The upper-right hand corner of a table shows the designation as "Preliminary" or "Final".

Transceiver Performance Specifications

This sections describes transceiver performance specifications.

Table 1–19 lists Stratix IV GX transceiver specifications.

Table 1–19. Stratix IV GX Transceiver Specification (Part 1 of 4)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Commercial/Industrial and -2x Commercial Speed Grade *(1)*			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Input frequency from REFCLK input pins	—	50	—	637.5	50	—	637.5	50	—	622.08	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	425	50	—	325	50	—	325	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a REFCLK pin	—	-0.3	—	—	-0.3	—	—	-0.3	—	—	V
Rise/fall time	—	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCI Express	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCI Express	—	0 to -0.5%	—	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1100	—	—	1100	—	—	1100	—	mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCI Express reference clock	250	—	550	250	—	550	250	—	550	mV
R_{REF}	— —	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCI Express Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	—

Table 1–19. Stratix IV GX Transceiver Specification (Part 2 of 4)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Commercial/Industrial and -2x Commercial Speed Grade *(1)*			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs
Receiver											
Data rate	—	600	—	8500	600	—	6500	600	—	5000	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	V
	V_{ICM} =1 .1 V setting *(4)*	—	—	1.6	—	—	1.6	—	—	1.6	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	Data Rate = 600 Mbps to 5 Gbps.	100	—	—	100	—	—	165	—	—	mV
	Data Rate > 5Gbps.	165	—	—	165	—	—	—	—	—	mV
V_{ICM}	V_{ICM} = 0.82 V setting	—	820	—	—	820	—	—	820	—	mV
	V_{ICM} =1 .1 V setting *(4)*	—	1100	—	—	1100	—	—	1100	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: -10dB									
	XAUI	100 MHz to 2.5 GHz: -10dB									
	(OIF) CEI	100 MHz to 4.875 GHz: -8dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope									
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: -6dB									
	XAUI	100 MHz to 2.5 GHz: -6dB									
	(OIF) CEI	100 MHz to 4.875 GHz: -6dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope									

Table 1–19. Stratix IV GX Transceiver Specification (Part 3 of 4)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Commercial/Industrial and -2x Commercial Speed Grade *(1)*			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable PPM detector *(5)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000									ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	—	—	—	16	—	—	16	—	—	16	dB
Signal detect/loss threshold	PCI Express (PIPE) Mode	65	—	175	65	—	175	65	—	175	mV
CDR LTR time *(6)*	—	—	—	75	—	—	75	—	—	75	µs
CDR minimum T1b *(7)*	—	15	—		15	—	—	15	—	—	µs
LTD lock time *(8)*	—	0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from `rx_freqlocked` *(9)*	—	—	—	4000	—	—	4000	—	—	4000	ns
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 3	—	9	—	—	9	—	—	9	—	dB
	DC Gain Setting = 4	—	12	—	—	12	—	—	12	—	dB
Transmitter											
Data rate	—	600	—	8500	600	—	6500	600	—	5000	Mbps
V_{OCM}	0.65 V setting —	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: -10dB									
	XAUI	312 MHz to 625 MHz: -10dB 625 MHz to 3.125 GHz: -10dB/decade slope									
	(OIF) CEI	100 MHz to 4.875 GHz: -8dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope									

Table 1–19. Stratix IV GX Transceiver Specification (Part 4 of 4)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Commercial/Industrial and -2x Commercial Speed Grade *(1)*			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: -6dB									
	(OIF) CEI	100 MHz to 4.875 GHz: -6dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope									
Rise time	—	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	ps
Intra differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	—	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	—	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1											
CMU PLL lock time from `CMUPLL_reset` deassertion	—	—	—	100	—	—	100	—	—	100	µs
PLD-Transceiver Interface											
Interface speed	—	25	—	250	25	—	250	25	—	250	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									—

Notes to Table 1–19:

(1) The -2x speed grade is the fastest speed grade offered in the following Stratix IV GX devices: EP4SGX70DF29, EP4SGX110DF29, EP4SGX110FF35, EP4SGX230DF29, EP4SGX110FF35, EP4SGX230DF29, EP4SGX230FF35, EP4SGX290FF35, EP4SGX290FH29, EP4SGX360FF35, and EPSGX360FH29.

(2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in transmitter only mode. The minimum `reconfig_clk` frequency is 37.5MHz if the transceiver channel is configured in receiver only or receiver and transmitter mode. For more details, refer to the *Stratix IV Dynamic Reconfiguration* chapter in volume 1 of the *Stratix IV Device Handbook*.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The 1.1-V RX V_{ICM} setting must be used if the input serial data standard is LVDS and the link is DC coupled.

(5) The rate matcher supports only up to +/-300 ppm.

(6) Time taken to `rx_pll_locked` goes high from `rx_analogreset` deassertion. Refer to Figure 1–1.

(7) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1.

(8) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1.

(9) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2.

Figure 1–1 shows the lock time parameters in manual mode. Figure 1–2 shows the lock time parameters in automatic mode.

LTD = Lock-To-Data LTR = Lock-To-Reference

Figure 1–1. Lock Time Parameters for Manual Mode

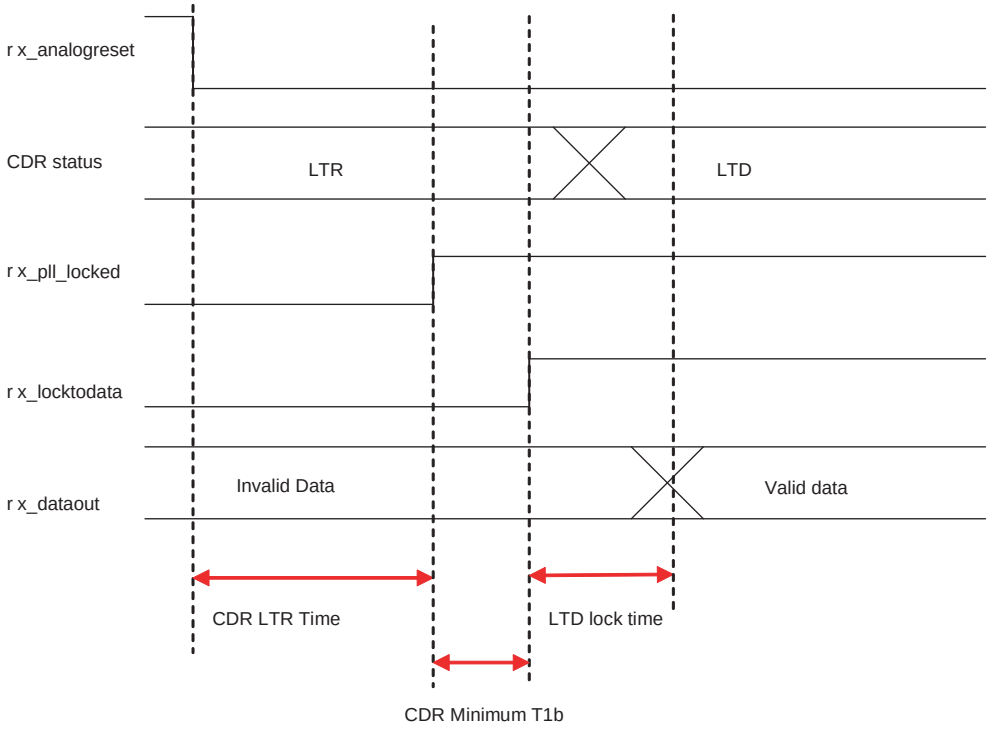


Figure 1–2. Lock Time Parameters for Automatic Mode

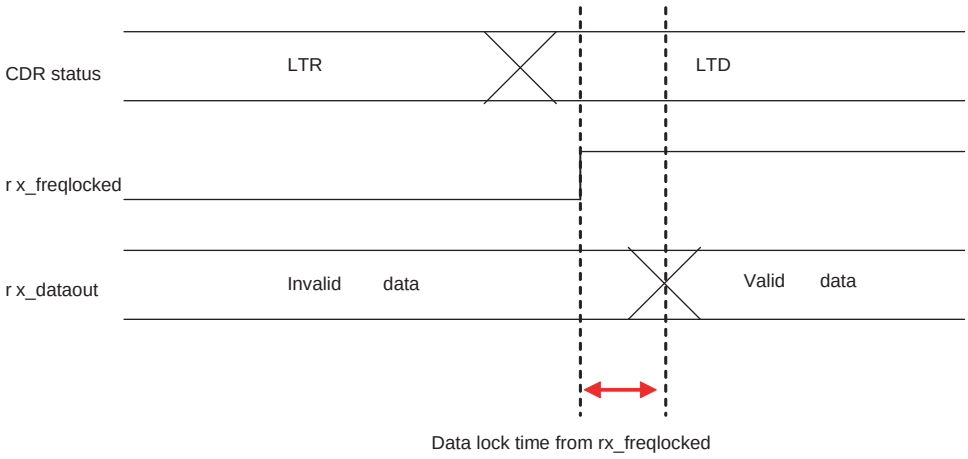


Table 1–20 through Table 1–23 show the typical V_{OD} for various differential termination settings.

Table 1–20. Typical V_{OD} Setting, TX Term = 85 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} Typical (mV)	170	340	510	595	680	765	850	1020

Table 1–21. Typical V_{OD} Setting, TX Term = 100 W

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} Typical (mV)	200	400	600	700	800	900	1000	1200

Table 1–22. Typical V_{OD} Setting, TX Term = 120 Ω

Symbol	V_{OD} Setting (mV)						
	0	1	2	3	4	5	6
V_{OD} Typical (mV)	240	480	720	840	960	1080	1200

Table 1–23. Typical V_{OD} Setting, TX Term = 150 Ω

Symbol	V_{OD} Setting (mV)					
	0	1	2	3	4	5
V_{OD} Typical (mV)	300	600	900	1050	1200	1350

Table 1–24 shows the Stratix IV GX transceiver block AC specifications.

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 1 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(3)*											
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS23	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS23	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS23	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS23	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance *(3)*											

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 2 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS23		> 15			> 15			> 15		UI
	Jitter frequency = 25 KHZ Pattern = PRBS23		> 1.5			> 1.5			> 1.5		UI
	Jitter frequency = 250 KHz Pattern = PRBS23		> 0.15			> 0.15			> 0.15		UI
Jitter tolerance at 2488.32 MBps	Jitter frequency = 0.06 KHz Pattern = PRBS23		> 15			> 15			> 15		UI
	Jitter frequency = 100 KHZ Pattern = PRBS23		> 1.5			> 1.5			> 1.5		UI
	Jitter frequency = 1 MHz Pattern = PRBS23		> 0.15			> 0.15			> 0.15		UI
	Jitter frequency = 10 MHz Pattern = PRBS23		> 0.15			> 0.15			> 0.15		UI
Fibre Channel Transmit Jitter Generation *(4)*, *(12)*											
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	—	—	0.23	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	—	—	0.11	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	—	—	0.33	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	—	—	0.2	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	—	—	0.52	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	—	—	0.33	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance *(4)*, *(13)*											
Deterministic jitter FC-1	Pattern = CJTPAT		> 0.37			> 0.37			> 0.37		UI
Random jitter FC-1	Pattern = CJTPAT		> 0.31			> 0.31			> 0.31		UI
Sinusoidal jitter FC-1	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI
Deterministic jitter FC-2	Pattern = CJTPAT		> 0.33			> 0.33			> 0.33		UI
Random jitter FC-2	Pattern = CJTPAT		> 0.29			> 0.29			> 0.29		UI
Sinusoidal jitter FC-2	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 3 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Deterministic jitter FC-4	Pattern = CJTPAT		> 0.33			> 0.33			> 0.33		UI
Random jitter FC-4	Pattern = CJTPAT		> 0.29			> 0.29			> 0.29		UI
Sinusoidal jitter FC-4	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI
XAUI Transmit Jitter Generation *(5)*											
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance *(5)*											
Total jitter	—		> 0.65			> 0.65			> 0.65		UI
Deterministic jitter	—		> 0.37			> 0.37			> 0.37		UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(6)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern	—	—	—	—	—	—	—	—	—	UI
PCI Express Receiver Jitter Tolerance *(6)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6			> 0.6			> 0.6		UI
Total jitter at 2.5 Gbps (Gen2)	Compliance pattern	—	—	—	—	—	—	—	—	—	UI
Serial RapidIO Transmit Jitter Generation *(7)*											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Serial RapidIO Receiver Jitter Tolerance *(7)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37			> 0.37			> 0.37		UI

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 4 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55			> 0.55			> 0.55		UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
GIGE Transmit Jitter Generation *(8)*											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance *(8)*											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.4			> 0.4			> 0.4		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66			> 0.66			> 0.66		UI
HiGig Transmit Jitter Generation *(9)*											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance *(9)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT		> 0.37		—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT		> 0.65		—	—	—	—	—	—	UI

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 5 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	—	—	—	UI
	Jitter Frequency = 1.875MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
(OIF) CEI Transmitter Jitter Generation *(10)*											
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	N/A	—	—	N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(10)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.675			N/A	—	—	N/A	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern=PRBS31 BER = 10^{-12}	> 0.988			N/A	—	—	N/A	—	—	UI

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 6 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 5			N/A	—	—	N/A	—	—	UI
	Jitter Frequency = 3.82 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.05			N/A	—	—	N/A	—	—	UI
	Jitter Frequency = 20 MHz Data Rate= 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.05			N/A	—	—	N/A	—	—	UI
SDI Transmitter Jitter Generation *(11)*											
Alignment jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.2	—	—	0.2	—	—	0.2	—	—	UI
	Data Rate = 2.97 Gbps (3G) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.3	—	—	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance *(11)*											

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 7 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 2			> 2			> 2		UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 0.3			> 0.3			> 0.3		UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 0.3			> 0.3			> 0.3		UI

Table 1–24. Stratix IV GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 8 of 8)

Symbol/ Description	Conditions	-2 Speed Commercial Speed Grade			-3 Speed Commercial and Industrial Speed Grade			-4 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 1			> 1			> 1		UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 0.2			> 0.2			> 0.2		UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) Pattern =75% Color Bar		> 0.2			> 0.2			> 0.2		UI

Notes to Table 1–24:

(1) Dedicated `refclk` pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(4) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(5) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(6) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(7) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(8) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(9) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(11) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(12) The fibre channel transmitter jitter generation numbers are compliant to the specification at δ_T interoperability point.
(13) The fibre channel receiver jitter tolerance numbers are compliant to the specification at δ_R interoperability point.

Core Performance Specifications

This sections describes the clock tree, PLL, DSP, TriMatrix, and configuration and JTAG specifications.

Clock Tree Specifications

Table 1–25 lists the clock tree specifications for Stratix IV devices.

Table 1–25. Stratix IV Clock Tree Performance - Preliminary

Device	Performance			Unit
	-2/-2x Speed Grade	-3 Speed Grade	-4 Speed Grade	
EP4SE110	600	500	450	MHz
EP4SE230	600	500	450	MHz
EP4SE290	600	500	450	MHz
EP4SE360	600	500	450	MHz
EP4SE530	600	500	450	MHz
EP4SE680	600	500	450	MHz
EP4SGX70	600	500	450	MHz
EP4SGX110	600	500	450	MHz
EP4SGX230	600	500	450	MHz
EP4SGX290	600	500	450	MHz
EP4SGX360	600	500	450	MHz
EP4SGX530	600	500	450	MHz

PLL Specifications

Table 1–26 describes the Stratix IV PLL specifications when operating in both the commercial junction temperature range (0 to 85×C) and the industrial junction temperature range (-40 to 100×C).

Table 1–26. Stratix IV PLL Specifications - Preliminary (Part 1 of 2)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	5	—	720 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO} *(2)*	PLL VCO operating Range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ}	Input clock cycle to cycle jitter	—	—	*(4)*	ps
f_{OUT}	Output frequency for internal global or regional clock	—	—	717 *(3)*	MHz
f_{OUT_EXT}	Output frequency for external clock output	—	—	717 *(3)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Dedicated clock output period jitter	—	—	*(4)*	ps
t_{OUTPJ_IO}	Regular I/O clock output period jitter	—	—	*(4)*	ps
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chains	—	*(4)*	—	SCANCLK cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	1	—	1	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	*(4)*	ms

Table 1–26. Stratix IV PLL Specifications - Preliminary (Part 2 of 2)

Symbol	Description	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	*(4)*	ms
f_{CLBW}	PLL closed-loop low bandwidth range	—	*(4)*	—	MHz
	PLL closed-loop medium bandwidth range	—	*(4)*	—	MHz
	PLL closed-loop high bandwidth range	—	*(4)*	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	*(4)*	—	ps
t_{ARESET}	Minimum pulse width on *areset* signal	10	—	—	ns

Notes to Table 1–26:

(1) F_{IN} is limited by I/O F_{MAX}.
(2) The VCO frequency reported by Quartus II software is after the post scale divider (k) and may be outside the VCO min and max range.
(3) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.
(4) Pending silicon characterization.

DSP Block Specifications

Table 1–27 describes the Stratix IV DSP block performance specifications.

Table 1–27. Stratix IV DSP Block Performance Specifications *(Note 1)* - Preliminary

Mode	Resources Used	Performance			Unit
	Number of Multipliers	-2/-2x Speed Grade	-3 Speed Grade	-4 Speed Grade	
9×9-bit multiplier	1	490	405	375	MHz
12×12-bit multiplier	1	490	405	375	MHz
18×18-bit multiplier	1	550	455	420	MHz
36×36-bit multiplier	1	440	365	335	MHz
18×18-bit multiply accumulator	4	490	405	375	MHz
18×18-bit multiply adder	4	490	405	375	MHz
18×18-bit multiply adder-signed full precision	2	490	405	375	MHz
18×18-bit multiply adder with loopback *(2)*	2	390	320	300	MHz
36-bit shift (32 bit data)	1	440	365	335	MHz
Double mode	1	440	365	335	MHz

Notes to Table 1–27:

(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.
(2) Maximum is for non-pipelined block with loopback input registers disabled and **Round** and **Saturation** disabled.

TriMatrix Memory Block Specifications

Table 1–28 describes the Stratix IV TriMatrix memory block specifications.

Table 1–28. Stratix IV TriMatrix Memory Block Performance Specifications Preliminary

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	TriMatrix Memory	-2 /-2x Speed Grade	-3 Speed Grade	-4 Speed Grade	
MLAB	Single port 64×10	0	1	600	500	450	MHz
	Simple dual-port 32×20 single clock	0	1	600	500	450	MHz
	Simple dual-port 64×10 single clock	0	1	600	500	450	MHz
M9K Block	Single-port 256×36	0	1	600	500	450	MHz
	Simple dual-port 256×36 single CLK	0	1	600	500	450	MHz
	True dual port 512×18 single CLK	0	1	600	500	450	MHz
M144K	Single-port 2K×72	0	1	600	500	450	MHz
	Simple dual-port 2K×72 dual CLK	0	1	600	500	450	MHz
	Simple dual-port 2K×64 dual CLK (with ECC)	0	1	333	275	250	MHz
	True dual-port 4K×36 dual CLK	0	1	600	500	450	MHz

Configuration and JTAG Specifications

Table 1–29 lists the Stratix IV configuration mode specifications.

Table 1–29. Stratix IV Configuration Mode Specifications - Preliminary

Programming Mode	DCLK Fmax	Unit
Passive serial	125	MHz
Fast passive parallel	125	MHz
Fast active serial	40	MHz
Remote update only in fast AS mode	10	MHz

Table 1–30 shows the JTAG timing parameters and values for Stratix IV devices.

Table 1–30. Stratix IV JTAG Timing Parameters and Values - Preliminary

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 *(1)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(1)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(1)*	ns

Note to Table 1–30:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.3 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Temperature Sensing Diode Specifications

Table 1–31 lists the specifications for the Stratix IV temperature sensing diode.

Table 1–31. Temperature Sensing Diode Specifications - Preliminary

Symbol	Description	Min	Max	Unit
f_{TSD_INCLK}	TSD Input Clock Frequency (without CLK divider)	0.25	1.01	MHz
	TSD Input Clock Frequency (with CLK divider)	38	42	MHz
$t_{DUTY\_TSD\_INCLK}$	Duty Cycle of TSD Input Clock	45	55	%

Periphery Performance

This section describes periphery performance including high-speed I/O, external memory interface, and OCT calibration block specifications.

High-Speed I/O Specification

Table 1–32 shows the high-speed I/O timing for Stratix IV devices.

Table 1–32. High-Speed I/O Specifications for Fastest Speed Grade - Preliminary ***(Note 1), (2), (3), (4)*** (Part 1 of 2)

Symbol	Conditions	-2/-2x Speed Grade			Unit
		Min	Typ	Max	
f_{IN} (input reference clock frequency) = f_{HSDR} / W	Clock boost factor, W = 1 to 40	5	—	717	MHz
f_{HSCLK} (source synchronous output clock frequency)	—	5 *(5)*	—	717	MHz
f_{HSDR} (data rate)	Serdes factor, J = 3 to 10	150	—	1600	Mbps
	Serdes factor, J = 2, Uses DDR Registers	*(6)*	—	1250	Mbps
	Serdes factor, J = 1, Uses SDR Register	*(6)*	—	717 *(7)*	Mbps
$f_{HSDRDPA}$ (DPA data rate)	Serdes factor, J = 3 to 10	150	—	1600	Mbps
Transmitter channel-to-channel skew (TCCS)	All differential standards	—	—	*(5)*	ps
Receiver sampling window (SW)	All differential standards	—	—	*(5)*	ps
$t_{OUTJITTER\_DC}$	—	—	—	*(5)*	ps
$t_{OUTJITTER\_IO}$	—	—	—	*(5)*	ps
Output t_{RISE}	All differential I/O standards	—	—	*(5)*	ps
Output t_{FALL}	All differential I/O standards	—	—	*(5)*	ps
t_{DUTY}	Tx output clock duty cycle	45	50	55	%
DPA run length	—	—	—	*(5)*	UI

Table 1–32. High-Speed I/O Specifications for Fastest Speed Grade - Preliminary *(Note 1), (2), (3), (4)* (Part 2 of 2)

Symbol	Conditions	-2/-2x Speed Grade			Unit
		Min	Typ	Max	
DPA jitter tolerance	Data channel peak-to-peak jitter tolerance	*(5)*	—	—	UI

Notes to Table 1–32:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following Left/Right PLL output specification: 150 <= input clock frequency × W <= 1600 MHz.

(4) Specifications for -3 and -4 speed grades will be available after silicon characterization.

(5) Pending silicon characterization.

(6) The minimum specification is dependent on the clock source (for example, PLL or clock pin) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register does not have a minimum toggle rate.

(7) Same as device clock tree F_{MAX}.

Table 1–33 shows the DPA lock time specifications for Stratix IV devices.

Table 1–33. DPA Lock Time Specifications - Preliminary

Standard	Training Pattern	Transition Density	Min	Unit
SPI-4	00000000001111111111	10%	*(1)*	Number of repetitions
Parallel Rapid I/O	00001111	25%	*(1)*	Number of repetitions
	10010000	50%	*(1)*	Number of repetitions
Miscellaneous	10101010	100%	*(1)*	Number of repetitions
	01010101	—	*(1)*	Number of repetitions

Note to Table 1–33:

(1) Pending silicon characterization.

External Memory Interface Specifications

Table 1–34 through Table 1–43 list the external memory interface specifications for the Stratix IV device family. Use these tables for memory interface timing analysis.

Table 1–34. Stratix IV Maximum Clock Rate Support for External Memory Interfaces with Half-Rate Controller *(Note 1)*, *(2)* (Part 1 of 2)

Memory Standards	Stratix IV GX Devices with 1152-Pin (with 24 Transceivers), 1517-Pin, and 1932-Pin Packages						Stratix IV GX Devices with 780-Pin and 1152-Pin (with 16 Transceivers) Packages					
	–2 Speed Grade (MHz)		–3 Speed Grade (MHz)		–4 Speed Grade (MHz)		-2x Speed Grade (MHz)		-3 Speed Grade (MHz)		-4 Speed Grade (MHz)	
	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*
DDR3 SDRAM *(4)*	533	333	400	333	333	333	333	333	333	333	333	333
DDR2 SDRAM *(4)*	400	333	333	333	333	333	333	333	333	333	333	333
DDR SDRAM *(4)*	200	200	200	200	200	200	200	200	200	200	200	200

Table 1–34. Stratix IV Maximum Clock Rate Support for External Memory Interfaces with Half-Rate Controller *(Note 1)*, *(2)* (Part 2 of 2)

Memory Standards	Stratix IV GX Devices with 1152-Pin (with 24 Transceivers), 1517-Pin, and 1932-Pin Packages						Stratix IV GX Devices with 780-Pin and 1152-Pin (with 16 Transceivers) Packages					
	–2 Speed Grade (MHz)		–3 Speed Grade (MHz)		–4 Speed Grade (MHz)		-2x Speed Grade (MHz)		-3 Speed Grade (MHz)		-4 Speed Grade (MHz)	
	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*	Column I/O Banks	Row I/O Banks *(3)*
QDRII+SRAM (2.5 clock cycle latency only) *(5)*, *(6)*	400	300	350	300	300	300	300	300	300	300	300	300
QDRII SRAM (1.5-V and 1.8-V HSTL) *(6)*	350	300	300	300	300	300	300	300	300	300	300	300
RLDRAM II (1.5-V and 1.8-V HSTL)	400	333	333	333	333	333	333	333	333	333	333	333

Notes to Table 1–34:

(1) Numbers are preliminary pending characterization. The supported operating frequencies listed here are memory interface maximums for the FPGA device family. Your design's actual achievable performance is based on design and system-specific factors, as well as static timing analysis of the completed design.

(2) Column I/Os refer to top and bottom I/Os. Row I/Os refer to left and right I/Os.

(3) The row I/O banks do not support 1.5-V HSTL and SSTL Class II I/O standards.

(4) This applies for interfaces with both modules and components.

(5) The QDRII+ SRAM devices with 2.0 clock cycle latency are not supported due to hardware limitations.

(6) Stratix IV devices in the 780- and 1152-pin packages support ×36 QDRII+/QDRII SRAM at a lower maximum frequency as detailed in the *External Memory Interfaces in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*.

Table 1–35. Stratix IV Maximum Clock Rate Support for External Memory Interfaces with Full-Rate Controller *(Note 1)*, *(2)*, *(3)*

Memory Standards	-2/-2x Speed Grade (MHz)		-3 Speed Grade (MHz)		-4 Speed Grade (MHz)	
	Column I/O Banks	Row I/O Banks *(4)*	Column I/O Banks	Row I/O Banks *(4)*	Column I/O Banks	Row I/O Banks *(4)*
DDR2 SDRAM	267	267	233	233	200	200
DDR SDRAM	200	200	200	200	200	200

Notes to Table 1–35:

(1) Numbers are preliminary until characterization is final. The supported operating frequencies listed here are memory interface maximums for the FPGA device family. Your design's actual achievable performance is based on design and system-specific factors, as well as static timing analysis of the completed design.

(2) Column I/Os refer to top and bottom I/Os. Row I/Os refer to left and right I/Os.

(3) This applies for interfaces with both modules and components.

(4) The row I/O banks do not support 1.5 V HSTL and SSTL Class II I/O standards.

Table 1–36. Stratix IV Maximum Clock Rate Support with the ×36 Mode Emulation *(Note 1)*, *(2)*, *(3)*

Memory Standards	-2/-2x Speed Grade (MHz)		-3/-3x Speed Grade (MHz)		–4 Speed Grade (MHz)	
	Column I/O Banks	Row I/O Banks *(4)*	Column I/O Banks	Row I/O Banks *(4)*	Column I/O Banks	Row I/O Banks *(4)*
QDRII+SRAM (2.5 clock cycle latency only) *(4)*	300	250	250	167	250	167
QDRII SRAM (1.5-V and 1.8-V HSTL)	300	250	250	167	250	167

Notes to Table 1–36:

(1) Numbers, based on using the half-rate controller, are preliminary until characterization is final. The supported operating frequencies listed here are memory interface maximums for the FPGA device family. Your design's actual achievable performance is based on design and system-specific factors as well as static timing analysis of the completed design.

(2) The performance listed in this table is lower than the performance listed in Table 1–34 due to double loading of the CQ/CQn pins. Double loading causes degradation in the signal slew rate which affects FPGA delay. Furthermore, due to the difference in slew rate, there is a shift in the setup and hold time window. You can perform an IBIS simulation to illustrate the shift in the clock signals.

(3) Column I/Os refer to top and bottom I/Os. Row I/Os refer to left and right I/Os.

(4) The QDRII+ SRAM devices with 2.0 clock cycle latency are not supported due to hardware limitations.

External Memory I/O Timing Specifications

Table 1–37 and Table 1–38 list Stratix IV device timing uncertainties on the read and write data paths. Use these specifications to determine timing margins for source synchronous paths between a Stratix IV FPGA and an external memory device.

Table 1–37. Sampling Window (SW) - Read Side - Preliminary

Memory Type	I/O Standard	Width	Sampling window (ps)					
			-2/-2x Speed Grade		-3 Speed Grade		-4 Speed Grade	
			Setup	Hold	Setup	Hold	Setup	Hold
DDR3	1.5 SSTL	×4	250	250	300	300	374	374
		×8	250	250	300	300	374	374
DDR2 Differential	1.8 V SSTL	×4	181	306	234	326	257	326
		×8	181	306	234	326	257	326
DDR2 SEIO	1.8 V SSTL	×4	231	256	284	276	307	276
		×8	231	256	284	276	307	276
DDR1 SEIO	2.5 V SSTL	×4	231	256	284	261	307	261
		×8	231	256	284	261	307	261
QDRII/II+	1.5 V HSTL	×9	231	256	284	261	307	261
		×18	261	286	314	291	337	291
		×36	261	286	314	291	337	291
QDRII/II+ Emulation	1.5 V HSTL	×36	261	328	314	337	337	350
QDRII	1.8 V HSTL	×9	231	256	284	261	307	261
		×18	261	286	314	291	337	291
		×36	261	286	314	291	337	291

Table 1–37. Sampling Window (SW) - Read Side - Preliminary

Memory Type	I/O Standard	Width	Sampling window (ps)					
			-2/-2x Speed Grade		-3 Speed Grade		-4 Speed Grade	
			Setup	Hold	Setup	Hold	Setup	Hold
RLDRAM II	1.5 V HSTL	×9	181	306	234	326	257	326
		×18	211	336	264	356	287	356
		×9	181	306	234	326	257	326
		×18	211	336	264	356	287	356

Table 1–38. Transmitter Channel-to-Channel Skew (TCCS) - Write Side - Preliminary

Memory Type	I/O Standard	Width	TCCS (ps)					
			-2/-2x Speed Grade		-3 Speed Grade		-4 Speed Grade	
			Lead	Lag	Lead	Lag	Lead	Lag
DDR3	1.5 SSTL	×4	260	260	290	290	310	310
		×8	260	260	290	290	310	310
DDR2 Differential	1.8 V SSTL	×4	229	246	230	355	250	388
		×8	229	246	230	355	250	388
DDR2 SEIO	1.8 V SSTL	×4	316	168	318	239	346	260
		×8	316	168	318	239	346	260
DDR1 SEIO	2.5 V SSTL	×4	313	157	315	222	343	242
		×8	313	157	315	222	343	242
QDRII/II+	1.5 V HSTL	×9	260	248	262	358	285	391
		×18	290	278	292	388	315	421
		×36	290	278	292	388	315	421
QDRII/II+ Emulation	1.5 V HSTL	×36	310	298	312	408	335	441
QDRII	1.8 V HSTL	×9	229	246	230	355	250	388
		×18	259	276	260	385	280	418
		×36	259	276	260	385	280	418
RLDRAM II	1.5	×9	260	248	262	358	285	391
		×18	290	278	292	388	315	421
		×9	229	246	230	355	250	388
		×18	259	276	260	385	280	418

DLL and DQS Logic Block Specifications

Table 1–39 describes the DLL frequency range specifications for Stratix IV devices.

Table 1–39. Stratix IV DLL Frequency Range Specifications - Preliminary

Frequency Mode	Frequency Range (MHz)			Resolution
	-2/-2x Speed Grade	-3 Speed Grade	-4 Speed Grade	
0	90 - 150	90 - 140	90 - 120	22.5
1	120 - 200	120 - 190	120 - 170	30
2	150 - 240	150 - 230	150 - 200	36
3	180 - 300	180 - 290	180 - 250	45
4	240 - 370	240 - 350	240 - 310	30
5	290 - 450	290 - 420	290 - 370	36
6	360 - 560	360 - 530	360 - 460	45

Table 1–40 describes the DQS phase offset delay per stage for Stratix IV devices.

Table 1–40. DQS Phase Offset Delay Per Setting *(Note 1)*, *(2)*, *(3)*

Speed Grade	Min	Max	Unit
-2/-2x	7	13	ps
-3	8	14	ps
-4	8.5	15.5	ps

Notes to Table 1–40:

(1) The valid settings for phase offset are -64 to +63 for frequency mode 0 to 3 and -32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear, with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10 phase offset settings to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 * 10.5 ps) ± 20 ps] = 730 ps ± 20 ps

OCT Calibration Block Specifications

Table 1–41 describes the OCT calibration block specifications for Stratix IV devices.

Table 1–41. OCT Calibration Block Specifications — Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	28	—	Cycles
T_{RS_RT}	Time required to dynamically switch from R_S to R_T	—	2.5	—	ns

Duty Cycle Distortion (DCD) Specifications

Table 1–42 lists the worst case DCD for Stratix IV devices.

Table 1–42. DCD on Stratix IV I/O Pins *(Note 1)*, *(2)* — Preliminary

Symbol	-2/2x Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle *(2)*	45	55	45	55	45	55	%

Notes to Table 1–42:

(1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree, and IOE driving dedicated and general purpose I/O pins.

(2) Detailed DCD specifications pending silicon characterization.

I/O Timing

Altera offers two ways to determine I/O timing: the Excel-based I/O timing and the Quartus II Timing Analyzer.

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O timing spreadsheet can be downloaded from the Stratix IV Device Literature webpage.

Programmable IOE Delay

Table 1–43 shows Stratix IV IOE programmable delay settings.

Table 1–43. Stratix IV IOE Programmable Delay

Parameter	Available Settings	-3 Speed Grade	
		Min Delay (ps)	Max Delay (ps)
D1	16	150	900
D2	8	330	700
D3	8	155	2581
D9	16	123	897
D10	7	118	377

Programmable Output Buffer Delay

Table 1–44 lists the delay chain settings that control the rising and falling edge delays of the output buffer. Default delay is 0 ps.

Table 1–44. Programmable Output Buffer Delay

Symbol	Parameter	Typ	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

Table 1–45 shows the glossary for this chapter.

Table 1–45. Glossary Table

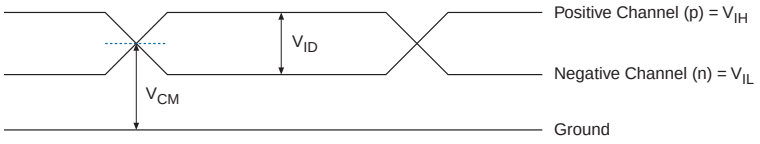
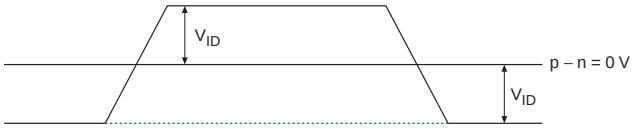
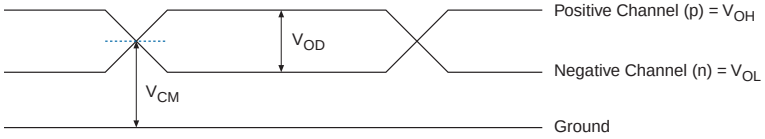
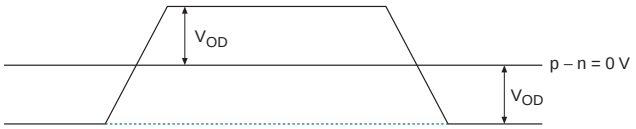
Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—

Table 1–45. Glossary Table

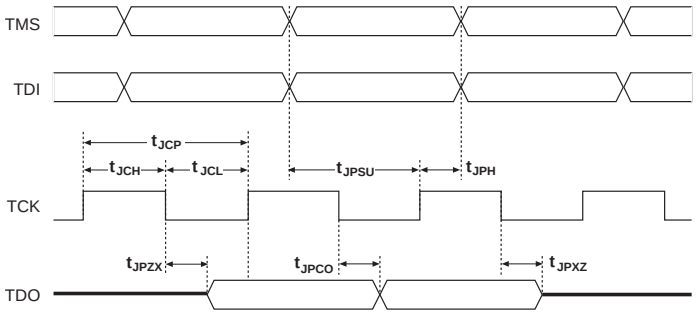
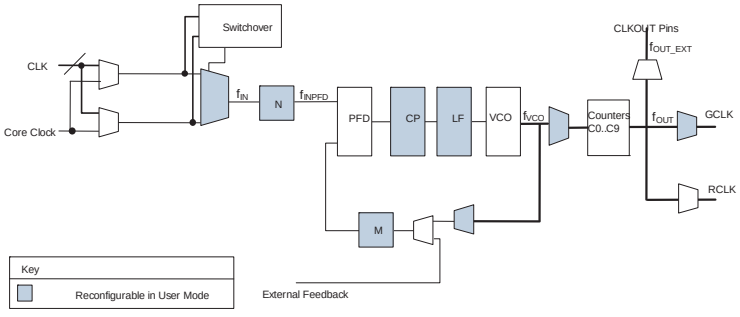
Letter	Subject	Definitions
F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G	—	—
H	—	—
I	—	—
J	J	HIGH-SPEED I/O Block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications are in the following figure: 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	**PLL Specifications**	The block diagram shown in the following figure highlights the PLL Specification parameters: **Diagram of PLL Specifications** *(1)*  **Note:** (1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Stratix IV device).

Table 1–45. Glossary Table

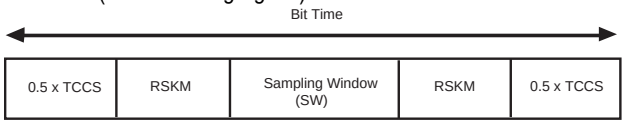
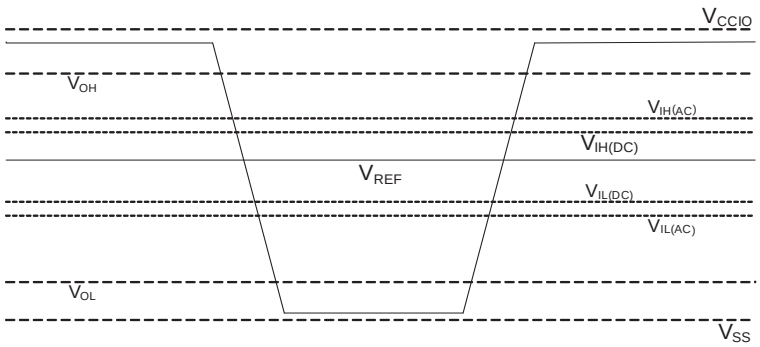
Letter	Subject	Definitions
S	**SW (sampling window)**	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window as shown in (the following figure):  *Timing Diagram*
	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTI and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing as shown in the following figure: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and the slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table)
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock. **Timing Unit Interval (TUI)** The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on PLL clock input
	t_{OUTPJ_IO}	Period jitter on general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on dedicated clock output driven by a PLL
	t_{RISE}	Signal Low-to-high transition time (20-80%)
U	—	—

Table 1–45. Glossary Table

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential Input Voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
W	W	HIGH-SPEED I/O BLOCK: Clock Boost Factor
X	—	—
Y	—	—
Z	—	—

Documents Referenced

This chapter references the following documents:

- *External Memory Interfaces in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*
- *PowerPlay Early Power Estimator User Guide for Stratix III and Stratix IV FPGAs*

PowerPlay Power Analysis chapter in the *Quartus II Handbook*

Document Revision History

Table 1–46 shows the revision history for this document.

Table 1–46. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2008 v2.1	■ Edited "I/O Timing" section	—
November 2008 v2.0	■ Minor text edits. ■ Updated Table 1–19, Table 1–32, Table 1–34 - Table 1–39	Minor text edits.
August 2008 v1.1	■ Updated Table 1–1, Table 1–2, Table 1–4, Table 1–5, and Table 1–26. ■ Removed figures from "Transceiver Performance Specifications" on page 1–10 that are repeated in the glossary.	Minor text edits and an additional note to Table 1–26.
May 2008 v1.0	Initial release.	—