Silicon PNP Power Transistors 2SB720

DESCRIPTION

·With TO-220 package
·High V_{CEO}
·High power dissipation

APPLICATIONS

·Power amplifier
·TV vertical deflection output

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base

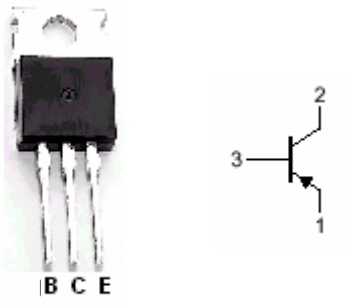

Fig.1 simplified outline (TO-220) and symbol

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-200	V
V_{CEO}	Collector-emitter voltage	Open base	-200	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-2.0	A
I_{CM}	Collector current-peak		-3.0	A
P_T	Total power dissipation	T_C=25□	25	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

Silicon PNP Power Transistors 2SB720

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-5mA ,I_B=0	-200			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C=-0.1mA ,I_E=0	-200			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=-0.1mA ,I_C=0	-5			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-500mA; I_B=-50mA			-1.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=-500mA; I_B=-50mA			-1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=-200V; I_E=0			-10	μA
I_{EBO}	Emitter cut-off current	V_{EB}=-5V; I_C=0			-10	μA
h_{FE}	DC current gain	I_C=-0.15A ; V_{CE}=-5V	35		200	
f_T	Transition frequency	I_C=-0.15A ; V_{CE}=-5V		100		MHz

PACKAGE OUTLINE

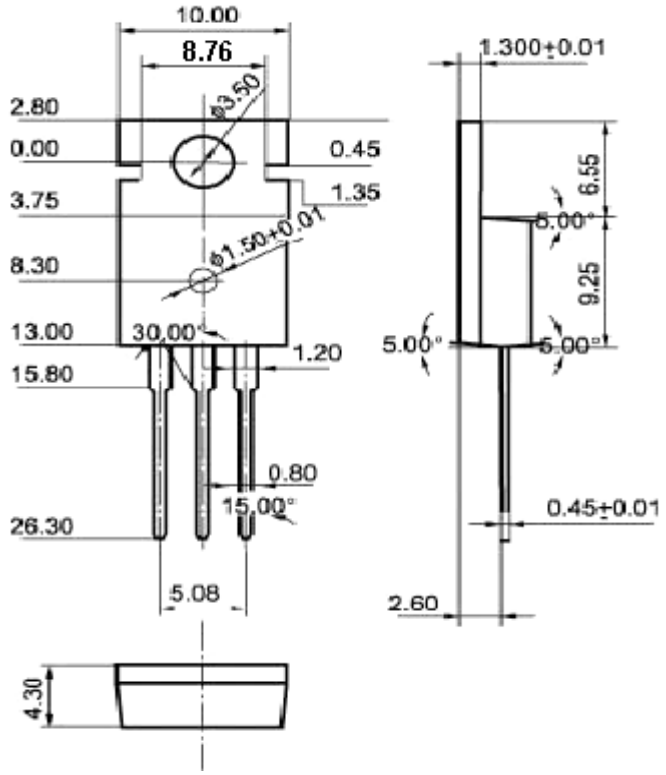

Fig.2 Outline dimensions(unindicated tolerance:±0.10 mm)