

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.30
Q_g (Max.) (nC)	76	
Q_{gs} (nC)	20	
Q_{gd} (nC)	37	
Configuration	Single	

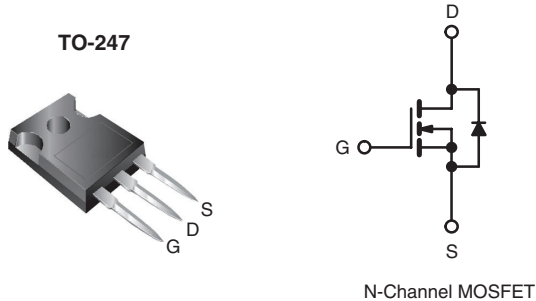
FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Isolated Central Mounting Hole
- Dynamic dV/dt Rated
- Repetitive Avalanche Rated
- Lead (Pb)-free Available


 Available
RoHS*
 COMPLIANT

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced MOSFETs technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of MOSFETs offer the designer a new standard in power transistors for switching applications. The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP350LCPbF
	SiHFP350LC-E3
SnPb	IRFP350LC
	SiHFP350LC


ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	V_{GS} at 10 V $T_C = 25$ °C	16
		$T_C = 100$ °C	9.9
Pulsed Drain Current ^a	I_{DM}	64	A
Linear Derating Factor		1.5	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	390	mJ
Repetitive Avalanche Current ^a	I_{AR}	16	A
Repetitive Avalanche Energy ^a	E_{AR}	19	mJ
Maximum Power Dissipation	P_D	190	W
Peak Diode Recovery dV/dt ^c	dV/dt	4.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	
		1.1	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 2.7$ μ H, $R_G = 25$ Ω , $I_{AS} = 16$ A (see fig. 12).
- $I_{SD} \leq 16$ A, $dI/dt \leq 200$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.49	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 320\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 9.6\text{ A}^b$	-	-	0.30	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 19\text{ A}^b$	8.1	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	2200	-	pF
Output Capacitance	C_{oss}		-	390	-	
Reverse Transfer Capacitance	C_{rss}		-	31	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 16\text{ A}$, $V_{DS} = 320\text{ V}$ see fig. 6 and 13 ^b	-	-	76	nC
Gate-Source Charge	Q_{gs}		-	-	20	
Gate-Drain Charge	Q_{gd}		-	-	37	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}$, $I_D = 16\text{ A}$, $R_G = 6.2\Omega$, $R_D = 12\Omega$, see fig. 10 ^b	-	14	-	ns
Rise Time	t_r		-	54	-	
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	
Fall Time	t_f		-	35	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	16	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	64	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 16\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}^b$	-	440	660	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	4.1	6.2	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

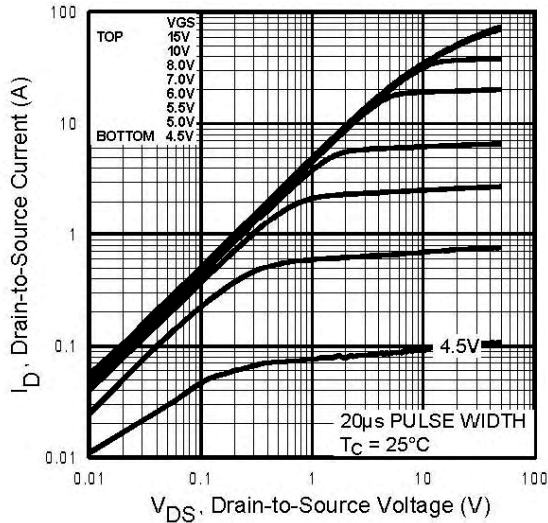


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

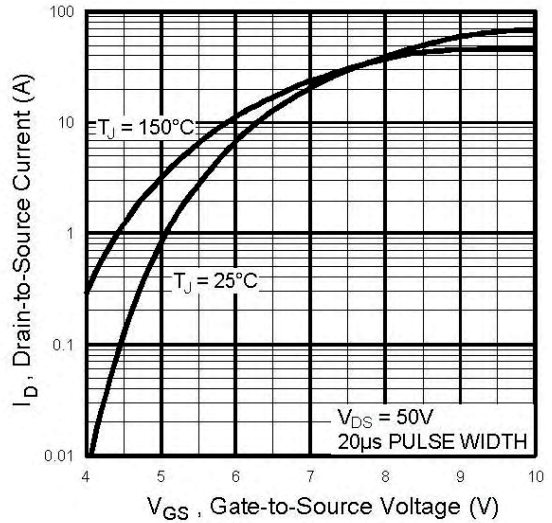


Fig. 3 - Typical Transfer Characteristics

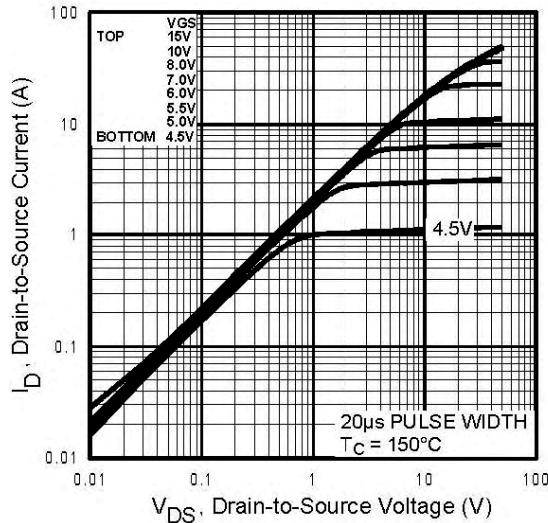


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

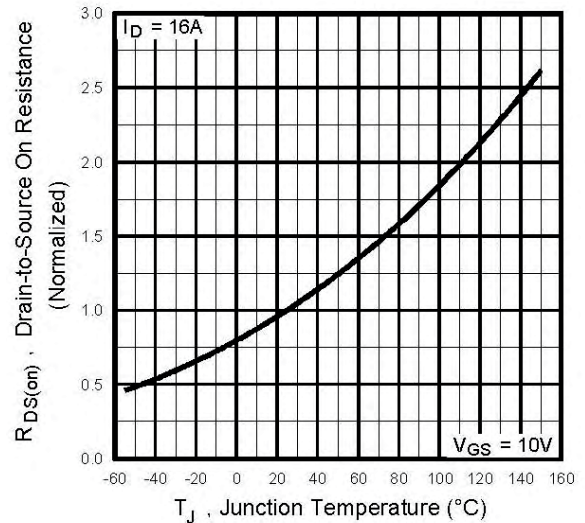


Fig. 4 - Normalized On-Resistance vs. Temperature

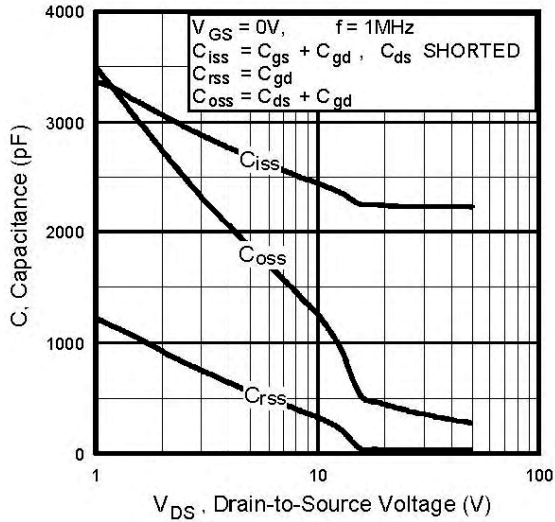


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

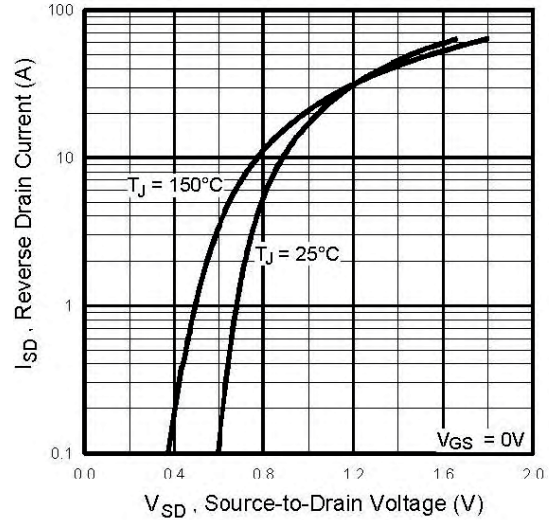


Fig. 7 - Typical Source-Drain Diode Forward Voltage

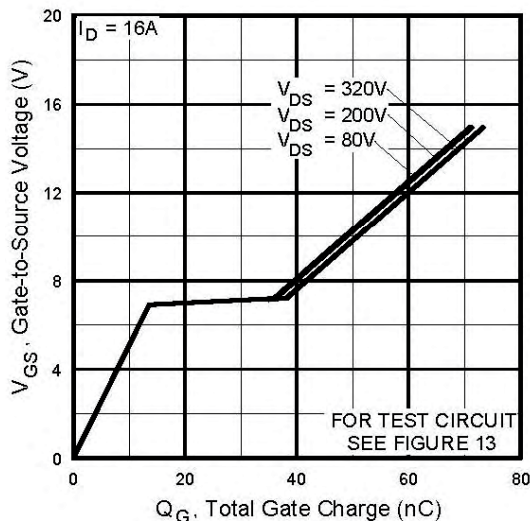


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

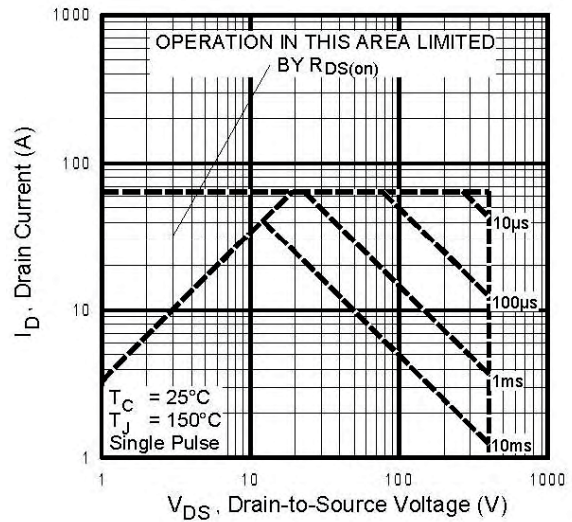


Fig. 8 - Maximum Safe Operating Area

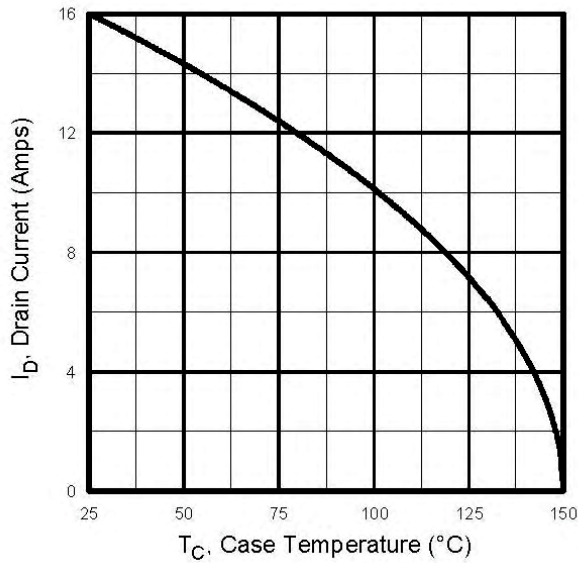


Fig. 9 - Maximum Drain Current vs. Case Temperature

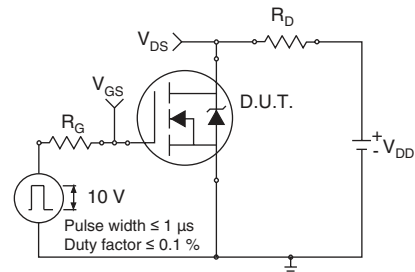


Fig. 10a - Switching Time Test Circuit

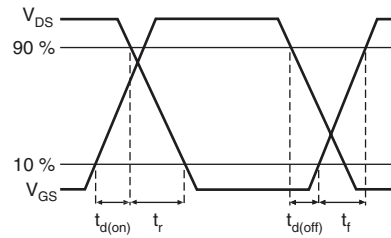


Fig. 10b - Switching Time Waveforms

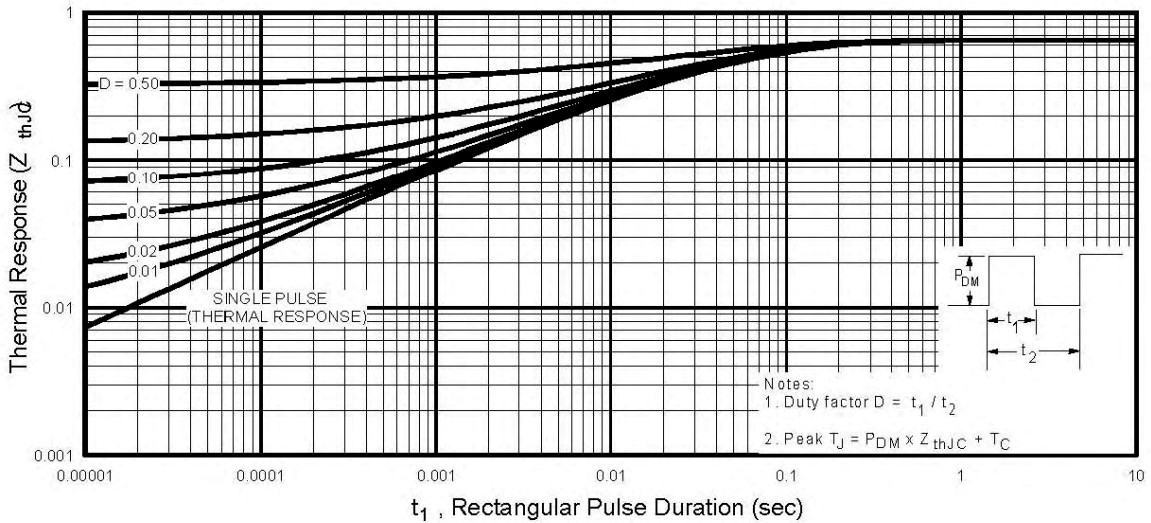


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

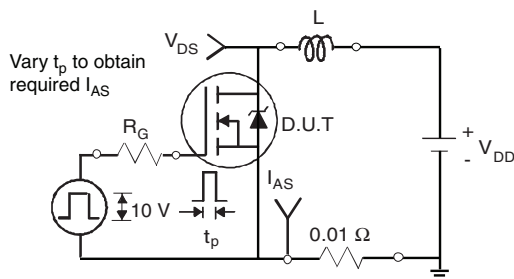


Fig. 12a - Unclamped Inductive Test Circuit

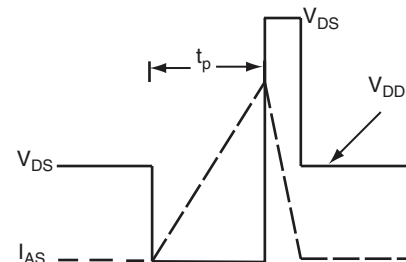


Fig. 12b - Unclamped Inductive Waveforms

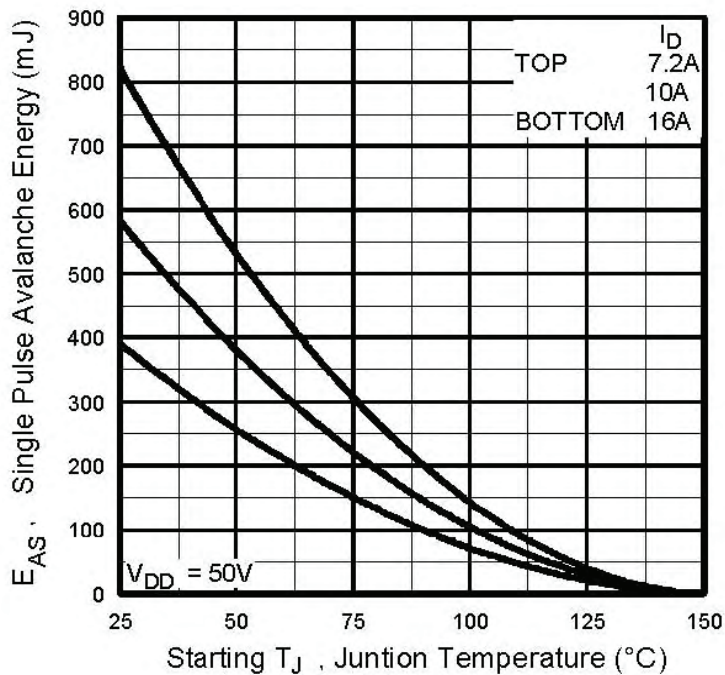


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

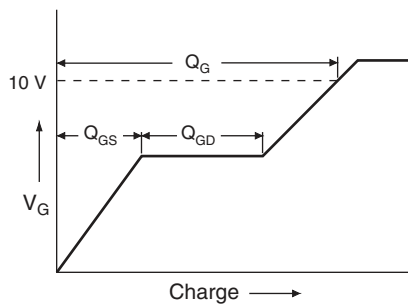


Fig. 13a - Basic Gate Charge Waveform

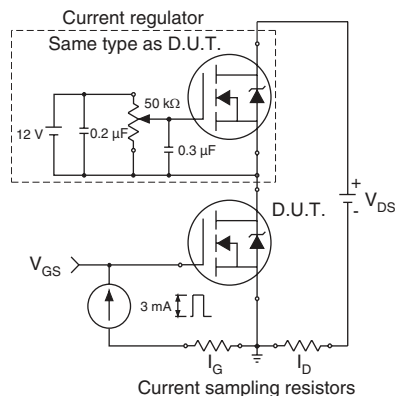
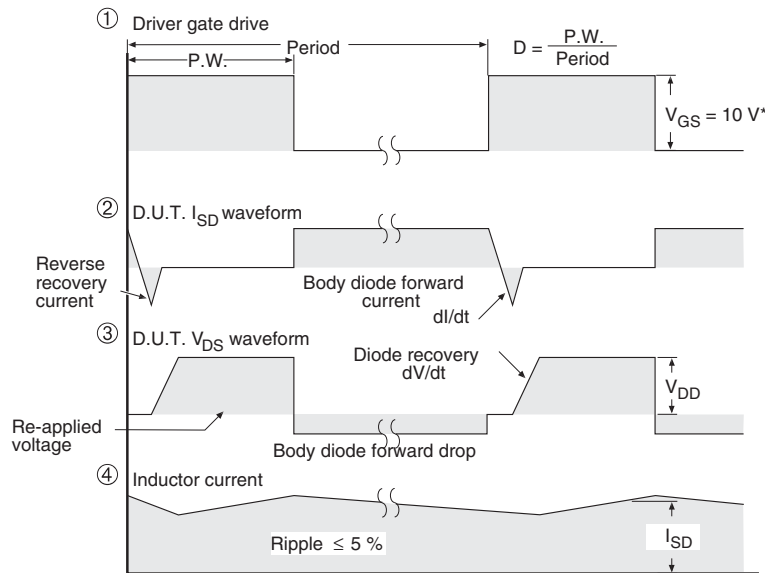
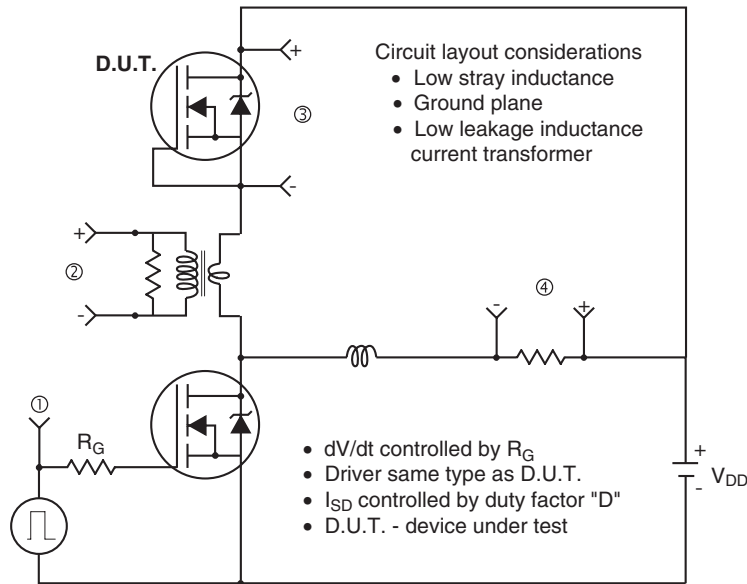


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Chsannel

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