18–40 GHz GaAs MMIC
Voltage Variable Attenuator

AV850M2-00

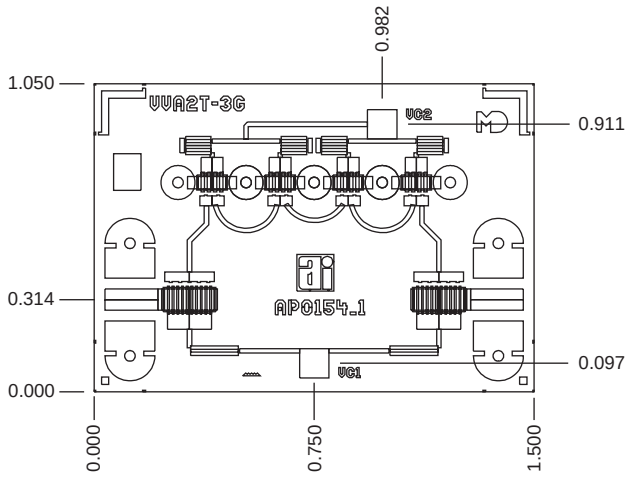
Features

- Dual Voltage Control
- 35 dB Attenuation Range
- Triple Gate 0.25 µm MESFET Design
- +10 dBm $P_{1\ dB}$ All Attenuation States
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

Description

Alpha's AV850M2-00 MMIC voltage variable attenuator is a standard TEE configuration incorporating triple-gate 0.25 µm power MESFETs. The attenuator has a typical insertion loss of 3 dB over the 18–40 GHz band. The attenuation range is 35 dB while typical I/P and O/P return loss is better than 6 dB. The chip uses Alpha's proven 0.25 µm MESFET technology and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The MMICs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate a conductive epoxy die attach process. This chip incorporates triple-gate FETs which results in less attenuation variation over temperature as well as better power handling performance at all attenuation states. All chips are screened for insertion loss, full attenuation and I/P and O/P match over the 18–40 GHz band for guaranteed performance.

Chip Outline



Dimensions indicated in mm.
All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.
Chip thickness = 0.1 mm.

Absolute Maximum Ratings

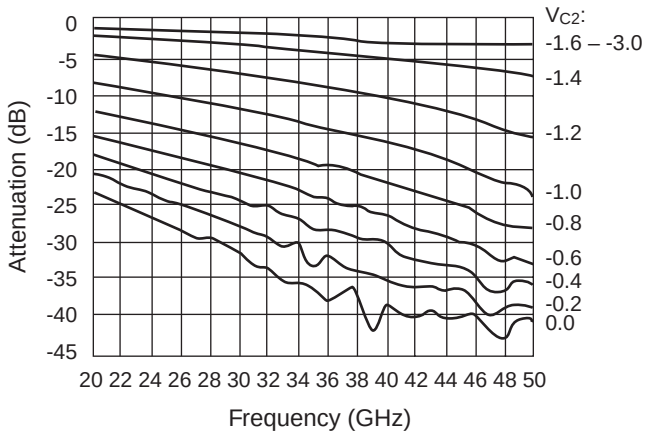
Characteristic	Value
Operating Temperature (T_C)	-55°C to +90°C
Storage Temperature (T_{ST})	-65°C to +150°C
Control Voltage (V_C)	-7 V_{DC}
Power In (P_{IN})	30 dBm
Junction Temperature (T_J)	175°C

Electrical Specifications at 25°C

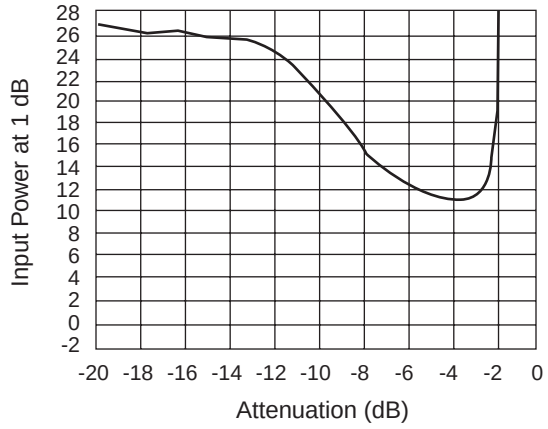
Parameter	Condition	Symbol	Min.	Typ.[2]	Max.	Unit
Maximum Attenuation	V_C = -1 V, V_{C2} = -0.25 V F = 18–35 GHz	ISO	20	30		dB
Minimum Attenuation	V_C = -1 V, V_{C2} = -3.25 V F = 18–35 GHz	I_L		2	3	dB
Input/Output Return Loss	F = 18–35 GHz	RL		-10	-6	dB
Maximum Attenuation	V_C = 0 V, V_{C2} = -0.8 V F = 35–40 GHz	ISO	20	35		dB
Minimum Attenuation	V_C = 0 V, V_{C2} = -3.25 V F = 35–40 GHz	I_L		3	4	dB
Input/Output Return Loss	F = 35–40 GHz	RL		-10	-5	dB
Input Power at 1 dB Compression (For All Attenuation Levels)[1]		$P_{1\ dB}$		10		dBm
Thermal Resistance		Θ_{JC}		101		°C/W

1. Not measured on a 100% basis.
2. Typical represents the median parameter value across the specified frequency range for the median chip.

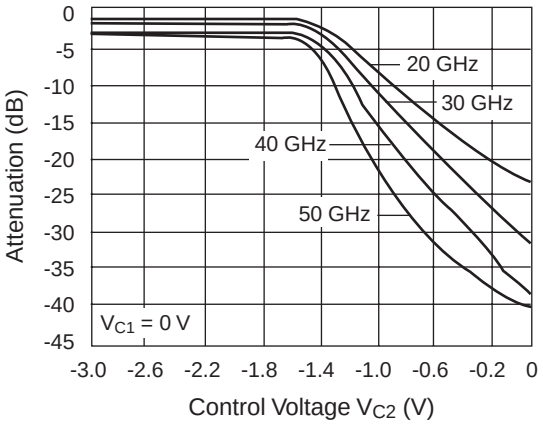
Typical Performance Data



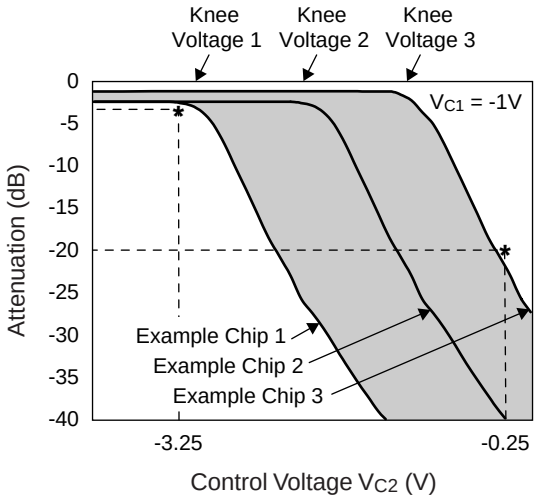
Attenuation vs. Frequency (V_{C1} = 0 V)



Attenuation vs. 1.0 dB Compression



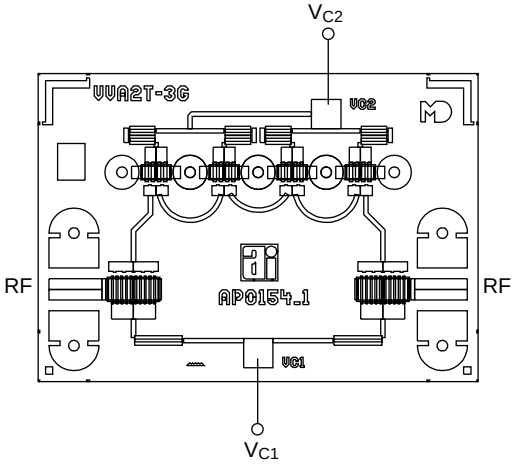
Attenuation vs. Control Voltage



Example Chip-to-Chip Variation for Any Single-Frequency of Operation (Low-Frequency Band)

* Asterisk in graph indicates guaranteed attenuation limits from the Electrical Specification table (knee voltage can vary from -3.25 V to approximately -1.0 V).

Bias Arrangement



V_{C1} controls the series devices, adjust for optimum VSWR.
V_{C2} controls the shunt devices, adjust to set attenuation.
Recommended Control Voltages:
For frequency 18–35 GHz: V_{C1} = -1 V, V_{C2} = -0.25 to -3.25 V.
For frequency 35–40 GHz: V_{C1} = 0 V, V_{C2} = -0.8 to -3.25 V.

Circuit Schematic