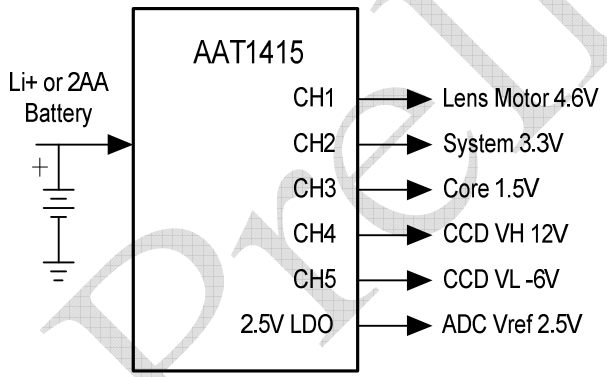
FIVE-CHANNEL DC-DC CONVERTER WITH A 2.5V LDO

FEATURES

- **Complete PWM Power Control Circuitry**
- **Input Voltage Range: 1.5 to 5.5V**
- **Low Start-Up Voltage: 1.2V**
- **Independent On / Off Control for All Channels**
- **Internal Soft-Start for All Channels**
- **Power-OK Outputs & Overload Protection**
- **Adjustable Operation Frequency with External Components Ranging from 100kHz to 1MHz**
- **VQFN-40 5*5 Package Available**

APPLICATIONS

- **Digital Still Cameras**
- **Digital Videos**
- **PDAs**
- **Portable Devices**

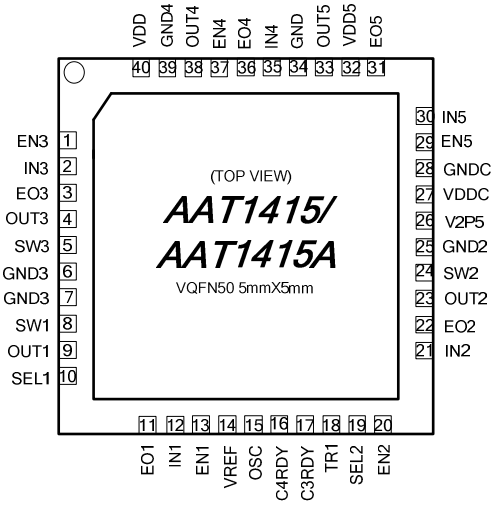


GENERAL DESCRIPTION

The AAT1415/AAT1415A provides an integrated 5-channel pulse-width-modulation (PWM) solution and a low noise LDO for the power supply of DC-DC converter. This device improves performance and size compared to conventional controllers in battery design. The AAT1415/AAT1415A has three current mode PWM converters (CH1, CH2, and CH3) and two voltage mode PWM converters (CH4 and CH5). Each current-mode channel has on-chip synchronous power FETs. The five channels include:

CH1: Boost /buck selectable DC-DC converter, which activates PWM function at 1.2V when it is configured as a boost converter.
CH2: Boost / buck selectable DC-DC converter.
CH3: Buck DC-DC converter.
CH4: Boost DC-DC controller for the CCD positive bias.
CH5: Inverting DC-DC controller for the CCD negative bias.

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1415	AAT1415 -Q8-T	Q8: VQFN 40-5*5	T: Tape and Reel	–40 °C to +85 °C	AAT1415 XXXXX XXXX	1. Part Name 2. Lot No. (6~9 Digits) 3. Date Code (4 Digits)
AAT1415A	AAT1415A -Q8-T	Q8: VQFN 40-5*5	T: Tape and Reel	–40 °C to +85 °C	AAT1415A XXXXX XXXX	1. Part Name 2. Lot No. (6~9 Digits) 3. Date Code (4 Digits)

NOTE: All AAT products are lead free and halogen free.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (VDD)	V_{MDD}	–0.3 to + 6.0	V
Pin Voltage 1 (OUT1, OUT2, VDDC, C3RDY, C4RDY, VDD5, SEL1, SEL2, TR1)	V_{I1}	–0.3 to + 6.0	V
Pin Voltage 2 (OUT3, VREF, OSC, EO_, EN_, IN_)	V_{I2}	–0.3 to (VDD + 0.3)	V
Pin Voltage 3 (OUT5)	V_{I3}	–0.3 to (VDD5 + 0.3)	V
Pin Voltage 4 (OUT4)	V_{I4}	–0.3 to (VDD + 0.3)	V
Pin Voltage 5 (V2P5)	V_{I5}	–0.3 to (VDDC + 0.3)	V
Pin Voltage 6 (GND_)	V_{I6}	– 0.3 to + 0.3	V
Input Voltage 7 (SW1)	V_{I7}	–0.3 to (OUT1 + 0.3V)	V
Input Voltage 8 (SW2)	V_{I8}	–0.3 to (OUT2 + 0.3V)	V
Input Voltage 9 (SW3)	V_{I9}	–0.3 to (OUT3 + 0.3V)	V
SW1 Current	I_{SW1}	3.6	A
SW2 Current	I_{SW2}	3.6	A
SW3 Current	I_{SW3}	3.6	A
Open Drain NMOS Current (C3RDY, C4RDY)	I_{OD}	10	mA
Operating Temperature Range	T_C	–40 °C to + 85 °C	°C
Storage Temperature Range	$T_{STORAGE}$	–65 °C to + 150 °C	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Free-Air Temperature	T_C	–40	+85	°C

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT1 = OUT2 = OUT3 = 3.6V, unless otherwise specified.)

General Item

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{VDD}		2.6		5.5	V
VDD Under-Voltage Lockout	V_{UVLO}		2.35	2.40	2.45	V
VDD Under-Voltage Lockout Hysteresis	V_{UHYS}			80		mV
CH1 Minimum Startup Voltage	V_{START}			1.2	1.5	V
Shutdown Supply Current Into VDD	I_{SHDN}			0.10	10.0	µA
Supply Current Into VDD with CH1 Enable	I_{CH1}	EN1 = 3.6V, IN1 = 1.5V		450	700	µA
Supply Current Into VDD with CH2 Enable	I_{CH2}	EN2 = 3.6V, IN2 = 1.5V		400	650	µA
Supply Current Into VDD with CH3 Enable	I_{CH3}	EN3 = 3.6V, IN3 = 1.5V		400	650	µA
Supply Current Into VDD with CH1 And CH4 Enable	I_{CH4}	EN1 = EN4 = 3.6V, IN1 = IN4 = 1.5V		550	800	µA
Supply Current Into VDD with CH1 And CH5 Enable	I_{CH5}	EN1 = EN5 = 3.6V, IN1 = 1.5V, IN5 = –0.5V		550	800	µA
Supply Current Into VDD with CH1 And LDO Enable	I_{CHC}	EN1 = 3.6V, IN1 = 1.5V		100	300	µA

Reference Voltage

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Output Voltage	V_{REF}	I_{REF} = 20µA	1.23	1.25	1.27	V
Reference Load Regulation		10µA < I_{REF} <200µA		4.50	10.0	%/mV
Reference Line Regulation		2.7V< V_{DD} <5.5V		1.3	5.0	%/mA

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT1 = OUT2 = OUT3 = 3.6V, unless otherwise specified.)

Oscillator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
OSC Discharge Trip Level	V_{ODT}	Rising Edge	1.225	1.250	1.275	V
OSC Discharge Resistance	R_{ODR}	OSC = 1.5V, I_{OSC} = 30mA		52	80	Ω
OSC Discharge Pulse Width	t_{OFF}			150		ns
OSC Frequency	f_{OSC}	R_{OSC} = 47kΩ, C_{OSC} = 100pF		500		kHz

Power Fail Latch and Thermal Protection

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
CH4, CH5 Overload Condition		Duty Cycle		100		%
CH1, CH2 Overload Threshold	V_{F12}	IN1, IN2, Fail Detection Voltage	1.07	1.10	1.13	V
CH3 Overload Threshold	V_{F13}	IN3 Fail Detection Voltage (AAT1415)	1.07	1.10	1.13	V
		IN3 Fail Detection Voltage (AAT1415A)	0.600	0.625	0.650	V
Overload Protection Fault Delay				100,000		Cycles
Thermal Shutdown	T_{SHDN}			160		°C
Thermal Hysteresis	T_{HYS}			20		°C

Logic Inputs

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
EN_, SEL_ Input Low Level	V_{IL}				0.4	V
EN_, SEL_ Input High Level	V_{IH}		1.4			V
SEL_ Input Leakage	I_{L9}			0.1	1.0	µA
EN_ Impedance to GND	R_{EN}		200	300	400	kΩ
TR1 Output Low Voltage	V_{TRL}	1.2mA Into TR1		0.1	0.2	V

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT1 = OUT2 = OUT3 = 3.6V, unless otherwise specified.)

CH1 (Boost / Buck)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN1 Regulation Voltage	V_{IN1}	IN1 = EO1	1.231	1.250	1.269	V
IN1 to EO1 Transconductance		IN1 = EO1		70		µS
CH1 Maximum Duty Cycle		Boost Mode (SEL1 = V_{DD})	85	90	95	%
		Buck Mode (SEL1 = GND)		100		%
IN1 Input Leakage Current	I_{L1}	IN1 = 0V to 1.5V	–100	0.01	+100	nA
Current-Sense Amplifier Transresistance		Boost Mode (SEL1 = V_{DD})		0.25		V/A
		Buck Mode (SEL1 = GND)		0.5		V/A
OUT1 Leakage Current	I_{LO1}	SEL1 = GND V_{SW1} = 0V, OUT1 = 3.6V		0.1	5.0	µA
SW1 Leakage Current	I_{LSW1}	SEL1 = GND V_{SW1} = OUT1 = 3.6V		0.1	5.0	µA
Switch On-Resistance	$R_{ON1(N)}$	N Channel		95		mΩ
	$R_{ON1(P)}$	P Channel		200		
SW1 Peak Current Limit	$I_{LIMIT1(N)}$	Boost Mode (SEL1 = V_{DD})		3		A
	$I_{LIMIT1(P)}$	Buck Mode (SEL1 = GND)		0.8		A
Soft-Start Interval				4,096		OSC Cycles
OUT1 Startup-to-Normal Operating Threshold	V_{UVLO1}	Rising Edge	2.30	2.50	2.65	V
OUT1 Startup-to-Normal Operating Hysteresis	V_{UHYS1}			80		mV
Startup t_{OFF}	t_{OS}	V_{DD} = 1.8V		700		ns
Startup Frequency	f_{START}	V_{DD} = 1.8V		200		kHz

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT2 = 3.6V, unless otherwise specified.)

CH2 (Boost / Buck)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN2 Regulation Voltage	V_{IN2}	IN2 = EO2	1.231	1.250	1.269	V
IN2 to EO2 Transconductance		IN2 = EO2		70		µS
CH2 Maximum Duty Cycle		Boost Mode (SEL2 = V_{DD})	85	90	95	%
		Buck Mode (SEL2 = GND)		100		%
IN2 Input Leakage Current	I_{L2}	IN2 = 0V to 1.5V	–100	0.01	+100	nA
Current-Sense Amplifier Transresistance		Boost Mode (SEL2 = V_{DD})		0.25		V/A
		Buck Mode (SEL2 = GND)		0.5		V/A
OUT2 Leakage Current	I_{LO2}	V_{SW2} = 0V, OUT2 = 3.6V		0.1	5.0	µA
SW2 Leakage Current	I_{LSW2}	V_{SW2} = OUT2 = 3.6V		0.1	5.0	µA
Switch On-Resistance	$R_{ON2(N)}$	N Channel		95		mΩ
	$R_{ON2(P)}$	P Channel		150		
SW2 Peak Current Limit	$I_{LIMIT2(N)}$	Boost Mode (SEL2 = V_{DD})		3		A
	$I_{LIMIT2(P)}$	Buck Mode (SEL2 = GND)		0.8		A
Soft-Start Interval				4,096		OSC Cycles
OUT2 Under-Voltage Lockout in Buck Mode	V_{UVLO2}	SEL2 = GND	2.45	2.50	2.55	V
OUT2 Under-Voltage Lockout in Hysteresis	V_{UHYS2}			80		mV

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT3 = 3.6V, unless otherwise specified.)

CH3 (Buck)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN3 Regulation Voltage	V_{IN3}	IN3 = EO3 (AAT1415)	1.231	1.250	1.269	V
		IN3 = EO3 (AAT1415A)	0.784	0.800	0.816	
IN3 to EO3 Transconductance		IN3 = EO3		70		µS
CH3 Maximum Duty Cycle				100		%
IN3 Input Leakage Current	I_{L3}	IN3 = 0V to 1.5V	–100	0.01	+100	nA
Current-Sense Amplifier Transresistance				0.5		V/A
SW3 Leakage Current	I_{LSW3}	V_{SW3} = 0V to 3.6V		0.1	5.0	µA
Switch On-Resistance	$R_{ON3(N)}$	N Channel		95		mΩ
	$R_{ON3(P)}$	P Channel		150		
SW3 Current Limit	I_{LIMIT3}			0.8		A
Soft-Start Interval				4,096		OSC Cycles
SW3 Peak Current Limit	$I_{LIMIT3(N)}$			0.8		A
Soft-Start Interval				2,048		OSC Cycles
C3RDY Output Low Voltage	V_{C3RDY}	0.1mA Into C3RDY		0.01	0.10	V
C3RDY Leakage Current	I_{C3RDY}	EN3 = GND		0.01	1.00	µA

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT3 = 3.6V, unless otherwise specified.)

CH4 (Buck)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN4 Regulation Voltage	V_{IN4}	IN4 = EO4	1.231	1.250	1.269	V
IN4 to EO4 Transconductance		IN4 = EO4		70		µS
CH4 Maximum Duty Cycle		IN4 = 0V	85	90	95	%
IN4 Input Leakage Current	I_{L4}	IN4 = 0V to 1.5V	–100	0.01	+100	nA
OUT4 Driver Resistance	$R_{ON4(N)}$	I_{OUT4} = 10mA		5		Ω
	$R_{ON4(P)}$	I_{OUT4} = –10mA		5		Ω
Soft-Start Interval				4,096		OSC Cycles
C4RDY Output Low Voltage	V_{C4RDY}	0.1mA Into C4RDY		0.01	0.10	V
C4RDY Leakage Current	I_{C4RDY}	EN4 = GND		0.01	1.00	µA

ELECTRICAL CHARACTERISTICS

(T_C = 25°C , V_{DD} = OUT1 = 3.6V, unless otherwise specified.)

CH5

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN5 Regulation Voltage	V_{IN5}		–0.01	0.00	+0.01	V
IN5 to EO5 Transconductance				70		µS
Maximum Duty Cycle		IN5 = 0V	85	90	95	%
IN5 Input Leakage Current	I_{L5}	IN5 = 0V to 0.5V	–100	0.1	+100	nA
OUT5 Driver Resistance	$R_{ON5(N)}$	I_{OUT5} = 10mA		5		Ω
	$R_{ON5(P)}$	I_{OUT5} = –10mA		5		Ω
Soft-Start Interval				4,096		OSC Cycles
VDD5 Under-Voltage Lockout Threshold	V_{UVLO5}	Rising Edge	2.30	2.50	2.65	V
VDD5 Under-Voltage Lockout Hysteresis	V_{UHYS5}			80		mV

ELECTRICAL CHARACTERISTICS

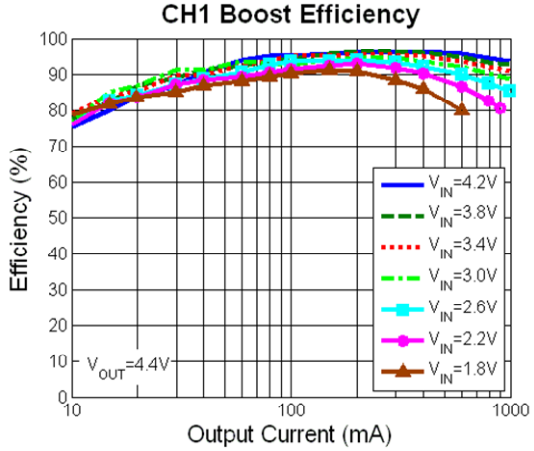
(T_C = 25°C , V_{DD} = VDDC = 3.6V, unless otherwise specified.)

2.5V LDO

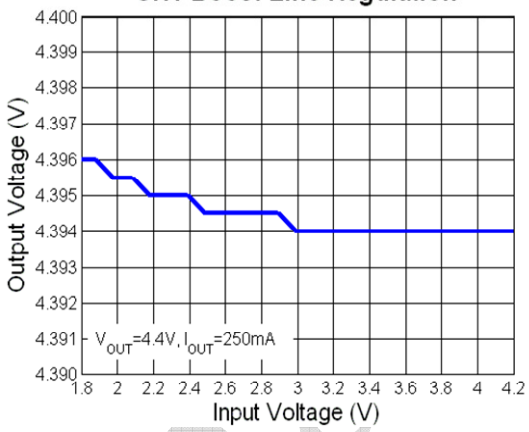
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{VDDC}	I_{V2P5} = 10mA	2.6		5.5	V
V2P5 Regulation Voltage	V_{V2P5}	I_{V2P5} = 10mA	2.45	2.50	2.55	V
V2P5 Dropout Voltage	V_{DROP25}	I_{V2P5} = 10mA			50	mV
V2P5 LDO Output Current	V_{V2P5}		100			mA
V2P5 LDO Output Current Limit	I_{LIMC25}			150		mA
V2P5 VDDC PSRR				60		dB
V2P5 Line Regulation		Measure V_{V2P5} V_{VDDC} = 2.6V ~ 5V			10	%/mV
V2P5 Load Regulation		Measure V_{V2P5} I_{V2P5} = 5mA ~ 100mA			5	%/mA

TYPICAL OPERATING CHARACTERISTICS

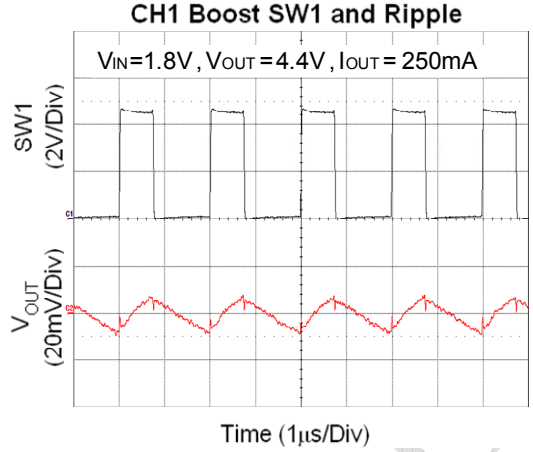
CH1 Boost Efficiency



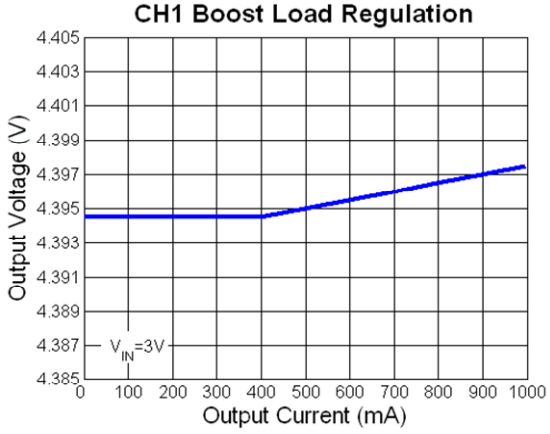
CH1 Boost Line Regulation



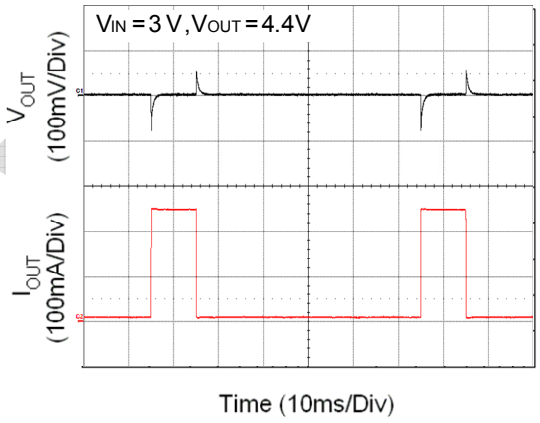
CH1 Boost SW1 and Ripple



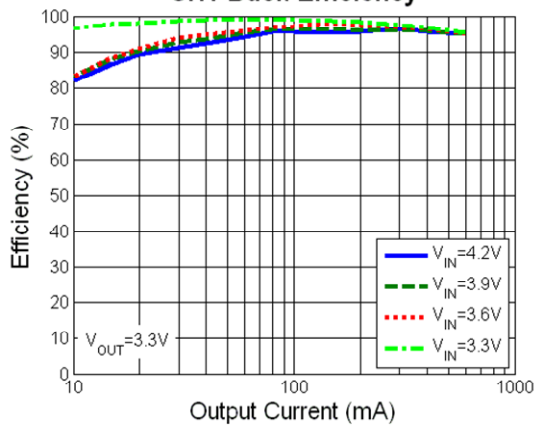
CH1 Boost Load Regulation



CH1 Boost Load Transient Response

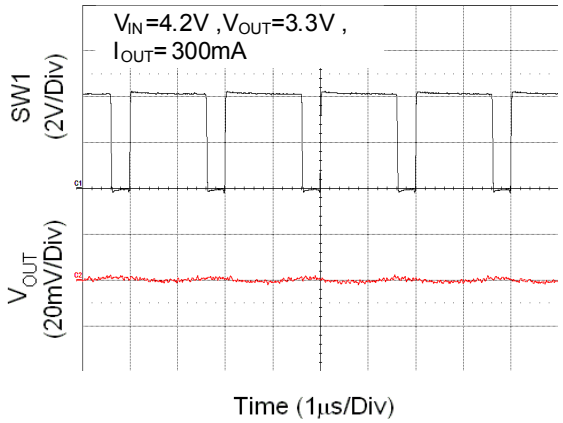


CH1 Buck Efficiency

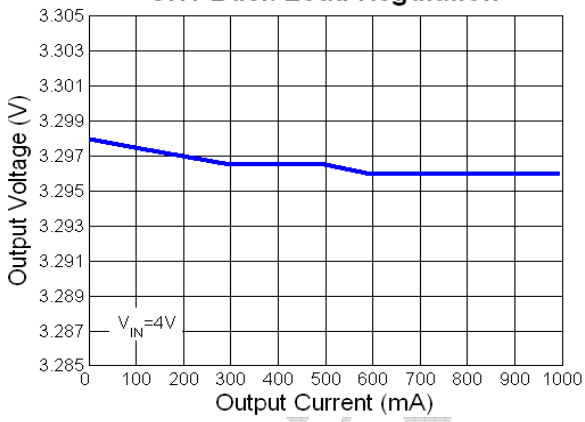


TYPICAL OPERATING CHARACTERISTICS

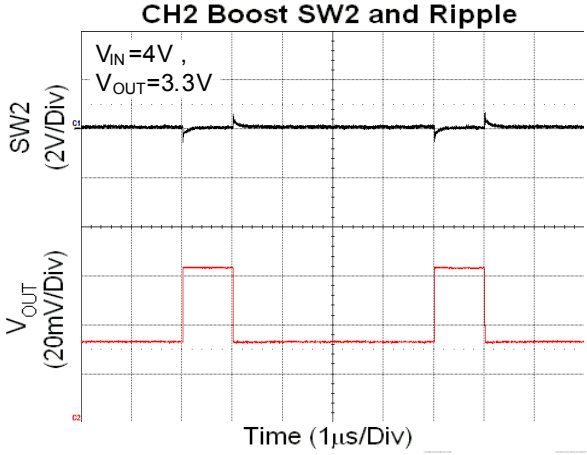
CH1 Buck SW1 and Ripple



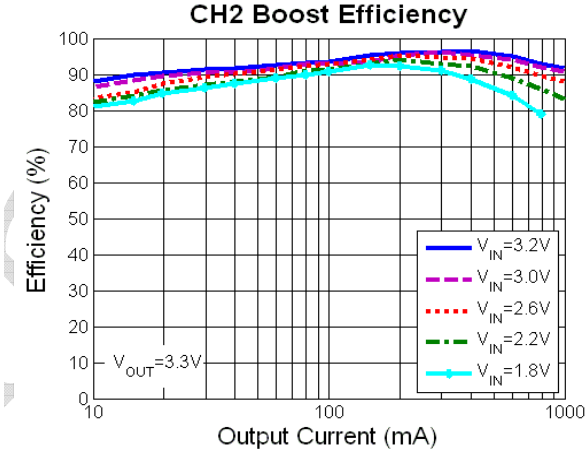
CH1 Buck Load Regulation



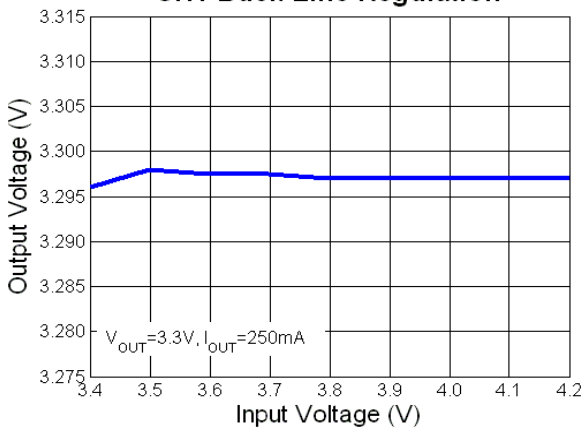
CH2 Boost SW2 and Ripple



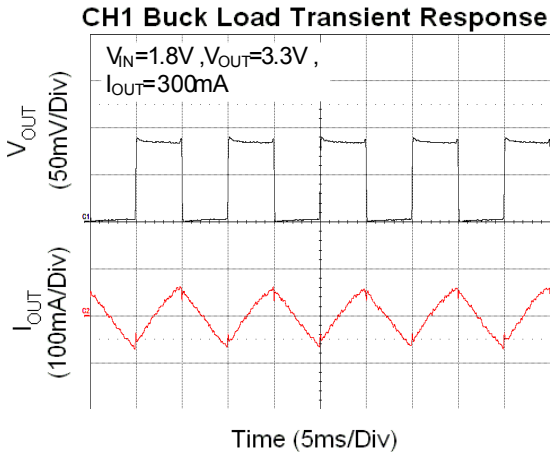
CH2 Boost Efficiency



CH1 Buck Line Regulation

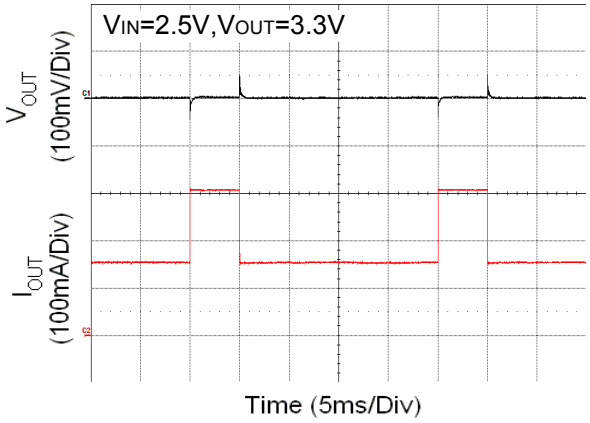


CH1 Buck Load Transient Response

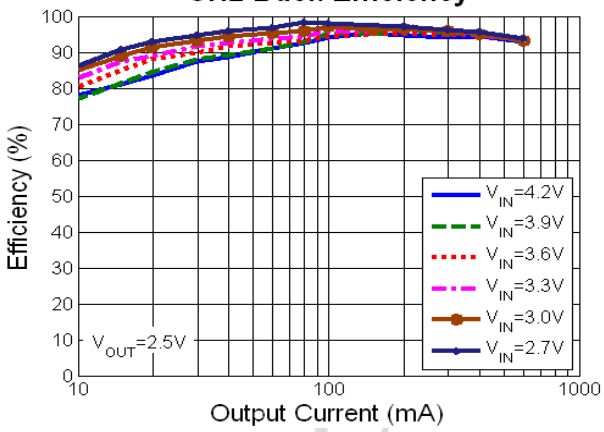


TYPICAL OPERATING CHARACTERISTICS

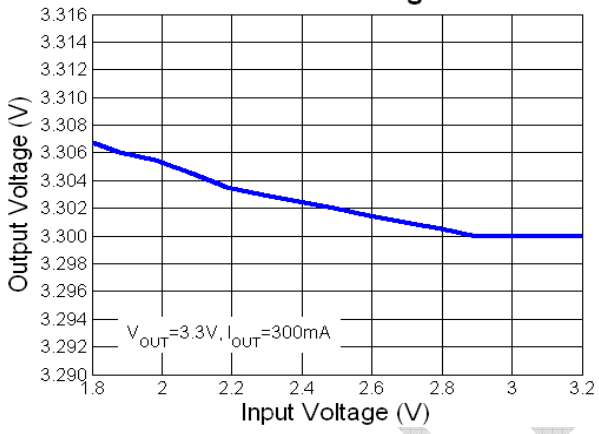
CH2 Boost Load Transient Response



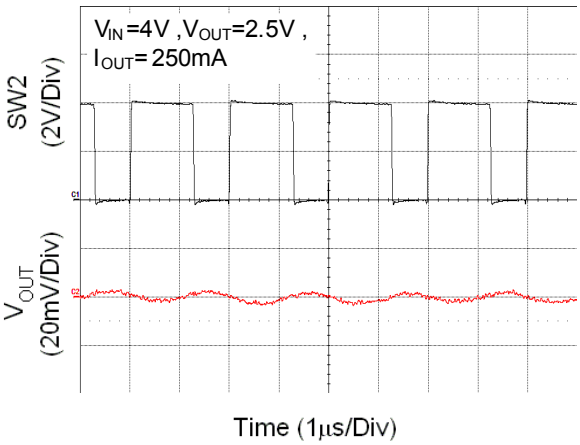
CH2 Buck Efficiency



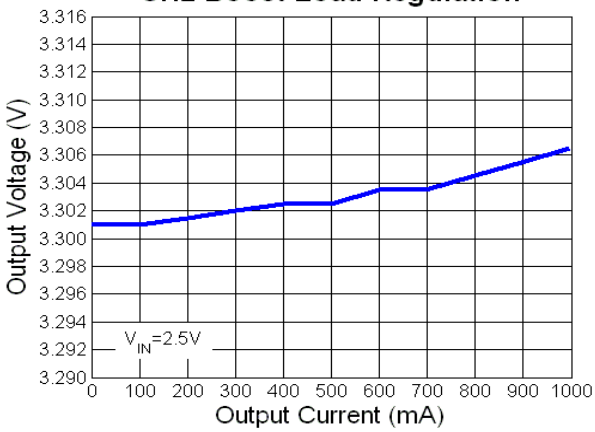
CH2 Boost Line Regulation



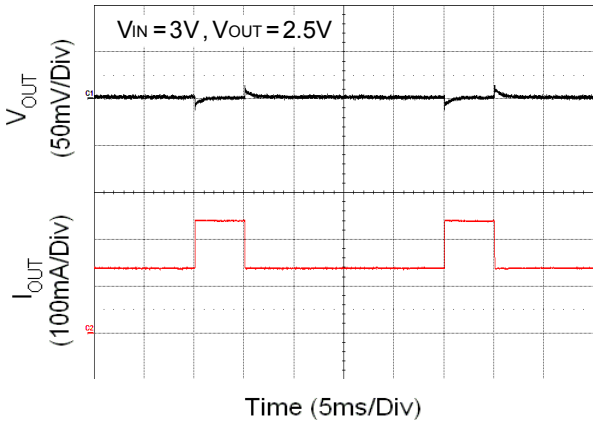
CH2 Buck SW2 and Ripple



CH2 Boost Load Regulation

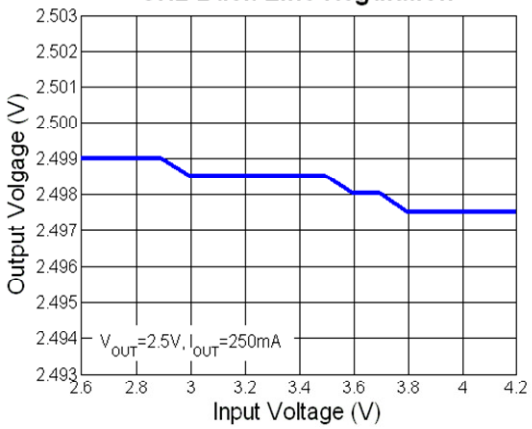


CH2 Buck Load Transient Response

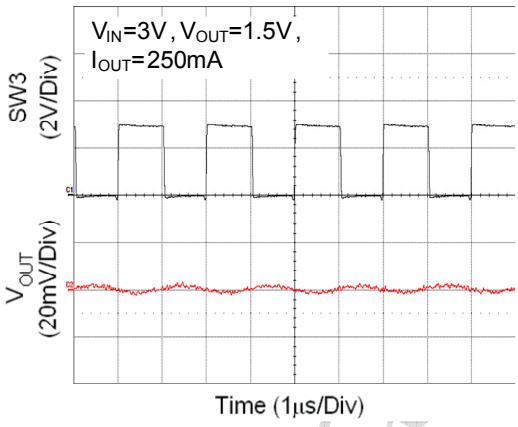


TYPICAL OPERATING CHARACTERISTICS

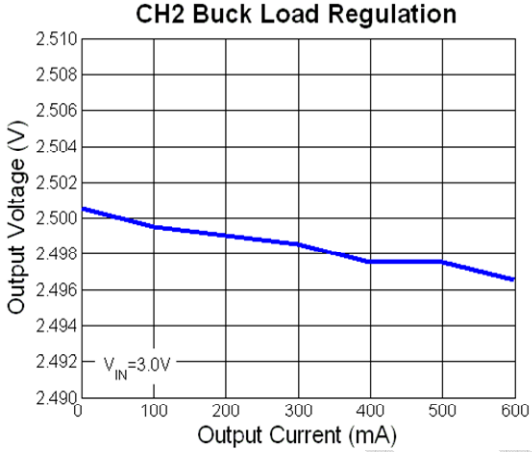
CH2 Buck Line Regulation



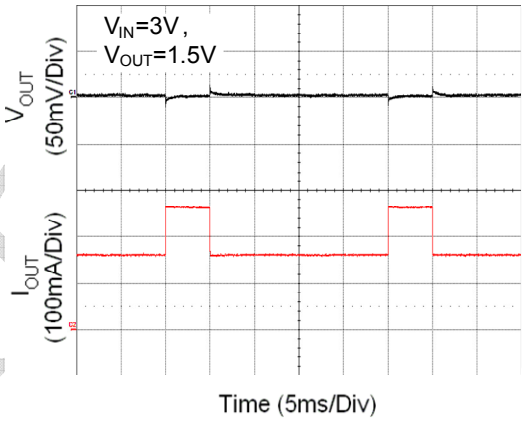
CH3 Buck SW3 and Ripple



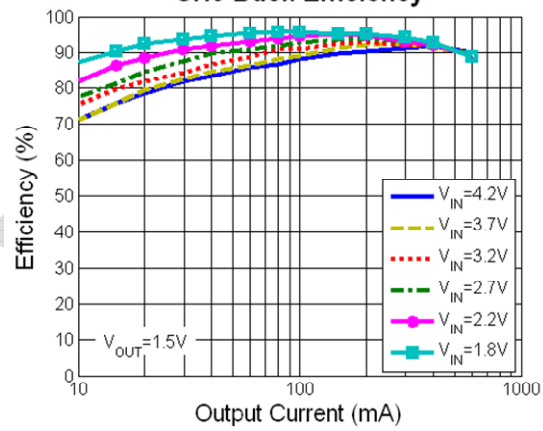
CH2 Buck Load Regulation



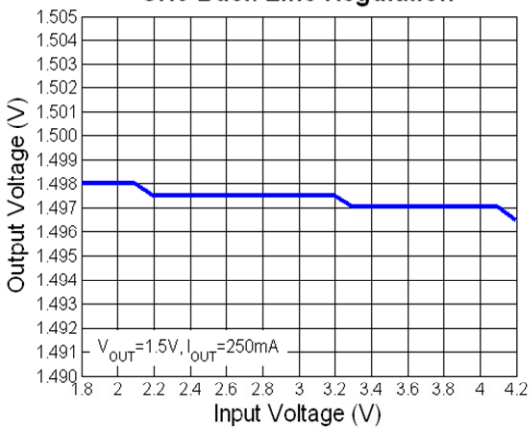
CH3 Buck Load Transient Response



CH3 Buck Efficiency

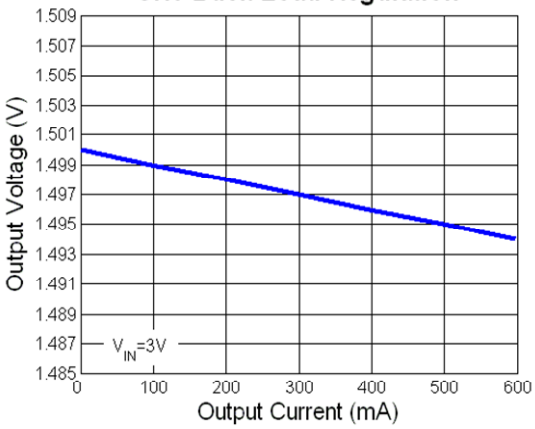


CH3 Buck Line Regulation

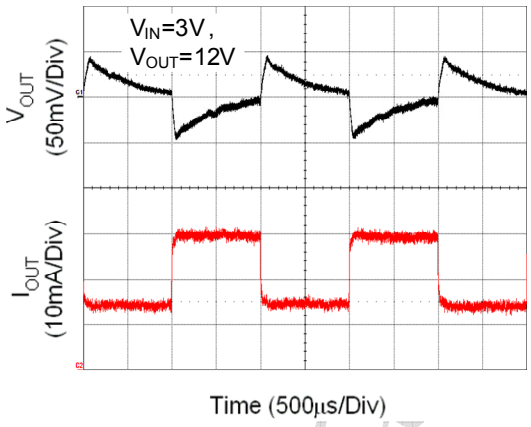


TYPICAL OPERATING CHARACTERISTICS

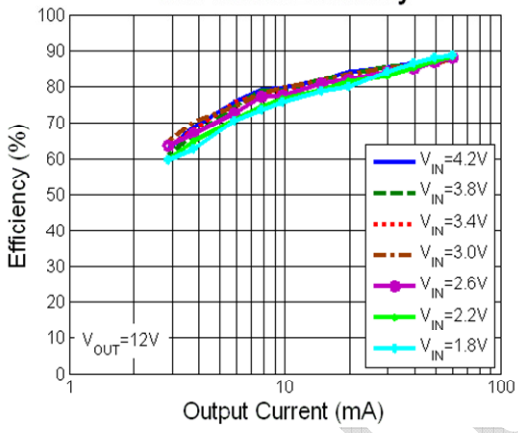
CH3 Buck Load Regulation



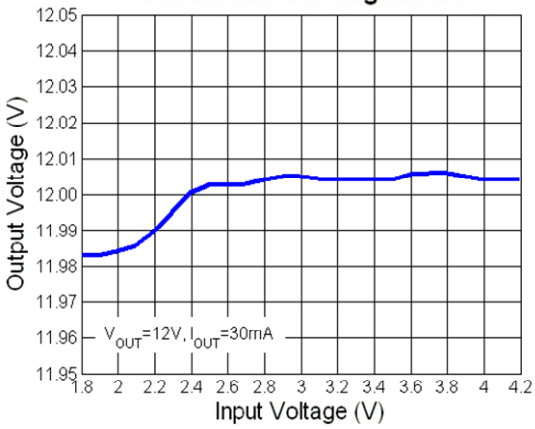
CH4 Boost Load Transient Response



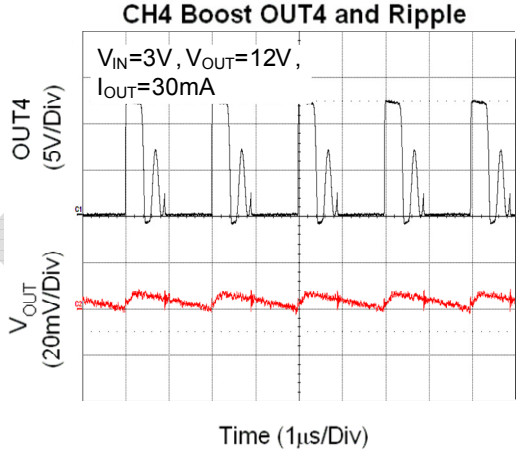
CH4 Boost Efficiency



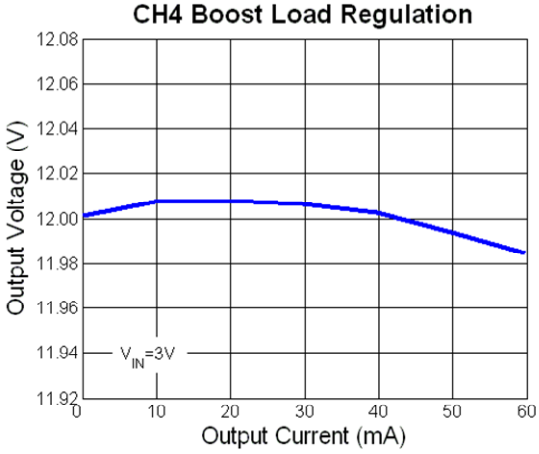
CH4 Boost Line Regulation



CH4 Boost OUT4 and Ripple

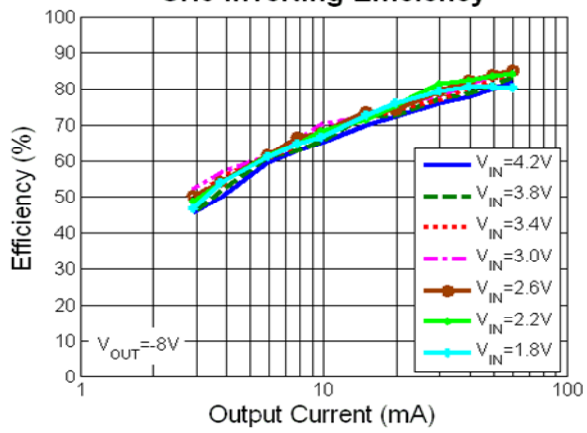


CH4 Boost Load Regulation

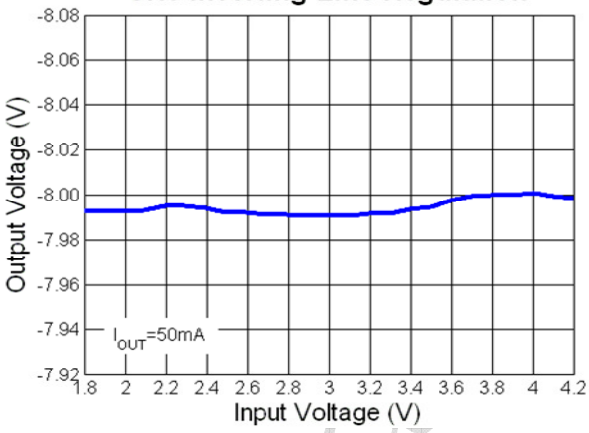


TYPICAL OPERATING CHARACTERISTICS

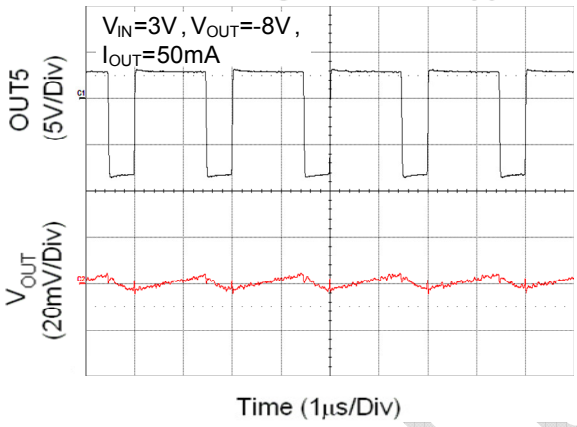
CH5 Inverting Efficiency



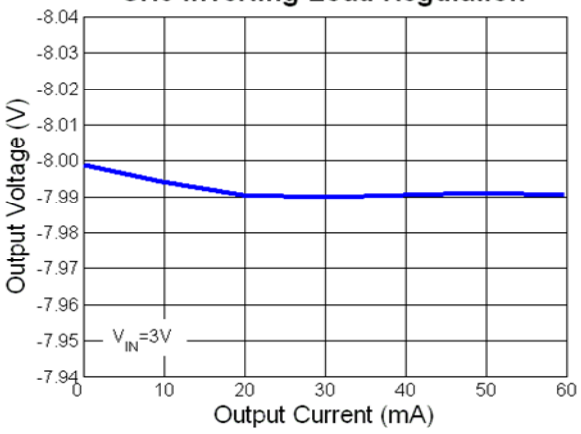
CH5 Inverting Line Regulation



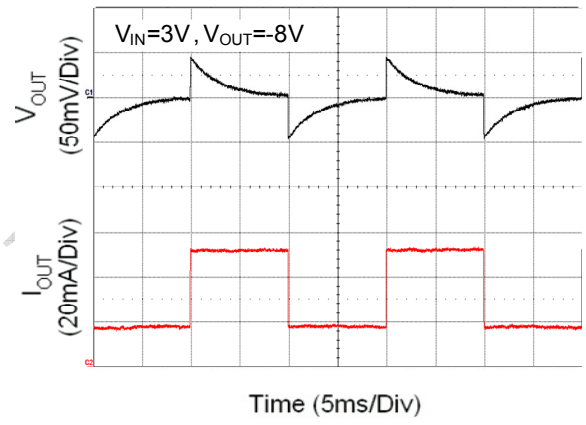
CH5 Inverting OUT5 and Ripple



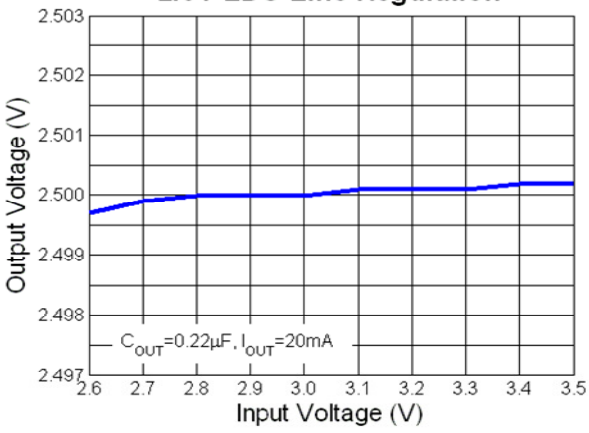
CH5 Inverting Load Regulation



CH5 Inverting Load Transient Response



2.5V LDO Line Regulation

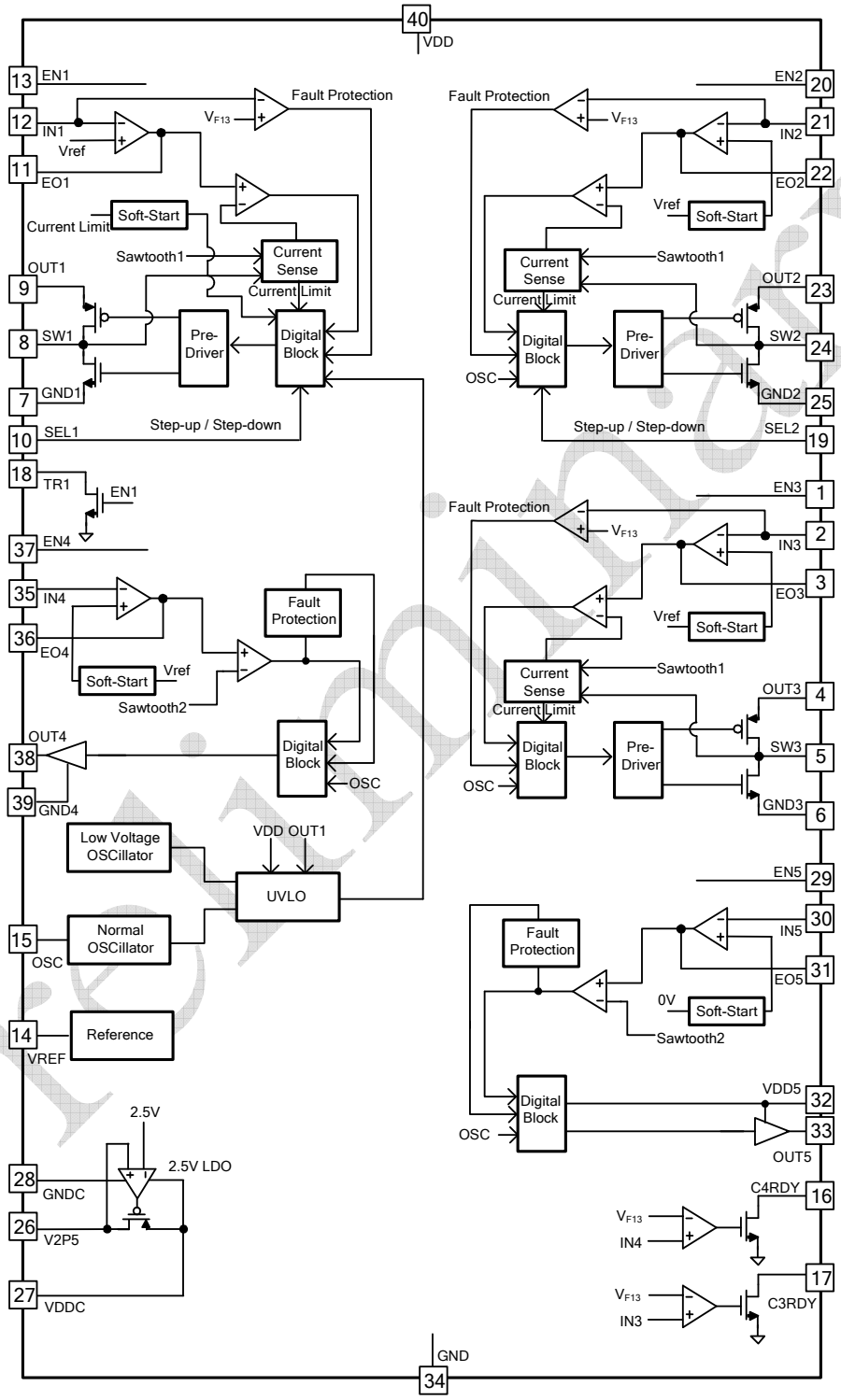


PIN DESCRIPTION

PIN NO	NAME	I/O	FUNCTION
1	EN3	I	ON/OFF Control for CH3
2	IN3	I	CH3 Feedback Input
3	EO3	I/O	CH3 Compensation Node
4	OUT3	I	CH3 Switching Power Input
5	SW3	I/O	CH3 Switching Node
6	GND3	-	CH3 Power Ground
7	GND1	-	CH1 Power Ground
8	SW1	I/O	CH1 Switching Node
9	OUT1	I/O	Switching Power Input (Boost) / Output (Buck) of CH1
10	SEL1	I	Configures CH1 as a Buck or a Boost Converter
11	EO1	I/O	CH1 Compensation Node
12	IN1	I	CH1 Feedback Input
13	EN1	I	ON/OFF Control for CH1
14	VREF	O	Reference Output
15	OSC	I/O	Oscillator Control
16	C4RDY	O	Power-Ok Signal for CH4
17	C3RDY	O	Power-Ok Signal for CH3
18	TR1	I/O	CH1 Feedback Resistor Truly Shutdown Input
19	SEL2	I	Configures CH2 as a Buck or a Boost Converter
20	EN2	I	ON/OFF Control for CH2
21	IN2	I	CH2 Feedback Input
22	EO2	I/O	CH2 Compensation Node
23	OUT2	I	CH2 Switching Power Input
24	SW2	I/O	CH2 Switching Node
25	GND2	-	CH2 Power Ground
26	V2P5	O	2.5V LDO Output
27	VDDC	I	LDO Power Input

28	GNDC	-	LDO Ground
29	EN5	I	ON/OFF Control for CH5
30	IN5	I	CH5 Feedback Input
31	EO5	I/O	CH5 Compensation Node
32	VDD5	I	CH5 Power Source
33	OUT5	O	CH5 Gate-Drive Output
34	GND	-	Internal Circuit Ground
35	IN4	I	CH4 Feedback Input
36	EO4	I/O	CH4 Compensation Node
37	EN4	I	ON/OFF Control for CH4
38	OUT4	I/O	CH4 Gate-Drive Output
39	GND4	-	CH4 Power Ground
40	VDD	I	Internal Circuit Power Source

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT

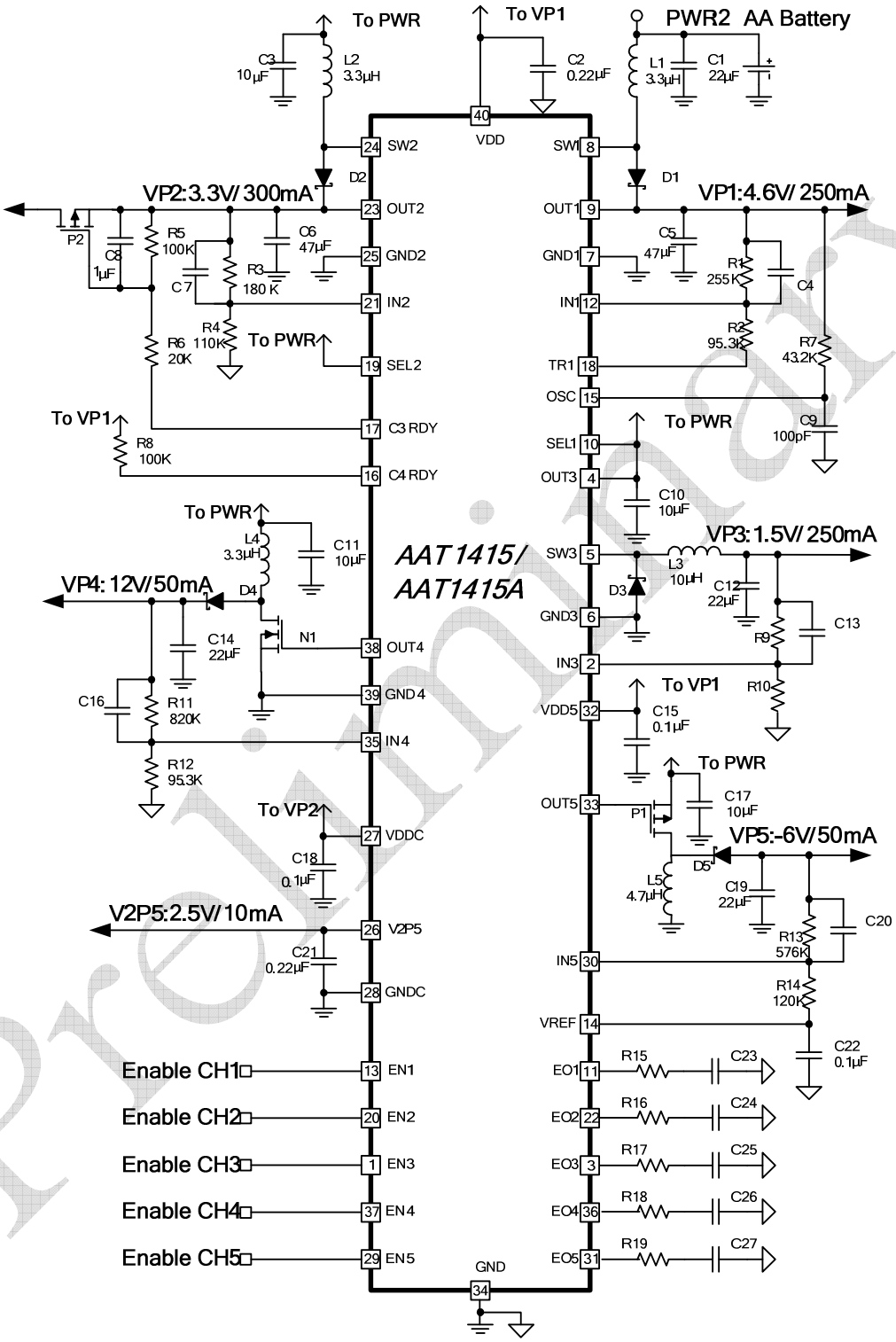


Figure 1. Typical 2-Cell AA-Powered System

TYPICAL APPLICATION CIRCUIT

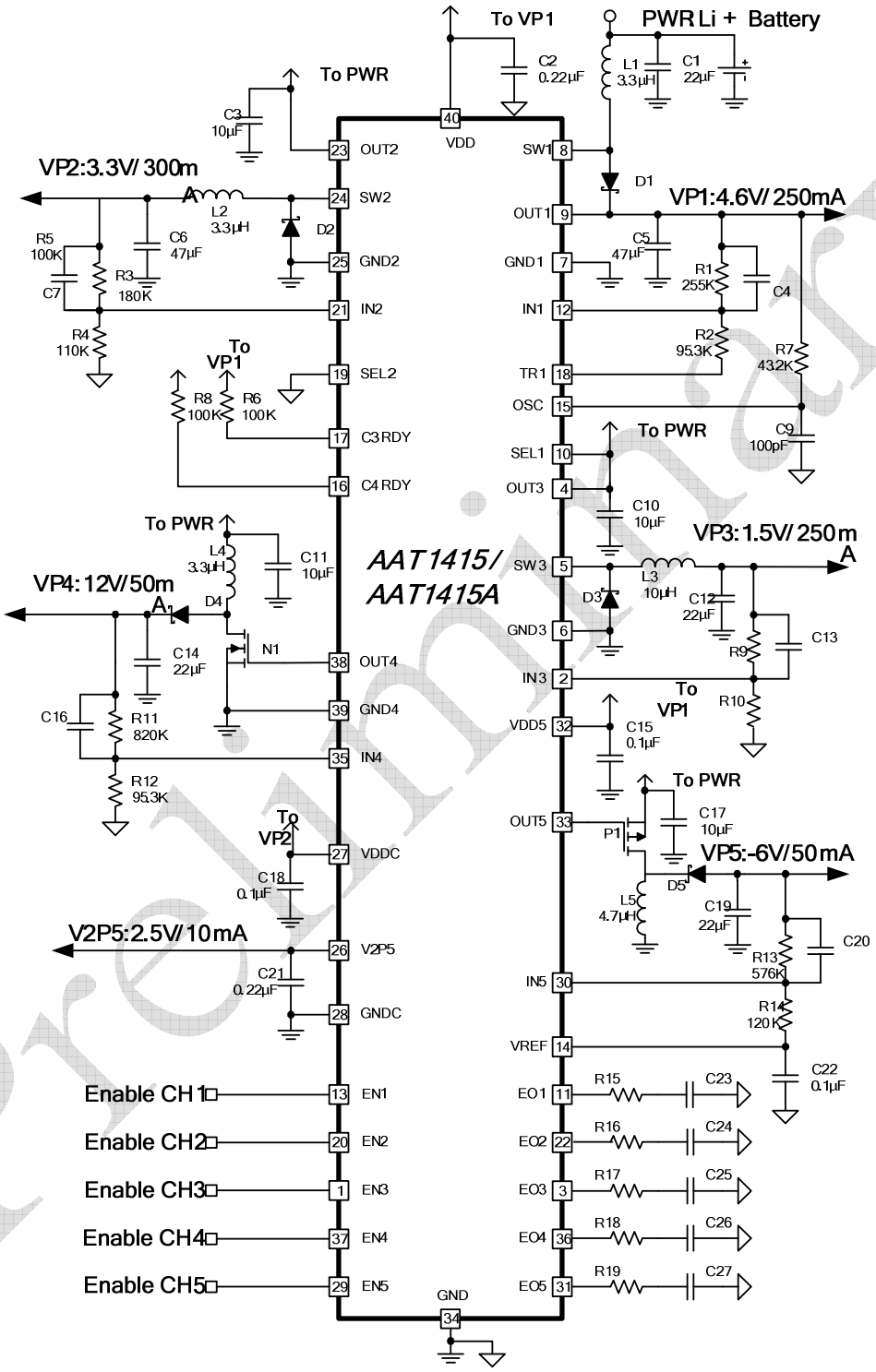


Figure 2. Typical 1-Cell Li+ Powered System (For CCD)

TYPICAL APPLICATION CIRCUIT

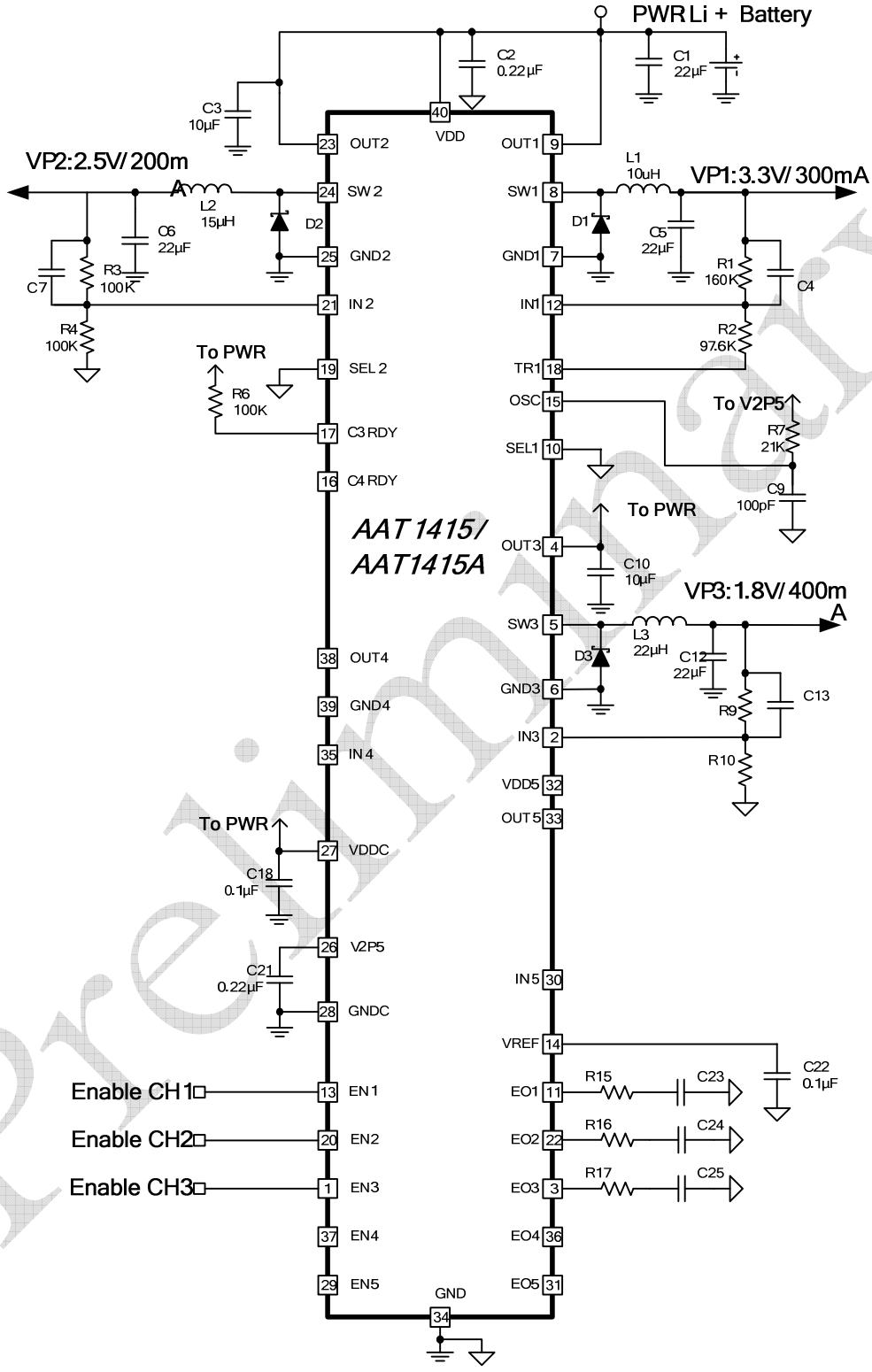


Figure 3. Typical 1-Cell Li+ Powered System (For CMOS)

DETAILED DESCRIPTION

The AAT1415/AAT1415A is a complete power-conversion IC for digital still cameras. It can accept input from a variety of sources, including single-cell Li+ batteries and 2-cell alkaline or NiMH batteries. The AAT1415/AAT1415A includes five DC-DC converter channels and a 2.5V LDO to generate all required voltages:

- Synchronous-rectified boost or buck DC-DC converter with on-chip MOSFETs—Typically supplies 4.6V for lens motor or 3.3V for main system power.
- Synchronous-rectified boost or Buck DC-DC converter with on-chip MOSFETs— Typically supplies 3.3V for main system power or 2.5V for DDR.
- Synchronous-rectified buck DC-DC converter with on-chip MOSFETs— Typically supplies 1.5V for the DSP core.
- Boost controller— Typically used for positive voltage to bias one or more of the LCD, CCD, and LED backlights.
- Inverter controller— Typically supplies negative CCD bias when high current is needed for large pixel-count CCDs.
- 2.5V LDO— Typically supplies 2.5V for analog-to-digital converter's reference voltage.

The AAT1415/AAT1415A includes three versatile status outputs that can provide information to the system. All are open-drain outputs and can directly drive MOSFET switches to facilitate sequencing, disconnect loads during overloads, or perform other hardware-based functions.

TR1

TR1 pulls low when EN1 pulls high. A typical use for TR1 is to reduce CH1 boost feedback network's leakage current when CH1 is disabled (Figure 1).

C3RDY

C3RDY pulls low when IN3 reaches V_{F13} (1.1V typ). C3RDY goes high impedance in shutdown, overload, and thermal limit when IN3 is under V_{F13}. A typical use for C3RDY is to enable 3.3V power to the CPU I/O after the CPU core is powered up (Figure 1), thus providing safe sequencing in hardware without system intervention.

C4RDY

C4RDY pulls low when IN4 reaches V_{F13} (1.1V typ). C4RDY goes high impedance in shutdown, overload, and thermal limit when IN4 is under V_{F13}. A typical use for C4RDY is to drive a PMOS that gates 5V power to the CCD until the VH CCD bias (generated by CH4) is powered up (Figure 4).

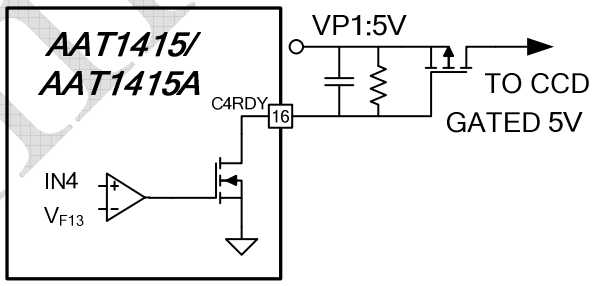


Figure 4. C4RDY Application Circuit

Soft-Start

The AAT1415/AAT1415A channels feature a soft-start function that limits inrush current and prevent excessive battery loading at startup by ramping the output voltage of each channel up to the regulation voltage.

This is accomplished by ramping the internal reference inputs to mostly channel error amplifier from 0V to the 1.25V reference voltage (CH5 from 1.25V to 0V) over a period of 4,096 oscillator cycles (16ms at 500kHz) when initial power is applied or when a channel is enabled. Soft-start of CH1 is different from others in order to avoid limiting startup capability with loading.

See Figure 6. soft-start mechanism. CH3 soft-start ramp takes half the time (2,048 clock cycles) of the other channel ramps. This allows the CH3 and CH2 output (when set to 3.3V) to track each other and rise at nearly the same dV/dt rate on power-up. Once the step-down output reaches its regulation point (1.5V or 1.8V typ), the CH2 output (3.3V typ) continues to rise at the same ramp rate. See Figure 7 timing chart of soft-start.

2.5V LDO

The 2.5V LDO regulates the VDDC voltages when the reference voltage (VREF) is ready and VDDC voltage is greater than 2.5V.

Fault Protection

If any DC-DC converter channel remains faulted for 100,000 clock cycles (200ms at 500kHz), then all outputs latch off until the AAT1415/AAT1415A is reinitialized or by cycling the input power. The fault-detection circuitry for any channel is disabled during its initial turn-on soft-start sequence. An exception to the standard fault behavior is that there is no 100,000 clock-cycle delay in entering the fault state if the OUT1 pin is dragged below its 2.5V UVLO1 threshold or is shorted. The UVLO1 immediately triggers and shuts down all channels. The CH1 then continues to attempt to start. If the CH1 output short remains, these attempts do not succeed since OUT1 remains near ground. If a soft-short or overload remains on OUT1, the startup oscillator switches the internal NMOS, but fault is retriggered if regulation is not achieved by the end of the soft-start interval. If OUT1 is dragged below the input, the overload is supplied by the body diode of the internal synchronous rectifier or by a Schottky diode connected from the battery to OUT1.

Reference

Connect a 0.1µF ceramic bypass capacitor from VREF to GND. VREF is enabled when EN1, EN2 or EN3 is high. The AAT1415/AAT1415A has internal 1.250V references.

Oscillator

The AAT1415/AAT1415A operating frequency is set by an RC network (R_{OSC}, C_{OSC}) at the OSC pin. The range of usable settings is 100kHz to 1MHz. The oscillation frequency changes as the forced voltage (V_{osc}) ramps upward following startup. The oscillation frequency is then constant once the main output is in regulation. At the beginning of a cycle, the timing capacitor charge through the resistor until it reaches VREF. The charge time, t_1, is as follows:

$$t_1 \approx -R_{OSC} \times C_{OSC} \times \ln\left(1 - \frac{1.25}{V_{OSC}}\right)$$

The capacitor voltage then decays to zero over time $t_2 \approx 150ns$. Choose C_{OSC} between 47pF and 330pF. Determine R_{OSC} and V_{OSC}. The oscillator frequency is as follows:

$$f_{OSC} \approx \frac{1}{t_1 + t_2}$$

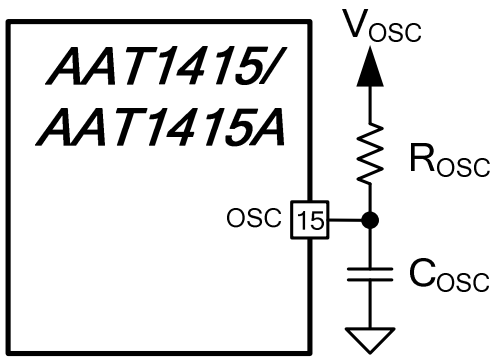


Figure 5. Oscillator Circuit

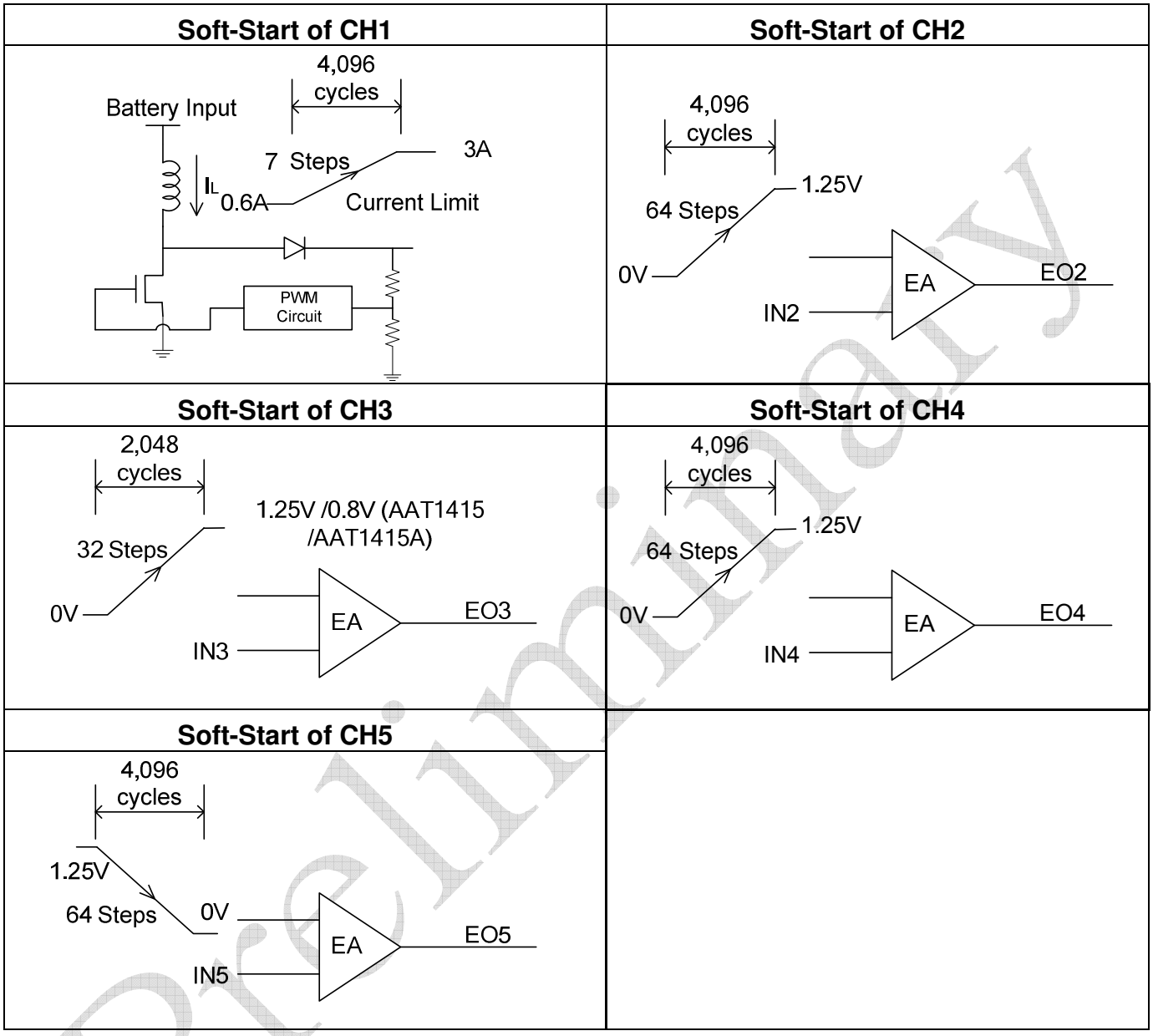


Figure 6. Soft-Start Mechanism

Soft Start Waveform

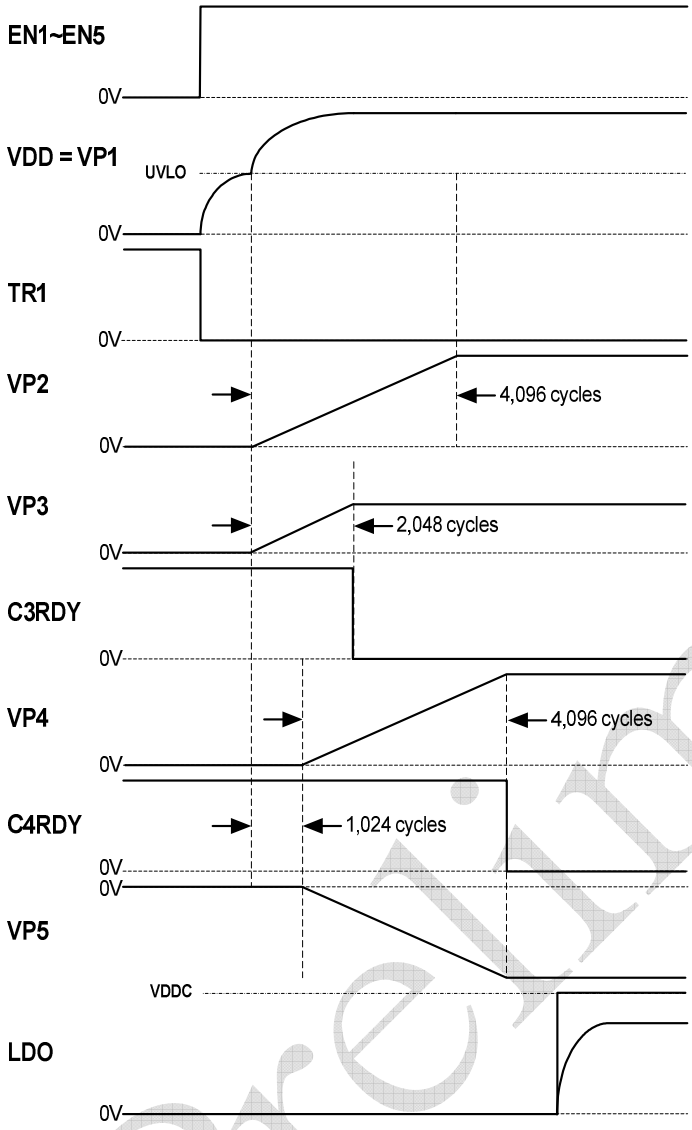


Figure 7. Timing Chart of Soft-Start

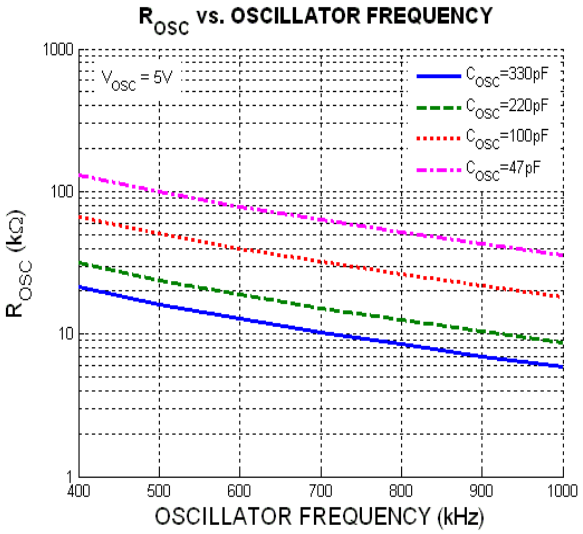


Figure 8. Oscillator Frequency

Low-Voltage Startup Oscillator

The AAT1415/AAT1415A internal control and reference voltage circuitry receives power from VDD and do not function when VDD is less than 2.5V. To ensure low voltage startup, the CH1 employs a low-voltage startup oscillator (about 200kHz) that activates at 1.2V if a Schottky diode is connected from PWR to OUT1. The startup oscillator drives the internal NMOS at SW1 until VDD reaches 2.5V, at which point voltage control is passed to the normal oscillator (current-mode PWM circuitry). At low input voltages, the CH1 can have difficulty starting into heavy loads.

DESIGN PROCEDURE

Programming the Output Voltage

The output voltage for each channel is programmed using a resistor divider from the output connected to the feedback pins. When setting the output voltage, connect a resistive voltage divider from the channel output to the corresponding IN_ input and then to GND. Choose the lower-side (IN_-to-GND) resistor, then calculate the upper-side (output-to-IN_) resistor as follows:

$$R_{UPPER\_} = R_{LOWER\_}\left(\frac{V_{OUT\_}}{V_{IN\_}} - 1\right) \quad \text{(For Boost / buck),}$$

$$R_{UPPER\_} = R_{LOWER\_}\left(\frac{-V_{OUT\_}}{V_{REF}}\right) \quad \text{(For Inverting),}$$

Where $V_{IN\_}$ is the feedback regulation voltage, 1.250V (AAT1415/AAT1415A, V_{IN3} = 0.8V), and typical values for $R_{LOWER\_}$ are in the range of 10kΩ to 100kΩ.

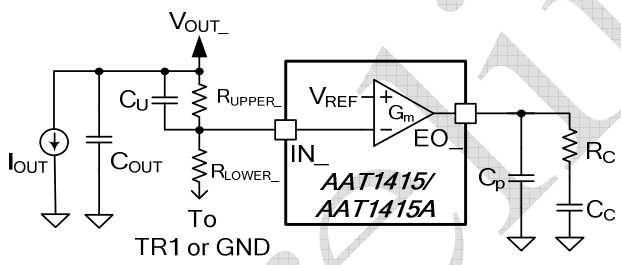


Figure 9a. Feedback Network (For Boost/Buck)

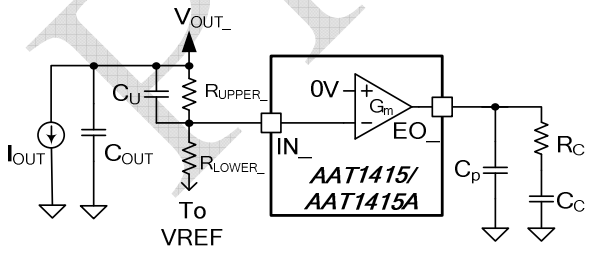


Figure 9b. Feedback Network (For Inverting)

Inductor Selection

The inductor is typically selected to operate with continuous conduction mode (CCM) for best efficiency in boost or buck converter and discontinuous conduction mode (DCM) for better response ability in boost or inverting controller (Table 1 and Table 2). The recommended inductance value range is between 2.2μH and 4.7μH for boost. The recommended inductance value range is between 6.8μH and 22μH for buck. The recommended inductance value range is between 3.3μH and 6.8μH for Inverting. With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated (Table 3). It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. This also needs to be taken into account when selecting an appropriate inductor.

Table 1. Response Ability for Various Topologies

Topology	Response Ability
Boost or Inverting	$\frac{V_{IN}}{L}$
Buck	$\frac{V_{IN} - V_{OUT}}{L}$
V_{IN} : Input Voltage, V_{OUT} : Output Voltage, L : Inductance, Response Ability Unit: $\frac{mA}{\mu s}$	

Table 2. DCM/CCM Critical Inductance Values

Topology	D	DCM/CCM
Boost	$1 - \frac{V_{IN}}{V_{OUT}}$	$\frac{R_{LOAD} \cdot D \cdot (1-D)^2}{2 \cdot f_{SW}}$
Buck	$\frac{V_{OUT}}{V_{IN}}$	$\frac{(1-D) \cdot R_{LOAD}}{2 \cdot f_{SW}}$
Inverting	$\frlac{\lvert V_{OUT} \rvert}{\lvert V_{OUT} \rvert + V_{IN}}$	$\frac{R_{LOAD} \cdot (1-D)^2}{2 \cdot f_{SW}}$
V_{IN} : Input Voltage, V_{OUT} : Output Voltage, R_{LOAD} : Loading, f_{SW} : Switch Frequency, Inductance Unit: Henry		

Table 3. Inductor Peak Current

Topology	Mode	Peak Current
Boost	CCM	$\frac{I_O}{(1-D)}+\frac{\Delta I_L}{2}$, $\Delta I_L=\frac{V_{OUT}\cdot D\cdot(1-D)}{f_{SW}\cdot L}$, $D=1-\frac{V_{IN}}{V_{OUT}}$
	DCM	$\sqrt{\frac{2\cdot(V_{OUT}-V_{IN})\cdot I_O}{L\cdot f_{SW}}}$
Buck	CCM	$I_O+\frac{\Delta I_L}{2}$, $(\Delta I_L=\frac{V_{OUT}\cdot(1-D)}{f_{SW}\cdot L}$, $D=\frac{V_{OUT}}{V_{IN}})$
	DCM	$\sqrt{\frac{2\cdot(V_{IN}-V_{OUT})\cdot V_{OUT}\cdot I_O}{L\cdot f_{SW}\cdot V_{IN}}}$
Inverting	CCM	$I_O+\frac{\Delta I_L}{2}$, $(\Delta I_L=\frac{V_{IN}\cdot D}{f_{SW}\cdot L}$, $D=\frac{\lvert V_{OUT}\rvert}{\lvert V_{OUT}\rvert+V_{IN}})$
	DCM	$\sqrt{\frac{2\cdot\lvert V_{OUT}\rvert\cdot I_O}{L\cdot f_{SW}}}$

V_{IN}: Input Voltage, V_{OUT}: Output Voltage, I_O: Output Current, L: Inductance, f_{SW}: Switch Frequency, Peak Current Unit: Ampere

Schottky Diode Selection

Choose a Schottky diode who's maximum reverse voltage rating is greater than the value in Table 4, and who's current rating is greater than the peak inductor current.

Table 4. Diode and MOS Minimum Voltage Rating

Topology	Minimum Voltage Rating
Boost	V_{OUT}
Buck	V_{IN}
Inverting	$V_{IN}+\lvert V_{OUT}\rvert$

External MOSFET Selection

The boost controller and Inverting controller drive external logic-level MOSFETs. MOSFETs' maximum drain-to-source voltage ($V_{DS(MAX)}$) rating must be greater than the value in Table 4. Their on-resistance ($R_{DS(ON)}$), total gate charge (Q_G) and reverse transfer capacitance (C_{RSS}) are the lower the better.

Input Capacitor

The input current to converters are discontinuous, and therefore input capacitors are required to supply the AC current to converters while maintaining the DC input voltage. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. For insuring stable operation a bypass ceramic 0.1µF capacitor should be placed as close to the IC VDD pin as possible.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE}\approx\frac{\Delta I_L}{2\pi\times f_{SW}\times C_{OUT}}$$

Where V_{RIPPLE} is the output ripple voltage, ΔI_L is the inductor ripple current, f_{SW} is the switching frequency and COUT is the output capacitance. In the case of tantalum or low- ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} \approx \Delta I_L \times R_{ESR}$$

Where V_{RIPPLE} is the output voltage ripple, ΔI_L is the inductor ripple current, and R_{ESR} is the equivalent series resistance of the output capacitors.

Boost Converter Compensation

The compensation resistor and capacitor (Figure 9a) are chosen to optimize control-loop stability. The boost converter employs current-mode control, thereby simplifying the control-loop compensation. When the converter operates with continuous conduction mode (typically the case), a right-half-plane zero appears in the loop-gain frequency response. To ensure stability, the cross over frequency (f_C) should be much less than that of the right-half-plane zero.

For CCM, the right-half-plane zero frequency (f_{RHPZ}) is given by the following:

$$f_{RHPZ} = \frac{V_{OUT\_} \times (1-D)^2}{2\pi \times L \times I_{LOAD}}$$

Typically target cross over frequency (f_C) is the value for 1/6 of the RHPZ. Choose f_C, and then calculate compensation capacitor (C_C) as follows:

$$C_C = \frac{V_{IN\_}}{R_{CS}} \times \frac{G_m}{2\pi \cdot f_C} \times \frac{(1-D)}{I_{LOAD}}$$

Where $V_{IN\_}$ is the feedback regulation voltage, 1.25V (typ), R_{CS} is the current-sense amplifier transresistance, 0.25V/A (typ), G_M is the error amplifier transconductance, 70µS (typ). Select R_C based on the allowed transient-droop (TD%) requirements by the following equation:

$$R_C = I_{L(PK)} \times \frac{R_{CS}}{TD\% \times V_{IN\_} \times G_m}$$

Where $I_{L(PK)}$ is the inductor peak current.

The output filter capacitor (typically ceramic capacitor) is then chosen to cancel the $R_C C_C$ zero:

$$C_{OUT} = \frac{I_{LOAD}}{V_{OUT\_}} \times R_C C_C$$

If the output filter capacitor (typically electrolytic capacitor) has significant equivalent series resistance (ESR), a zero occurs at the following:

$$Z_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

If $Z_{ESR} >> f_C$, it can be ignored. If Z_{ESR} is less than f_C, it should be cancelled with a pole set by capacitor C_P connected from EO_ to GND:

$$C_P = \frac{C_{OUT} \times R_{ESR}}{R_C}$$

If the system wants better transient response, it can parallel a capacitor C_U with $R_{UPPER\_}$ from IN_ to $V_{OUT\_}$:

$$C_U = \frac{1}{2\pi \times R_{UPPER\_} \times f_C \times \left(V_{IN\_} / V_{OUT\_} \right)}$$

If C_P or C_U is calculated to be less than 10pF, it can be omitted. Additionally, C_P or C_U can suppress the inrush current.

So, for a 3.3V/250mA output with V_I = 2.0V, L = 3.5µH, R_{UPPER} = 164k, f_{SW} = 500kHz and transient-droop 5%:

$$C_C = \frac{1.25V}{0.25V/A} \times \frac{70\mu A/V}{2\pi \cdot 35kHz} \times \frac{(1-0.39)}{250mA} \approx 3.3nF,$$

$$R_C = 0.64 \times \frac{0.25V/A}{0.05 \times 1.25 \times 70\mu A/V} \approx 36k\Omega,$$

$$C_{OUT} = \frac{250mA}{3.3V} \times 36k\Omega \times 3.3nF \approx 10\mu F$$

When the C_{OUT} value is two to three times greater than what's calculated above, better output voltage ripple can be achieved.

$$C_U = \frac{1}{2\pi \times 164k\Omega \times 35kHz \times (1.25V/3.3V)} \approx 100pF$$

Buck Converter Compensation

The buck converter employs current-mode control, thereby simplifying the control-loop compensation. When the buck converter operates with continuous inductor current (typically the case), a R_{LOAD} C_{OUT} pole appears in the loop-gain frequency response. To ensure stability, set the compensation $R_C C_C$ (Figure 9a) to zero to compensate for the R_{LOAD} C_{OUT} pole. Then set the loop crossover frequency below 1/5 of the switching frequency. The compensation resistor and capacitor are then chosen to optimize control-loop stability.

Choose the compensation capacitor C_C to set the desired crossover frequency f_C. Determine the value by the following equation:

$$C_C = \frac{V_{IN\_}}{I_{LOAD} \times R_{CS}} \times \frac{G_m}{2\pi \cdot f_C}$$

where $V_{IN\_}$ is the feedback regulation voltage, 1.25V (typ), R_{CS} is the current-sense amplifier transresistance, 0.5V/A (typ), G_m is the error amplifier transconductance, 70µS (typ). Select R_C based on the allowed transient-droop (TD%) requirements by the following equation:

$$R_C = I_{L(PK)} \times \frac{R_{CS}}{TD\% \times V_{IN\_} \times G_m}$$

Where $I_{L(PK)}$ is the inductor peak current.

The output filter capacitor (typically ceramic capacitor) is then chosen to cancel the $R_C C_C$ zero:

$$C_{OUT} = \frac{I_{LOAD}}{V_{OUT\_}} \times R_C C_C$$

If the output filter capacitor (typically electrolytic capacitor) has significant equivalent series resistance (ESR), a zero occurs at the following:

$$Z_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

If $Z_{ESR} >> f_C$, it can be ignored. If Z_{ESR} is less than f_C, it should be cancelled with a pole set by capacitor C_P connected from EO_ to GND:

$$C_P = \frac{C_{OUT} \times R_{ESR}}{R_C}$$

If the system wants better transient response, it can parallel a capacitor C_U with $R_{UPPER\_}$ from IN_ to $V_{OUT\_}$:

$$C_U = \frac{1}{2\pi \times R_{UPPER\_} \times f_C \times \left(V_{IN\_}/V_{OUT\_}\right)}$$

If C_P or C_U is calculated to be less than 10pF, it can be omitted.

So, for a 1.5V/250mA output with V_I = 3.0V, L = 10µH, R_{UPPER} = 20 kΩ, f_{SW} = 500kHz and transient-droop 3%:

$$C_C = \frac{1.25V}{250mA \times 0.5V/A} \times \frac{70\mu A/V}{2\pi \cdot 70kHz} \approx 2.2nF,$$

$$R_C = 0.325A \times \frac{0.5V/A}{0.03 \times 1.25 \times 70\mu A/V} \approx 68k\Omega,$$

$$C_{OUT} = \frac{250mA}{1.5V} \times 68k\Omega \times 2.2nF \approx 22\mu F,$$

$$C_U = \frac{1}{2\pi \times 20k\Omega \times 70kHz \times (1.25V / 1.5V)} \approx 220pF.$$

Boost Controller Compensation

The boost controller employs voltage-mode control to regulate their output voltage. A benefit of discontinuous conduction mode (DCM) is more flexible loop compensation, better response ability and no maximum duty-cycle restriction on boost ratio. When the boost converter operates with discontinuous conduction mode (typically the CCD VH case), the boost controller has a single pole at the following:

$$f_P = \frac{2 \times V_{OUT} - V_I}{2\pi \times R_{LOAD} \times C_{OUT} \times V_{OUT}}$$

Set the loop cross over frequency (f_C) below the lower of 1/10 the switching frequency (f_{SW}). Choose the compensation capacitor C_C to set the desired crossover frequency f_C. Determine the value by the following equation:

$$C_C = \frac{V_{OUT} \cdot V_I}{(2 \cdot V_{OUT} - V_I)} \times \frac{G_m}{2\pi \cdot f_C} \times \sqrt{\frac{V_{OUT}}{M \cdot (V_{OUT} - V_I)}}$$

Where:

$$M = \frac{2 \cdot L \cdot f_{SW}}{R_{LOAD}}$$

The $R_C C_C$ zero is then used to cancel the f_P pole, so:

$$R_C = \frac{V_{OUT} \cdot R_{LOAD} \cdot C_{OUT}}{(2 \cdot V_{OUT} - V_I) \cdot C_C}$$

The typical R_C is under 500 kΩ.

If the system wants better transient response, it can parallel a capacitor C_U with $R_{UPPER\_}$ from IN_ to $V_{OUT\_}$:

$$C_U = \frac{1}{2\pi \times R_{UPPER\_} \times f_C \times \left(V_{IN\_} / V_{OUT\_} \right)}$$

If C_U is calculated to be less than 10pF, it can be omitted. Additionally, C_U can suppress the inrush current

So, for a 13V/30mA output with V_I = 3.0V, L = 3.5 µH, R_{UPPER} = 100 kΩ, f_{SW} = 500kHz:

$$C_C = \frac{13V \cdot 3V}{(2 \cdot 13V - 3V)} \times \frac{70\mu A/V}{2\pi \cdot 50kHz} \times \sqrt{\frac{13V}{8m \cdot (13V - 2V)}} \approx 4.7nF$$

$$R_C = \frac{13V \cdot 433\Omega \cdot 10\mu F}{(2 \cdot 13V - 3V) \cdot 4.7nF} \approx 500k\Omega,$$

$$C_U = \frac{1}{2\pi \times 100k \times 50kHz \times (1.25V / 13V)} \approx 330pF.$$

Inverting Controller Compensation

The inverting controller also employs voltage-mode control to regulate their output voltage. To operate in discontinuous conduction mode (DCM) is preferred for simple loop compensation and freedom from duty-cycle restrictions on the inverter input-output ratio. When the Inverting converter operates with discontinuous conduction mode (typically the CCD VL case), the inverting controller has a single pole at the following:

$$f_P = \frac{1}{\pi \cdot R_{LOAD} \cdot C_{OUT}}$$

Set the loop cross over frequency (f_C) below the lower of 1/10 the switching frequency (f_{SW}). Choose the compensation capacitor C_C to set the desired crossover frequency f_C. Determine the value by the following equation:

$$C_C = \frac{V_I}{(|V_{OUT}| + V_{REF}) \cdot \sqrt{M}} \times \frac{G_m}{2\pi \cdot f_C}$$

Where:

$$M = \frac{2 \cdot L \cdot f_{SW}}{R_{LOAD}}$$

The $R_C C_C$ zero is then used to cancel the f_P pole, so:

$$R_C = \frac{R_{LOAD} \cdot C_{OUT}}{2 \cdot C_C}$$

The typical R_C is under 500kΩ.

If the system wants better transient response, it can parallel a capacitor C_U with $R_{UPPER\_}$ from IN_ to $V_{OUT\_}$:

$$C_U = \frac{1}{2\pi \times R_{UPPER\_} \times f_C \times \left(\frac{V_{IN\_}}{|V_{OUT\_}| + V_{IN\_}} \right)}$$

If C_U is calculated to be less than 10pF, it can be omitted. Additional C_U can suppress the inrush current. So, for a –7V/50mA output with V_I = 3.0V, L = 4.7µH, R_{UPPER} = 56kΩ, f_{SW} = 500kHz:

$$C_C = \frac{3V}{(|-7| + 1.25V) \cdot \sqrt{33.6m}} \times \frac{70\mu A / V}{2\pi \cdot 20kHz} \approx 2.2nF$$

$$R_C = \frac{140\Omega \cdot 10\mu F}{2 \cdot 2.2nF} \approx 300k\Omega,$$

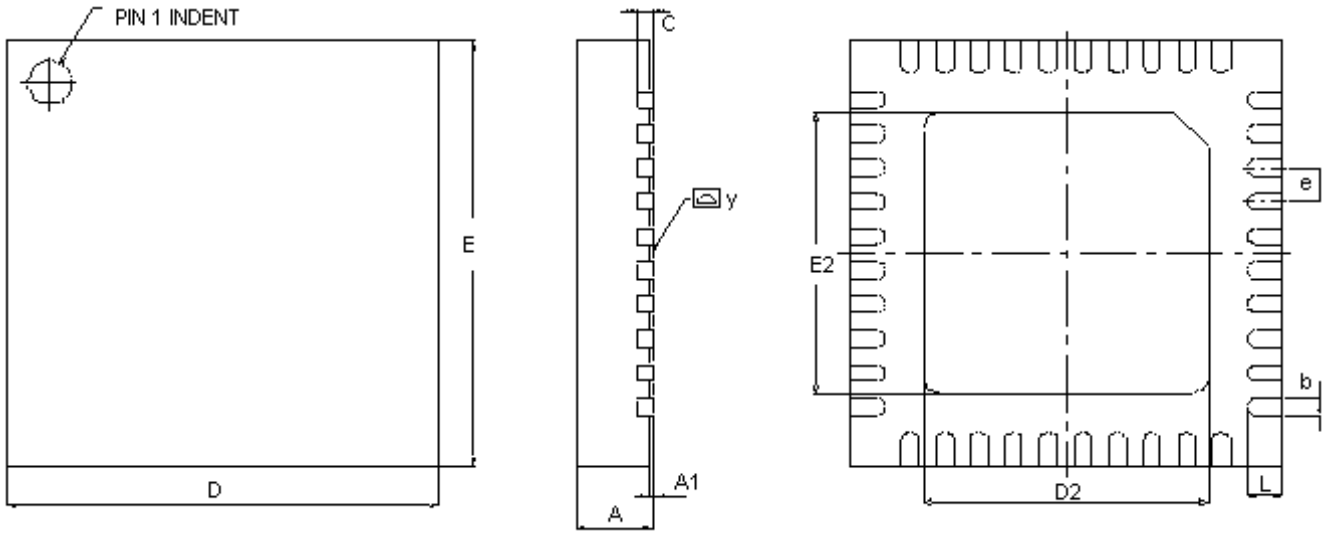
$$C_U = \frac{1}{2\pi \times 56k\Omega \times 20kHz \times \left(\frac{V_{IN\_}}{|V_{OUT\_}| + V_{IN\_}} \right)} \approx 1nF$$

LAYOUT CONSIDERATIONS

Conductors carrying discontinuous currents and any high-current path should be made as short and wide as possible. The compensation network should be very close to the EO_ pin and avoid through VIA. The IC must be bypassed with ceramic capacitors placed close to the VDD and VREF. A separate low-noise ground plane containing the reference and signal grounds should connect to the power-ground plane at only one point to minimize the effects of power-ground currents. Typically, the ground planes are best joined right at the IC. Tie the feedback resistor divider to be very close to output capacitor and far away from the inductor or Schottky diode. Keep the feedback network (IN_) close to the IC. Switching nodes (SW_) should be kept as small as possible and should be routed away from high-impedance nodes such as IN.

PACKAGE DIMENSION

VQFN40 5*5



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.8	0.9	1.0
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
C	------	0.2	------
D	4.9	5.0	5.1
D2	3.25	3.30	3.35
E	4.9	5.0	5.1
E2	3.25	3.30	3.35
e	------	0.4	------
L	0.35	0.40	0.45
y	0	------	0.075